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CLASS TEST 2019-20

ELECTRICAL ENGINEERING

Subject : Microprocessors

Date of test : 15/03/2019

Answer Key

1.	(a)	7.	(c)	13.	(b)	19.	(c)	25.	(c)
2.	(c)	8.	(b)	14.	(c)	20.	(c)	26.	(a)
3.	(a)	9.	(b)	15.	(b)	21.	(d)	27.	(d)
4.	(c)	10.	(d)	16.	(d)	22.	(a)	28.	(b)
5.	(b)	11.	(c)	17.	(b)	23.	(a)	29.	(a)
6.	(a)	12.	(d)	18.	(a)	24.	(d)	30.	(b)

Detailed Explanations

2. (c)

TRAP is also called as RST 4.5

Vector address = $(4.5 \times 8)_{10} = (36)_{10} = (24)_H$
= $(0024)_H$.

TRAP is a positive edge triggered and level triggered interrupt.
RST 6.5 is a level triggered interrupt with third highest priority.
INTR is a level triggered interrupt.

3. (a)

```
MOV H, B      ; H ← B
MOV L, C      ; L ← C
XCHG          ; DE ↔ HL, exchange HL and DE register pair contents
MOV B, H      ; B ← H
MOV C, L      ; C ← L
```

4. (c)

RM is conditional return instruction. When sign flag is set RM is executed with three machine cycles and 12 T-states.

5. (b)

Memory chip has 10 address lines and 8 data lines. As control enable is active low and given to NAND gate output. For chip to be enabled A_{15}, A_{14}, A_{13}, A_{12}, A_{11} and A_{10} has to be ones.

A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	Address
1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	$(FC00)_H$
1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	1	
		⋮									⋮					⋮
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	$(FFFF)_H$

7. (c)

Here register C acts as counter and is loaded with 7. Loop is executed 7-times.
Total T-states = 7 T + 7(4 T) + 6(10 T) + 7 T = 102 T-states

8. (b)

PSW register can be seen as accumulator register with flag register.

			Status Register							
PSW =	Accumulator	+	S	Z	X	AC	X	P	X	CY

contents of register B are added to register A and the result is stored in register A. Here the flags get affected as ADD is an arithmetic instruction.
∴ PSW = 0000000001X1X1X1
'X' is a don't care bit
PSW = 0000000001110101

9. (b)

When XRA instruction is executed Sign, Zero, Parity flags are modified to reflect the result of operation with Carry and Auxiliary flags being reset.

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10. (d)

Total five memory accesses are involved when the instruction LHLD 2000 is executed by the microprocessor one Op-code fetch cycle and four memory read cycles.

11. (c)

6000 : LXI SP, 1000H// SP is loaded with 1000 H
6003 : PUSH B // Contents of BC are pushed into stack and SP = SP – 2 = 0FFE
6004 : PUSH D // Contents of DE are pushed into stack and SP = SP – 2 = 0FFC
6005 : CALL 2500 // Call the subroutine at 2500 H and push the content of program counter in stack, so SP = SP – 2 = 0FFC – 2 = 0FFA
6008 : POP B // Contents of top of stack are loaded in BC pair and SP = SP + 2 = 0FFA + 2 = 0FFC
6009 : HLT // Halt the program

After HLT instruction is executed PC is stored with 600A and stack pointer with 0FFC

12. (d)

```
LDA 7500 H // Load the contents in location 7500 H to accumulator
CMA        // Complement accumulator ( Ā )
INR A      // Increment A by one ( Ā + 1)
STA 7500 H // Store contents of accumulator to memory locaton 7500 H
HLT        // Halt the program
```

Contents in location 7500 H are two's complemented.

13. (b)

Intel 8237 → DMA controller
Intel 8279 → Display interface
Intel 8259 → Programmable interrupt controller
Intel 8155 → Input Output and timer

14. (c)

```
MVI C, 73 H    ; C ← 73 H
MVI B, 57 H    ; B ← 57 H
MOV A, C       ; A ← C
MOV A, B       ; A ← B
MOV C, A       ; C ← A
MVI D, 37 H    ; D ← 37 H
OUT PORT 1     ; PORT 1 ← 57 H
HLT            ; Halt
```

57 H goes out from the microprocessor accumulator to PORT 1

15. (b)

SPHL ; Load contents of HL into stack pointer. This is a one Byte instruction that needs 6 T-states to execute fully.

16. (d)

Effective memory access time = [Hit ratio × access time in cache memory
+ (1 – Hit ratio) × access time in main memory]
= 0.8 × 10 ns + (1 – 0.8) × 100 ns
= 8 ns + 20 ns
= 28 ns

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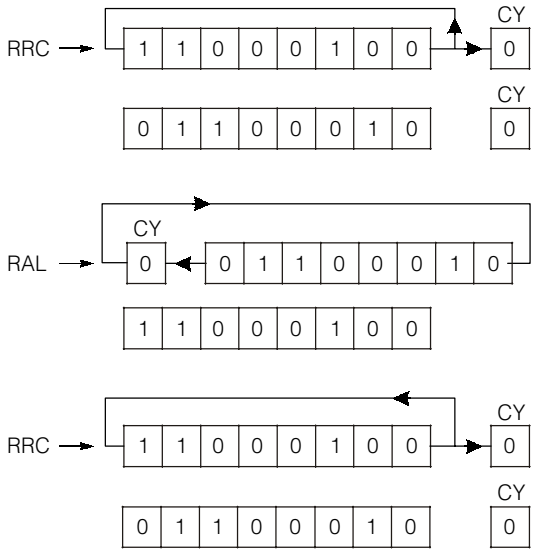
17. (b)

Accumulator is initially loaded with C4 H. Instruction ORA A resets the carry flag



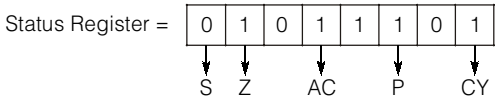
Contents of accumulator are 62 H.

18. (a)

```
LXI SP, 9000      ; SP ← 9000
LXI H, 005D       ; HL ← 005D
PUSH H            ; SP = SP – 2 = 8FFE
POP PSW           ; Pop the contents 005D onto PSW register.
```

PSW = accumulator + status register

PSW = | 00 | 5D |



19. (c)

The loop is executed four times adding the contents of accumulator with decremented contents of register B.

$A = 04 + 04 + 03 + 02 + 01 + 02$

$A = (16)_{10}$

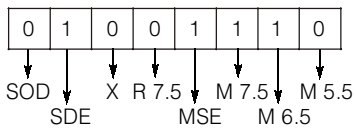
$A = (10)_{H}$

20. (c)

Vector address $= (5 \times 8)_{10} = (40)_{10} = (28)_{H}$

21. (d)

After executing SIM instruction, accumulator set-up for the SIM instruction is shown as



As MSE is enabled, M 7.5 and M 6.5 are masked.

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22. (a)

```
        MVI B, 00 H     ; Load contents 00 into register B
        MVI C, 08 H     ; Load contents 08 into register C
        MOV A, D        ; Move the contents of register D to register A
BACK:   RAR             ; Rotate accumulator contents right with carry flag
        JNC SKIP        ; If CY = 0, move the sequence to SKIP
        JNR B           ; If CY = 1, Increment counter B
SKIP:   DCR C           ; Decrement contents of C by one
        JNZ BACK        ; If z = 0 jump sequence to BACK else Halt
        HLT             ; Halt, buses tristated
```

Clearly we can notice contents of register D are taken to A to number of ones. The number of ones are stored in count register B.

23. (a)

```
        MVI A, 27 H     ; A ← 27 H
        ADD A           ; A ← 27 H + 27 H, A ← 4E H ; CY = 0, P =1
        LXI SP, 2700 H  ; SP ← 2700 H
        PUSH PSW        ; A and flags register contents are stored in 26FF H and 26FF H locations
        POP H           ; Retrieve flags in L
        MOV A, L        ; Flags in accumulator
        CMA             ; Complement accumulator, CY = 1, P = 0
        MOV L, A        ; Accumulator in L
        PUSH H          ; Save on stack
        POP PSW         ; Back to flag register
        HLT             ; Terminate program execution.
```

The program complements the flags.

24. (d)

HLT is a 1 Byte instruction with 5 T-states or more.

25. (c)

Analysis of code:

```
        LXI H, 2200 H   ; Initialize pointer
        MOV A, M        ; Get the number 45 H
        INX H           ; Increment the pointer
        ADD M           ; Add 45 H and 46 H
        DAA             ; Convent HEX to valid BCD ; A ← 91 H
        STA 2300 H      ; Store the result
        HLT             ; Terminate program execution
```

26. (a)

The code performs 2's complement of an 8-bit number. 87 H is loaded in accumulator and is complemented. Contents are incremented by one. The result [2's complement] is stored in C051 H location.

27. (d)

$A \leftarrow (A7)_H$

$A \rightarrow 10100111$

$A \rightarrow 10100111$

Bitwise or $\rightarrow \underline{10100111}$

after ORA A instruction is executed sign flag is set.

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sequence jumps to OUTPRT

$\bar{A} \rightarrow 01011000$

$\bar{A} + 1 \rightarrow 01011001$

Finally $(59)_H$ is displayed at Port 01 H.

28. (b)

```
MVI B, 33 H   ; B ← 33 H
MVI C, 40 H   ; C ← 40 H
PUSH B        ; PUSH the contents of BC pair on to stack
POP H         ; POP the contents of stack into HL pair
SHLD C050     ; Contents of HL are stored in locations C050 and C051 respectively
HLT           ; Halt
```

Finally the contents of C050 are 40 H and C051 are 33 H respectively.

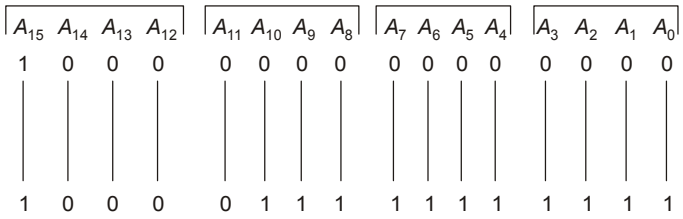
29. (a)

Size of one memory chip = 256 × 1 bits

Required memory size = 1 kB

$$\text{Total chips required} = \frac{1024 \times 8 \text{ bits}}{256 \times 1 \text{ bits}} = 32$$

30. (b)



8000 H - 87FF H

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