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Digital Electronics

EC | EE

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CLASS TEST 2020-2021

EC | EE

Date of Test : 23/02/2020

ANSWER KEY ➤ Digital Electronics

1. (d)	7. (a)	13. (b)	19. (b)	25. (a)
2. (d)	8. (d)	14. (b)	20. (b)	26. (b)
3. (b)	9. (a)	15. (d)	21. (b)	27. (a)
4. (d)	10. (a)	16. (b)	22. (c)	28. (a)
5. (c)	11. (b)	17. (a)	23. (d)	29. (d)
6. (c)	12. (c)	18. (a)	24. (d)	30. (c)

DETAILED EXPLANATIONS

1. (d)

From the decoder circuit it is clear that

$$f(A, B, C) = I_2 + I_4 + I_6$$

now,

	Input	Literals produced	Minterm at the output
I_2	010	$\bar{A}\ C\ \bar{B}$	$(\bar{A}\,\bar{B}\,C) \Rightarrow m_1$
I_4	100	$A\ \bar{C}\ \bar{B}$	$(A\,\bar{B}\,\bar{C}) \Rightarrow m_4$
I_6	110	$A\ C\ \bar{B}$	$(A\,\bar{B}\,C) \Rightarrow m_5$

$$\therefore \quad f(A, B, C) = \Sigma m(1, 4, 5)$$

2. (d)

The *K*-map of Q^+ can be given as follows:

A \ BQ	00	01	11	10
0	0	0	0	0
1	1	1	0	1

$$\therefore \quad Q^+ = A\bar{B} + A\bar{Q}$$

3. (b)

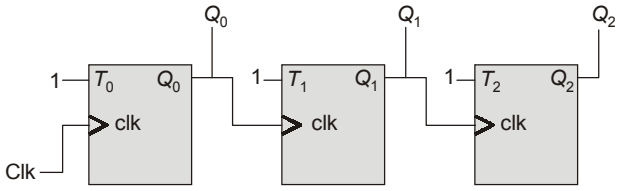
For six states, we require minimum 3 number of flip-flops.

i.e. $2^n \geq \text{MOD}$

$2^n \geq 6$

$n_{\min} = 3$

4. (d)



Thus this will create a MOD 8 or 3 bit down counter.

5. (c)

$$f_{out} = \frac{f_{in}}{\text{MOD (total)}}$$

$$\therefore \quad \text{MOD} = \frac{f_{in}}{f_{out}} = 5 \times 10 \times 2x \times 4$$

$$x = \frac{1}{400} \times \frac{1.6 \times 10^9}{1 \times 10^6} = \frac{1600}{400}$$

$$x = 4 \text{ flip-flops}$$

6. (c)

$\because$ The logic will perform the function of positive AND gate.

Since,

A (Volt)	B (Volt)	T_1	T_2	T_3	Output
V^-	V^-	OFF	OFF	ON	V_{sat}
V^-	V^+	OFF	ON	ON	V_{sat}
V^+	V^-	ON	OFF	ON	V_{sat}
V^+	V^+	ON	ON	OFF	V_{CC}

The corresponding truth table for negative logic:

A	B	Output
1	1	1
1	0	1
0	1	1
0	0	0

Thus the circuit will behave as negative OR-logic.

7. (a)

The output logic function of the given circuit can be expressed as,

$$f = \overline{\left(\overline{(\overline{AB})C}\right)\left(\overline{\overline{C}D}\right)} = (\overline{AB})C + \overline{C}D = (\overline{A} + \overline{B})C + \overline{C}D$$

8. (d)

$$I_R = I_3 + I_2 + I_0$$

$$= \left(\frac{E_{reff}}{2R} + \frac{E_{reff}}{4R} + \frac{E_{reff}}{16R}\right) = \left(\frac{10}{10} + \frac{10}{20} + \frac{10}{80}\right)$$

$$= \frac{130}{80} = \frac{13}{8} = 1.625 \text{ mA}$$

9. (a)

V_1	V_2	Y	M_1	M_2	M_3	M_4
0	0	V_{DD}	OFF	OFF	ON	ON
0	V_{DD}	0	OFF	ON	OFF	ON
V_{DD}	0	0	ON	OFF	ON	OFF
V_{DD}	V_{DD}	0	ON	ON	OFF	OFF

Thus, the gate will be a positive NOR gate.

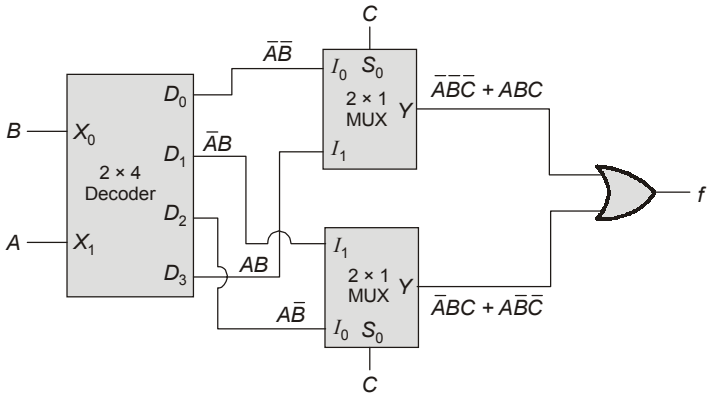
10. (a)

$$t_{max} = 2^{n+1} T_{clock} = 2^9 T_{clock}$$

$$R_{min} = \frac{1}{t_{max}} = \frac{1}{2^9 T_{clock}} = \frac{f_{clock}}{2^9} = \frac{50000}{512} = 97.65 \text{ Hz}$$

11. (b)

The above circuit can be redrawn as



Thus,

$$f = \underbrace{\bar{A}\bar{B}\bar{C} + ABC} + \underbrace{\bar{A}BC + A\bar{B}\bar{C}}$$

$$= \bar{B}\bar{C}(A + \bar{A}) + BC(\bar{A} + \bar{A})$$

$$= \bar{B}\bar{C} + BC$$

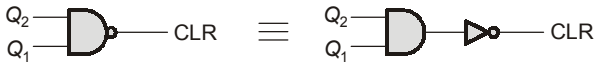
$$= B \odot C$$

12. (c)

The circuit can be designed by using a NAND gate which can be equally represented by an AND gate followed by not gate.

$\because$ The clear should be on the 6th pulse. i.e., when the output $(Q_2Q_1Q_0) = (110)$.

So, the combinational circuit is as follows:



13. (b)

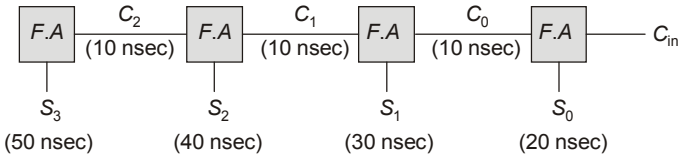
To find the essential prime implicants, we have to select those groups in which there is atleast one min-term which is part of only that group and cannot be grouped by any other way.

AB \ CD	00	01	11	10
00	0	0	1	0
01	1	1	1	0
11	0	1	1	1
10	0	1	0	0

So, there are 4 prime implicants in the given *K*-map.

14. (b)

The 4-bit parallel adder can be analyzed as follows:



Thus, the last sum bit will be generated in 50 nsec.
Thus, the maximum rate of 4-bit additions possible is,

$$\frac{1}{50\times10^{-9}}/\text{sec} = \frac{10^9}{50}/\text{sec} = 20\times10^6/\text{sec}$$

15. (d)

$$f_1(A,B,C) = \Sigma m(2, 3, 4)$$
$$f_2(A,B,C) = \Sigma m(2, 3, 4)$$

for output f_{out} to be zero, f_3 should be equal to

$$\therefore \quad f_3(A,B,C) = \Sigma m(0, 1, 5, 6, 7)$$

Hence, the maximum number of possible minterms = 5.

16. (b)

The given circuit represents a 3-bit counter. So the count can be represented as

Clk	Q_2	Q_1	Q_0	
Initially	0	0	0	
1	0	0	1	
2	0	1	0	
3	0	1	1	
4	1	0	0	
5	1	0	1	$\Rightarrow$5th clock pulse
6	1	1	0	
7	1	1	1	

$$\therefore \quad Y = Q_2 \oplus Q_1 \oplus Q_0$$
$$= 1 \oplus 0 \oplus 1 = 0$$

17. (a)

$$\because \quad Q + \bar{Q} = 1 \text{ always, thus the flip-flop will toggle always.}$$

$$\therefore \quad f_{out} = \frac{f_{clk}}{2} = \frac{10}{2}\times10^3 = 5\ \text{kHz}$$

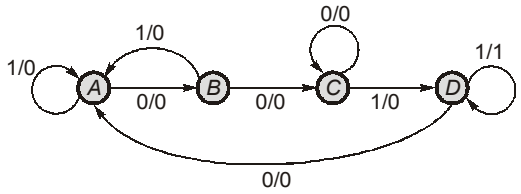
18. (a)

At first cycle, the inputs of flip-flop are

$$J_2K_2 = 1\ 0 \text{ (Set)}$$
$$J_1K_1 = 0\ 1 \text{ (Reset)}$$
$$J_0K_0 = 0\ 1 \text{ (Reset)}$$
$$\therefore \quad Q_2 = 1$$
$$Q_1 = 0$$
$$Q_0 = 0$$
$$\therefore \quad \text{Output}\,(Q_2Q_1Q_0) = (100)_2$$

19. (b)

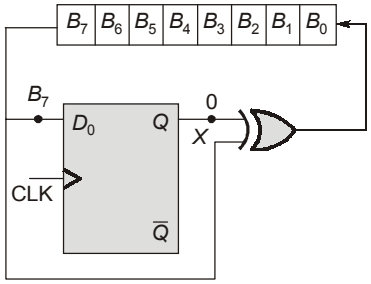
The state diagram can be drawn as



Hence, minimum number of states = 4.

20. (b)

Initially the input at 'D' will be B_7 and the signal X is '0'



Therefore $B_0 = B_7 \oplus 0$

For the next clock pulse $D = B_6$

$X = B_7$

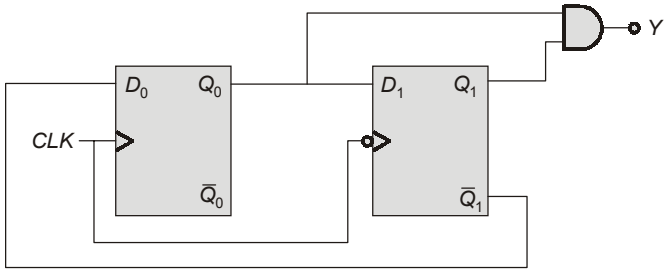
$\therefore \quad B_0 = B_7 \oplus B_6$

and $B_1 = B_7 \oplus 0$

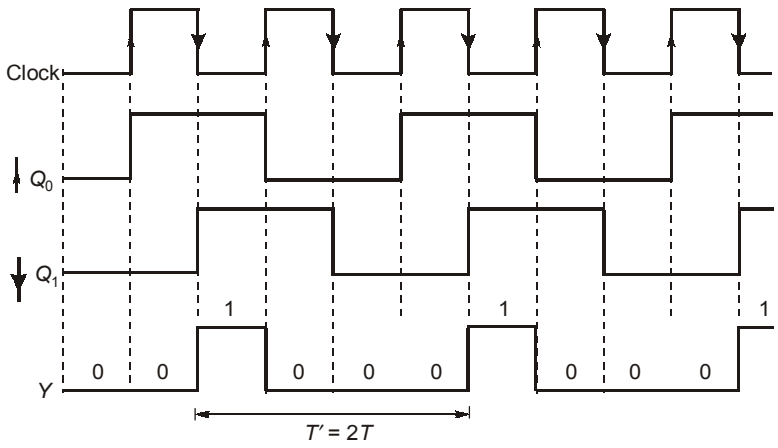
similarly for every clock pulse each bit of register shows the Ex-OR combination of binary inputs. Thus, the circuit represents the conversion from binary to Gray code.

21. (b)

Assume the output of both the flip-flops is 0 initially.



Waveforms :



$$\text{Duty cycle} = \frac{T_{ON}}{T_{ON} + T_{OFF}} \times 100\% = \frac{1}{1+3} \times 100\%$$

$$= \frac{1}{4} \times 100\% = 25\%$$

22. (c)

Here

$$J_0 = 1,$$
$$K_0 = Q_2,$$
$$J_1 = \bar{Q}_2 \odot Q_0,$$
$$K_1 = 1,$$
$$J_2 = Q_1,$$
$$K_2 = 1$$

CLK	Q_2	Q_1	Q_0
Initial state	0	0	0
1	0	0	1
2	0	1	1
3	1	0	1
4	0	0	0

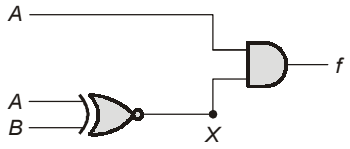
Modulus of the counter is 4.

$$4\overline{)115}\ 28$$
$$8$$
$$35$$
$$32$$
$$3 \text{ clock pulses}$$

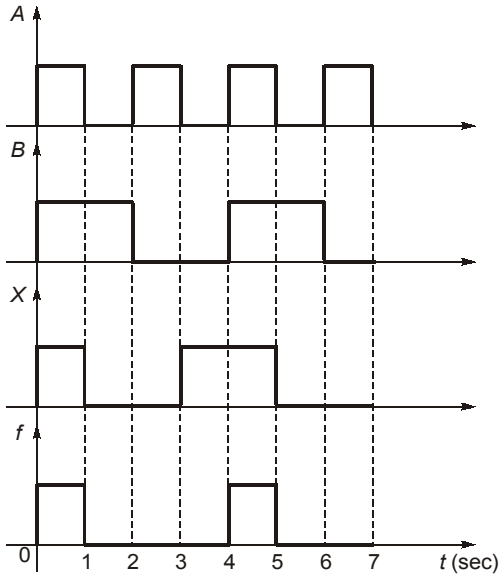
Thus, the count after 115 clock pulses will be $(Q_2Q_1Q_0) = 101$.

23. (d)

Since their is no propagation delay, the given circuit can be reduced as,



Now, the waveform at point X can be found out by using EX-NOR operation of A and B.
The waveform of f can be drawn by taking AND operation of A and X as follows:



24. (d)

The logic outputs of the OR gates can be given as

$$F_1 = \Sigma m(0, 1, 2, 4, 6)$$
$$F_2 = \Sigma m(0, 3, 6)$$
$$F_3 = \Sigma m(0, 4, 6, 7)$$

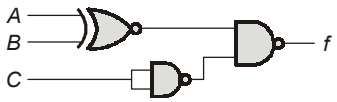
After passing the functions through a NAND gate, we get,

$$f = \overline{F_1 \cdot F_2 \cdot F_3}$$

$$\overline{f} = F_1 \cdot F_2 \cdot F_3 = \Sigma m(0, 6)$$

$$\overline{f} = \bar{A}\bar{B}\bar{C} + AB\bar{C} = (\bar{A}\bar{B} + AB) \cdot \bar{C} = (A \odot B) \cdot \bar{C}$$

$$f = (A \oplus B) + C = \overline{(A \odot B)(\bar{C})}$$



Thus, we require 5 + 2 = 7 gates.
5 for EX-NOR gate and 2 more NAND gates.

25. (a)

$$D_1 = Q_1 Q_0 \odot X$$

$$D_0 = \bar{Q}_1$$

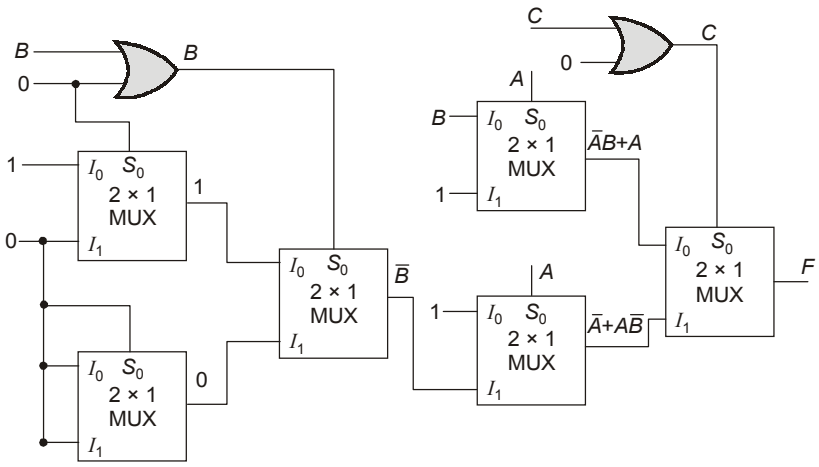
$$Z = Q_0 + X$$

The state table of the given circuit can be developed as follows:

Present State		Input	FF Inputs		Next State		Output
Q_1	Q_0	X	D_1	D_0	Q_1^+	Q_0^+	Z
0	0	0	1	1	1	1	1
0	0	1	0	1	0	1	1
0	1	0	1	1	1	1	1
0	1	1	0	1	0	1	1
1	0	0	1	0	1	0	0
1	0	1	0	0	0	0	1
1	1	0	0	0	0	0	0
1	1	1	1	0	1	0	1

The state diagram given in option (a) satisfies this.

26. (b)



$$\therefore \quad F = \bar{C}(A + \bar{A}B) + C(\bar{A} + A\bar{B}) = \bar{C}(A + B) + C(\bar{A} + \bar{B})$$
$$= A\bar{C} + B\bar{C} + \bar{A}C + \bar{B}C = (A \oplus C) + (B \oplus C)$$

27. (a)

The given circuit is BCD to Excess-3 code converter with BCD inputs $A_{MSB}\ B\ C\ D_{LSB}$ and Excess-3 code output $W_{MSB}\ X\ Y\ Z_{LSB}$.

Since, each code uses 4-bits to represent a decimal digit. There must be four input variables and four output.

Decimal values	Input				Output				Decimal values
	A	B	C	D	W	X	Y	Z	
0	0	0	0	0	0	0	1	1	3
1	0	0	0	1	0	1	0	0	4
2	0	0	1	0	0	1	0	1	5
3	0	0	1	1	0	1	1	0	6
4	0	1	0	0	0	1	1	1	7
5	0	1	0	1	1	0	0	0	8
6	0	1	1	0	1	0	0	1	9
7	0	1	1	1	1	0	1	0	10
8	1	0	0	0	1	0	1	1	11
9	1	0	0	1	1	1	0	0	12

K-map for *Y*

AB \ CD	$\bar{C}\bar{D}$	$\bar{C}D$	CD	$C\bar{D}$
$\bar{A}\bar{B}$	1		1	
$\bar{A}B$	1		1	
AB	X	X	X	X
$A\bar{B}$	1		X	X

Where, don't care '*X*' filled for decimal digits 10 -15.

$$Y = CD + \bar{C}\bar{D} = C \odot D$$

28. (a)

$$2r + 3 + 4r + 4 + r + 4 + 3r + 2 = 2r^2 + 2r + 3$$
$$10r + 13 = 2r^2 + 2r + 3$$
$$2r^2 - 8r - 10 = 0$$
$$r^2 - 4r - 5 = 0$$
$$r = 5, -1$$

$\because$ Radix cannot be negative

$\therefore \quad r = 5$

29. (d)

The accuracy is ± 0.1% of full scale, i.e.

$$\text{Accuracy} = \pm\frac{0.1}{100} \times 1.260\ \text{V} = \pm 1.26\ \text{mV}$$

The offset error is = ± 1 mV

$\therefore$ maximum error = ± 1.26 mV + ± 1 mV

= ± 2.26 mV

30. (c)

Number of states for 8-bit up-counter = $2^8 - 1 = 255$

thus the counter ranges from –0 to 255

Hence, to go from $(10101011)_2 = (171)_{10}$ to $(00111010)_2 = (58)_{10}$

The counter has to go initially from 171 to 255 and then from 0 to 58.

Hence,

from 171 to 255 = 255 – 171 = 84 clock pulse required

from 255 to 0 = 1 clock pulse requried

and from 0 to 58 = 58 clock pulse requried

$\therefore$ The total number of clock pulse required is

$= 84 + 1 + 58$

$= 143$

■■■■