ESE 2019

UPSC ENGINEERING SERVICES EXAMINATION

Main Examination

Thoroughly Revised and Updated | 18 Previous Solved Papers

Electrical Engineering

Conventional Solved Questions

Paper-II

Also useful for

State Engineering Services Examinations

MADE EASY Publications

www.madeeasypublications.org

MADE EASY Publications

Corporate Office: 44-A/4, Kalu Sarai (Near Hauz Khas Metro Station), New Delhi-110016
E-mail: infomep@madeeasy.in
Contact: 011-45124660, 0-8860378007
Visit us at: www.madeeasypublications.org

ESE-2019 : Main Examination
Electrical Engineering : Paper-II | Conventional Solved Questions : (2001-2018)

1st Edition : 2008
2nd Edition : 2009
3rd Edition : 2010
4th Edition : 2011
5th Edition : 2012
6th Edition : 2013
7th Edition : 2014
8th Edition : 2015
9th Edition : 2016
10th Edition : 2017

11th Edition: 2018

Director's Message

During the last few decades of engineering academics, India has witnessed geometric growth in engineering graduates. It is noticeable that the level of engineering knowledge has degraded gradually, while on the other hand competition has increased in each competitive examination including GATE and UPSC examinations. Under such scenario higher level efforts are required to take an edge over other competitors.

B. Singh (Ex. IES)

The objective of MADE EASY books is to introduce a simplified approach to the overall concepts of related stream in a single book with specific presentation. The topic-wise presentation will help the readers to study & practice the concepts and questions simultaneously.

The efforts have been made to provide close and illustrative solutions in lucid style to facilitate understanding and quick tricks are introduced to save time.

Following tips during the study may increase efficiency and may help in order to achieve success.

- Thorough coverage of syllabus of all subjects
- Adopting right source of knowledge, i.e. standard reading text materials
- Develop speed and accuracy in solving questions
- Balanced preparation of Paper-I and Paper-II subjects with focus on key subjects
- Practice online and offline modes of tests
- Appear on self assessment tests
- Good examination management
- Maintain self motivation
- Avoid jumbo and vague approach, which is time consuming in solving the questions
- Good planning and time management of daily routine
- Group study and discussions on a regular basis
- Extra emphasis on solving the questions
- Self introspection to find your weaknesses and strengths
- Analyze the exam pattern to understand the level of questions
- Apply shortcuts and learn standard results and formulae to save time

B. Singh (Ex. IES)
CMD, MADE EASY Group

ESE 2019 : Main Examination

Electrical Engineering: Paper-II

Conventional Solved Questions of UPSC Engineering Services Examination

Contents

■■■

1 Analog Electronics

Revised Syllabus of ESE: *Operational amplifiers – characteristics and applications.*

1. Operational Amplifier-Characteristics and Application

Q.1 In an ideal operational amplifier, the voltage gain for the common mode signal is

(a) 0 (b) 0.5

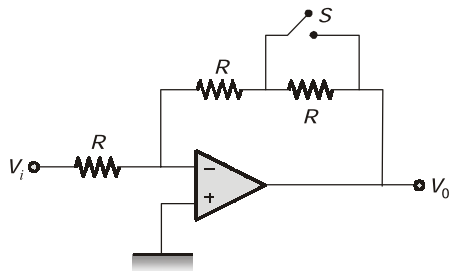
(c) 2.0 (d) infinite

[2 marks : 2002]

Solution: (a)

For an ideal operational amplifier, the voltage gain for the common mode signal is equal to zero.

Q.2 The magnitude of the gain in the inverting operational amplifier circuit shown in figure is *Y*, with the switch open.



When the switch is closed the magnitude of the gain is

(a) $-Y$ (b) $Y/2$

(c) $2Y$ (d) $-2Y$

[2 marks : 2003]

Solution: (b)

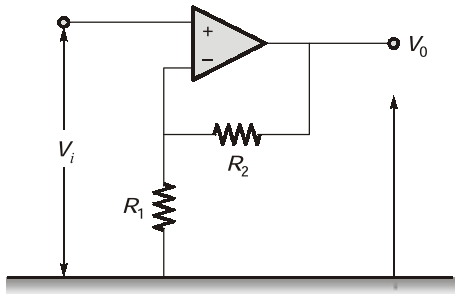
For inverting operational amplifier

$$V_0 = -\left(\frac{R_f}{R_1}\right)V_i$$

For switch is open, $$Y = \frac{V_0}{V_i} = -\left(\frac{2R}{R}\right) = -2$$

For switch is closed, $$Y' = \frac{V_0}{V_i} = -\left(\frac{R}{R}\right) = -1 = \left(\frac{Y}{2}\right)$$

Q.3 The operational amplifier circuitry is given below. Determine its gain and indicate its applicability.

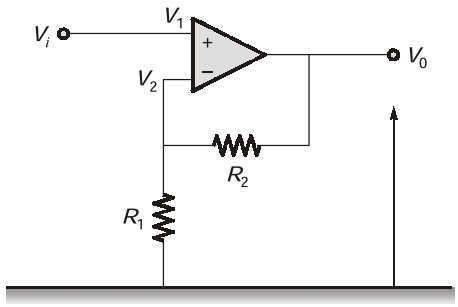


[7 marks : 2003]

Solution:

$$V_1 = V_i$$

and
$$V_2 = \frac{V_0 \times R_1}{R_1 + R_2}$$



By virtual ground concept,

$$V_1 = V_2$$

$$\therefore \quad V_i = \frac{V_0 \times R_1}{R_1 + R_2}$$

$$\therefore \quad V_0 = \left(\frac{R_1 + R_2}{R_1}\right) V_i$$

Applications:

1. Used as comparator
2. As a zero crossing detector
3. Used as voltage follower circuit
4. Used in active peak detector
5. Used in rectifier circuit
6. Used in S-H circuit

Q.4 Explain the operation of a Schmitt trigger circuit using an operational amplifier. Discuss the effect of hysteresis in such a circuit.

[8 marks : 2003]

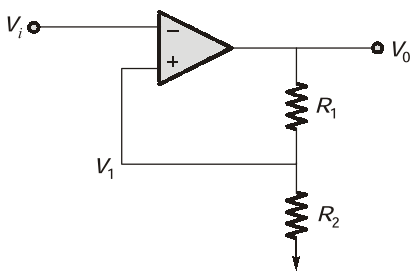
Solution:

Schmitt trigger or wave shaping circuit:

It is a switching circuit which converts non-rectangular wave form into rectangular waveform.

$$V_{UT} = \beta\, V_{sat} = \frac{R_2}{R_1 + R_2} V_0$$

$$V_{LT} = -\beta\, V_{sat} = \frac{-R_2}{R_1 + R_2} V_0$$



Schmitt trigger circuit:

$$V_1 = \beta V_0$$

where, $\beta = \dfrac{R_2}{R_1 + R_2}$

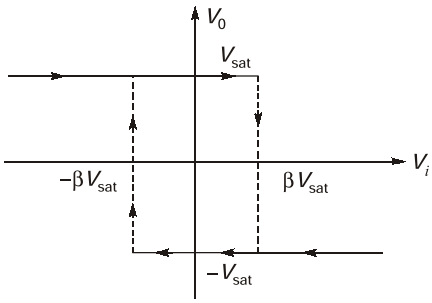
Transfer characteristics of schmitt trigger exhibit hysteresis characteristics.

Let us consider voltage V_i is less than (V_1) we get the output of (+) ($V_{saturation}$) and if 'V_i' is increasing, then V_0 remains ($+V_{sat}$) until ($V_i = V_1$), at this critical value, output voltage switches to $V_0 = (-V_{saturation})$ and remain at this value, as long as ($V_i > V_0$).

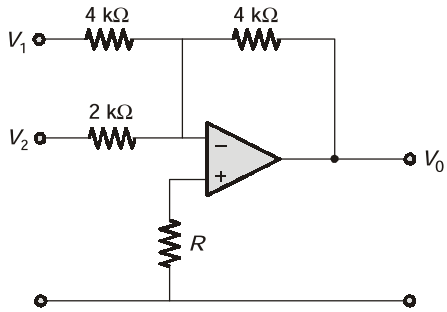
The difference between V_{UT} and V_{LT} is defined as hysteresis V_H and given as

$$V_H = V_{UT} - V_{LT} = \frac{2R_2 V_0}{R_1 + R_2}$$

In such a circuit due to hysteresis loop, no transaction can takes place when $-\beta V_{sat} < V_i < \beta V_{sat}$



Q.5 The most appropriate value of '*R*' in the circuit shown is



(a) 0 (b) 1 kΩ
(c) 2 kΩ (d) 4 kΩ

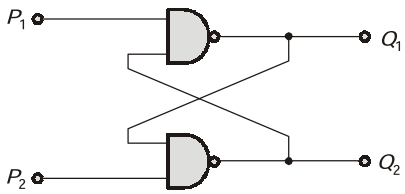
[2 marks : 2004]

Solution: (a)

R is the dc resistance seen from the –ve terminal by removing all the sources by its internal resistance.

$\therefore \quad R = 2\ k\Omega \parallel 4\ k\Omega \parallel 4\ k\Omega = 1\ k\Omega$

Q.6 The correct match between the pin numbers of an Op-Amp μA 741 in the left column and their functions in the right columns are



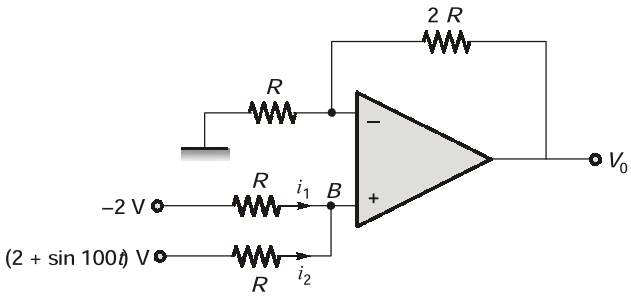
Pin number		Functions	
(A)	2	(P)	output
(B)	3	(Q)	non-inverting (+1 N)
(C)	4	(R)	inverting (–1 N)
(D)	6	(S)	$-V_{CC}$
		(T)	$+V_{CC}$

[5 marks : 2004]

Solution:

2 – (*R*) – inverting (–1 N)
3 – (*Q*) – non-inverting (+1 N)
4 – (*S*) – V_{CC}
6 – (*P*) – output

Q.7 A non inverting operational amplifier summer is shown in the below figure. The output voltage V_0 is



(a) $\frac{3}{2}\sin 100t$ (b) $3\sin 100t$

(c) $\sin 100t$ (d) $2\sin 100t$

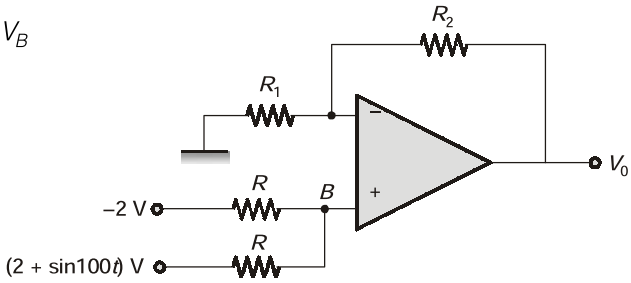
[2 marks : 2005]

Solution: (a)

$$R_2 = 2R$$
$$R_1 = R$$

According to concept of non-inverting amplifier

$$V_0 = V_B\left[1+\frac{R_2}{R_1}\right] = V\left(1+\frac{2R}{R}\right) = 3V_B$$



Now, $$V_B = -2\times\frac{R}{2R}+(2+\sin 100t)\times\frac{R}{2R}$$

$$= -1+1+\frac{\sin 100t}{2}$$

$$V_B = \frac{\sin 100t}{2}$$

$\therefore$ $$V_0 = 3V_B = \frac{3}{2}\sin 100t$$

Q.8 Describe with necessary diagrams:

(i) an Integrator, and

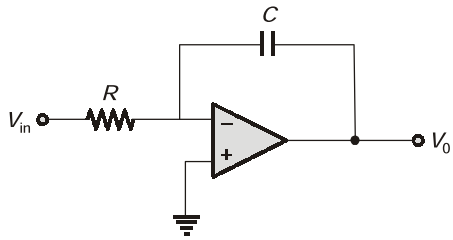
(ii) a differentiator using operational amplifier circuits. How the offset voltage can be minimized in an integrator at the output, and what is to be done to reset the integrator?
Discuss how in a practical differentiator high frequency oscillation can be prevented? How the outputs of a differentiator varies when (a) Ramp input is used, (b) Rectangular input is used?

[20 marks : 2005]

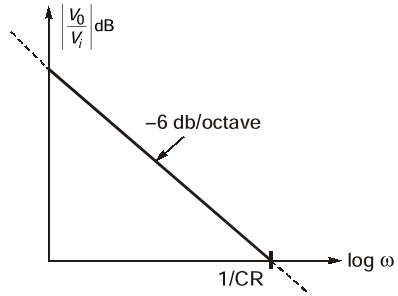
Solution:

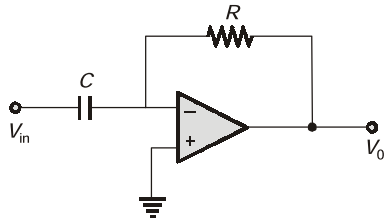
$$V_0 = \frac{-1}{RCs}V_{in}$$

$\therefore$ $$V_0(t) = \frac{-1}{RC}\int V_{in}\,dt$$

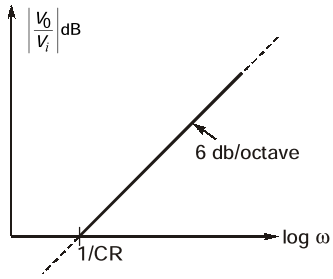


Integrator circuit





Differentiator Circuit



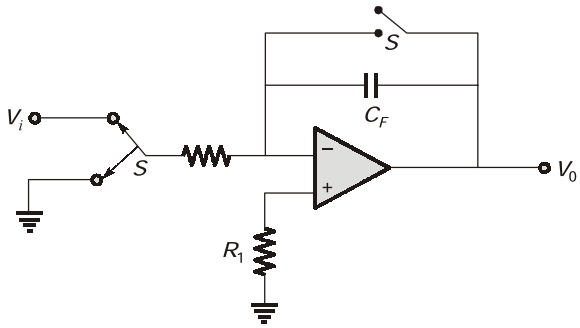
$$\therefore \quad V_0 = -RCs \times V_{in}$$

$$\therefore \quad V_0 = -RC\frac{d}{dt}V_{in}$$

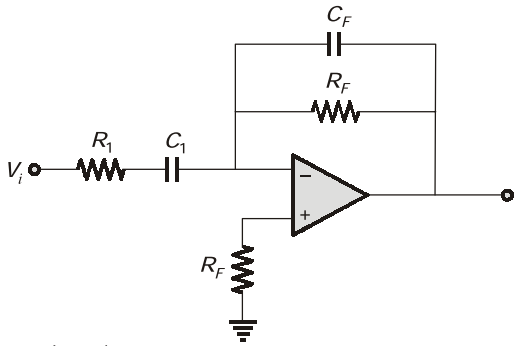
In integrator, feed back element is capacitor and thus at dc, where the capacitor behaves as an open circuit, there is no negative feedback. The offset voltage can be minimised using a resistance connected across the integrator capacitance *C*.

Practically we consider differentiator circuit as a 'noise magnifier. This is due to the spike introduced at the output every time there is a sharp change in $V_i(t)$.

For this reason it suffers stability problems. Otherwise for high frequency (ω_0), input applied to differentiator will get multiple of factor $-(RC\,\omega_0)$. Hence for a differentiator, level at the output increase immensely. We use an external circuit to reset the integrator as:



To eliminate the problem of high frequency oscillation in a differentiator circuit, circuit of differentiator is modified as:



and we take $R_1C_1 = R_FC_F$

For this we get, $f_b = \dfrac{1}{2\pi R_1C_1}$

So, till frequency f_b gain of differentiator increases but as frequency further increases above f_b, gain decreases at rate of –20 dB/decade so problem of instability at high frequency is solved.

(i) The output of the differentiator due to ramp input will be step signal.

$$r(t) = t$$

Output, $$c(t) = \frac{d}{dt}r(t) = u(t)$$

(ii) For a rectangular input

$$r(t) = u(t) - u(t-T)$$

$$\therefore \quad \text{output} = \delta(t) - \delta(t-T)$$

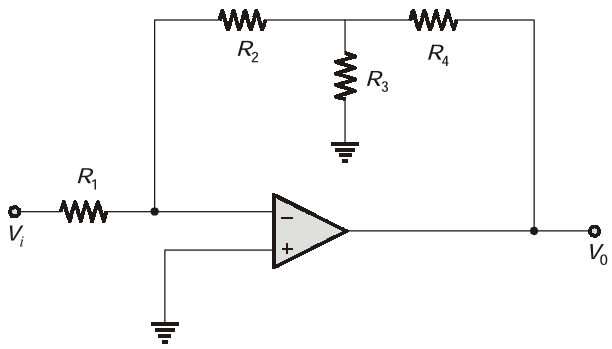
Q.9 An operational Amplifier is basically a
(a) Low gain A.C. Amplifier
(b) High gain D.C. Amplifier
(c) High gain R.C. coupled Amplifier
(d) Low gain Transformer-coupled Amplifier

[2 marks : 2007]

Solution: (b)

An operational amplifier is basically a high gain DC amplifier.

Q.10 Derive an expression for the closed loop gain V_0/V_i of the circuit shown below. Assume ideal OP-AMP.



[10 marks : 2007]

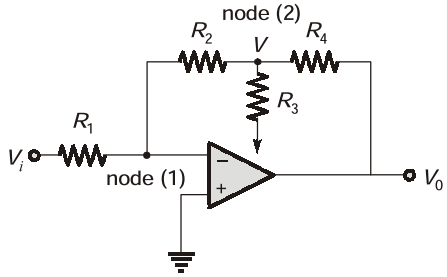
Solution:

By applying KCL at node (1)

By Virtual ground concept, voltage at node 1 = 0 V

$$\frac{0-V_i}{R_1}+\frac{0-V}{R_2} = 0$$

$$\therefore \quad V = -\left(\frac{R_2}{R_1}\right)V_i$$



Applying KCL on node 2,

$$\frac{V-0}{R_2}+\frac{V-V_0}{R_4}+\frac{V}{R_3} = 0$$

$$V\left(\frac{1}{R_2}+\frac{1}{R_4}+\frac{1}{R_3}\right) = \frac{V_0}{R_4}$$

$$V\left(\frac{R_3R_4+R_2R_3+R_2R_4}{R_2R_3R_4}\right) = \frac{V_0}{R_4}$$

Putting value of V_i in above expression,

$$\frac{-R_2}{R_1}\left(\frac{R_3R_4+R_2R_3+R_2R_4}{R_2R_3R_4}\right)\times R_4 = \frac{V_0}{V_i}$$

$$\therefore \quad \left(\frac{V_0}{V_i}\right) = \frac{-\left(R_3R_4+R_2R_3+R_2R_4\right)}{R_1R_3}$$

2 Digital Electronics

Revised Syllabus of ESE: *Combinational and sequential logic circuits, multiplexers, multi-vibrators, sample and hold circuits, A/D and D/A converters, basics of filter circuits and applications, simple active filters; basics of linear integrated circuits.*

1. Logic Gates and Switching Circuits

Q.1 Implement the following operations: $\vec{F} = \bar{x}\,\bar{y} + xy + \bar{y}\,z$

Using:

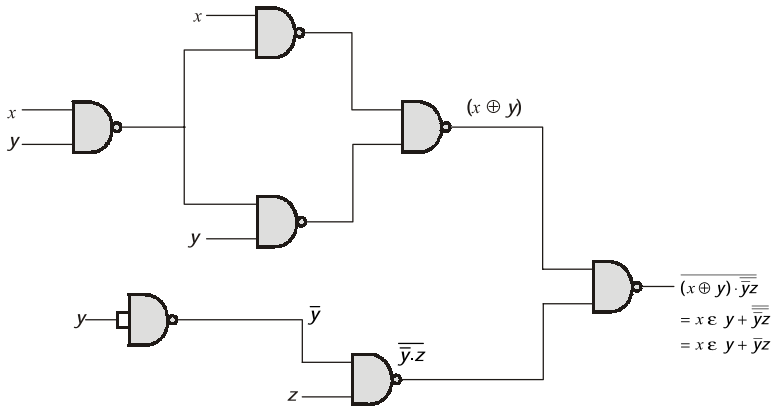
(i) Nand gates only (ii) NOR gates only

(iii) AND and NOT gates (iv) OR and NOR gates

[10 marks : 2001]

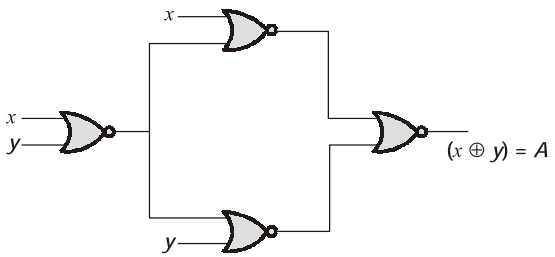
Solution:

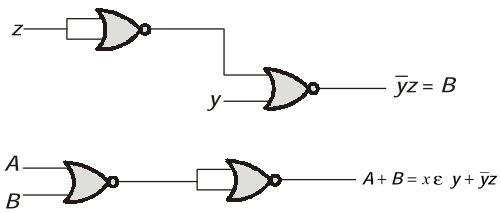
(i)
$$F = \bar{x}\,\bar{y} + xy + \bar{y}z$$
$$F = x \odot y + \bar{y}\,z$$
$$\bar{F} = \overline{x \odot y + \bar{y}\,z}$$
$$\bar{F} = x \oplus y + \bar{y}\,z$$
$$F = \overline{\underbrace{x \oplus y}_{A} + \underbrace{\bar{y}\,z}_{B}} = \overline{A \cdot B}$$
$$A = x \oplus y$$
$$B = \overline{\bar{y}\,z}$$



(ii) Using NOR gates

$$F = \overline{xy} + xy + \bar{y}z$$
$$F = x \odot y + \bar{y}z$$
$$= A + bA + B(A = x \odot y, B = \bar{y}z)$$
$$\bar{F} = \overline{x \odot y}.\overline{\bar{y}\,z}$$





(iii) $\because$ NAND = AND + NOT $\rightarrow$ So replace all NAND gates in (i) part by AND + NOT

(iv) $\because$ NOR = OR + NOT $\rightarrow$ So replace all NOR gates by OR + NOT.

Q.28 Show how n-channel enhancement MOSFETs can be connected to obtain (i) NOR logic and (ii) NAND logic. Verify the logical operation in each case.

[8 marks : 2009]

Solution:

NMOS NAND:

Figure shows a two-input NAND gate using NMOS field-effect transistors. Transistors T_1 and T_2 are of the enhancement type and T_3, which acts as the load resistance, is of the depletion type.

If $A = 0$ and $B = 0$ (i.e. A and B have 0-V inputs), transistors T_1 and T_2 will remain OFF. Then, output $Z = V_{DD}$ (logic 1). The same situation prevails, when $A = 0$, $B = 1$; and $B = 0$, $A = 1$ (here logic 1 = V_{DD}). Now, if $A = B = 1$, then both T_1 and T_2 conduct and the output $Z = 0$. This may be summarized as

$$\left.\begin{array}{lll} A=0, & B=0, & Z=1 \\ A=0, & B=1, & Z=1 \\ A=1, & B=0, & Z=1 \\ A=1, & B=1, & Z=0 \end{array}\right\} \quad \ldots(i)$$

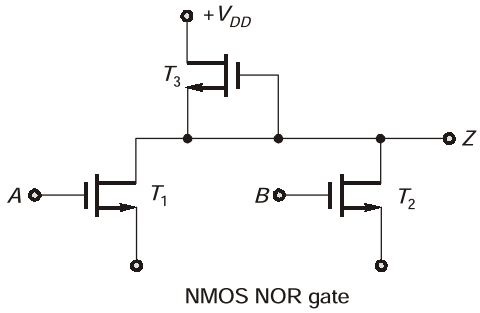
The logic relations in equation (i) are seen to be that of the NAND operation. So, we conclude that the logic gate shown in figure performs positive logic NAND operation.

NMOS NOR:

In this case, we connect the transistors in parallel, as shown in figure.

We notice that,

$$\left.\begin{array}{lll} A=0, & B=0, & Z=1 \\ A=0, & B=1, & Z=0 \\ A=1, & B=0, & Z=0 \\ A=1, & B=1, & Z=0 \end{array}\right\} \quad \ldots(ii)$$



NMOS NOR gate

where logic 0 represents zero volt and logic 1 represents $+V_{DD}$. When 0 volt is applied at the inputs of the transistors they remain OFF, and when V_{DD} is applied at the inputs, the transistors conduct. We find that equation (ii) represents a NOR function.

Q.29 Among DTL, RTL, ECL and CMOS logic families, ECL has the propagation delay and power dissipation/gate respectively as

(i) low, high (ii) low, low

(iii) high, low (iv) high, high

[2 marks : 2011]

Solution:

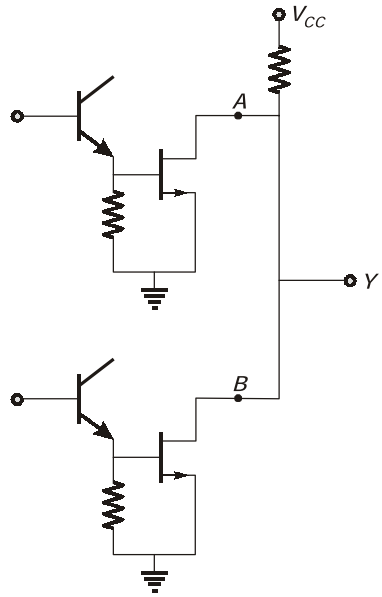
ECL is fastest logic family so propagation delay will be low but due to use non-saturated region of transistor power dissipation is high. So (i) is correct option.

Q.30 Prove the two open collector TTL inverters when connected together produce the NOR gate.

[4 marks : 2014]

Solution:

A and B are the outputs of the two open collector devices. Either open collector output "Pulls down" the voltage at Y.

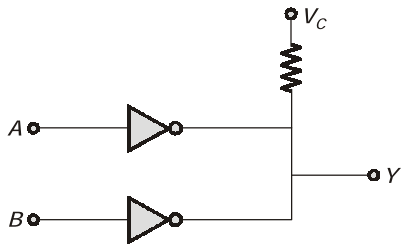


Truth table:

A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

$Y = AB$

From above, we see that the outputs of two open collector gates, when put in parallel, create an AND function. So, $Y = A'B'$. But by, DeMorgan's law, $A'B' = \overline{A+B}$. Thus, two open collector inverters in parallel create a NOR function.



6. A/D and D/A Converters

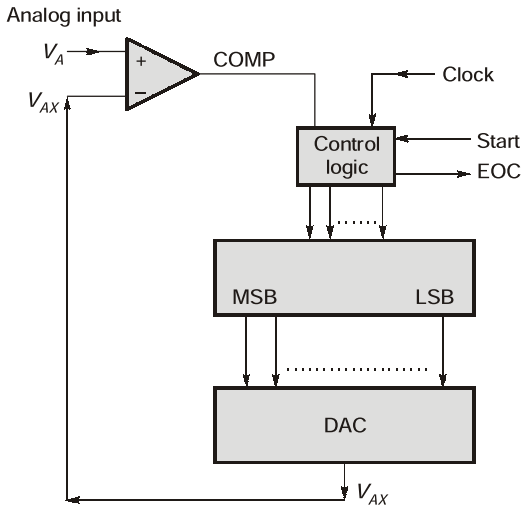
Q.31 Explain with diagram the principle of operation of an A/D converter based on successive approximation method". How it is better that A/D converter based on counter type?

[12 marks : 2003]

Solution:

The successive approximation converter is one of the most widely used types of ADC. It has more complex circuitery than the digital ramp ADC but a much shorter conversion time.

In addition SACs have a fixed value of conversio time that is not dependent on the value of the analog input. Simplified block diagram is shown above. The control logic modifies the content of register bit by bit until the register data are the digital equivalent of the analog input V_A within the resolution of converter.



Let us explain this by considering a four bit SACs.

Let analog input is 1.04 V.

DAC's step size is 1 V.

The operation begin with clearing all the register bits i.e

$$Q_3 = Q_2 = Q_1 = Q_0 = 0$$

or $$[Q] = 0000$$

This makes the DAC output

$V_{AX} = 0$ V with $V_{AX} < V_A$ the comperator output is high.

At the next step control logic sets the MSB of the register to 1 so that $[Q] = 1000$ this produces $V_{AX} = 8$ V because $V_{AX} < V_A$ the COMP output is still high. This high tells the control logic that the setting of MSB did not make V_{AX} to exceed V_A so that MSB is kept at 1.

The control logic now proceeds to next lower bit Q_2. It sets Q_2 to 1 to produce $[Q] = 1100 = 12$ V, because $V_{AX} > V_A$. The COMP output goes low. This low signal tell the control logic that value of V_{AX} is too large and control logic then clear Q_2. So register content back to 1000.

The control logic sets the next lower bit Q_1 so that $[Q] = 1010$ and $V_{AX} = 10$ V, with $V_{AX} < V_A$ COMP is high and tells the control logic to keep Q_1 at 1.

In final step where the control logic sets the next lower bit Q_0 so that $[Q] = 1011 = 11$ V because $V_{AX} > V_A$, COMP goes low to signal that V_{AX} is too large and the control logic clear Q_0 back to 0.

At this point, all the register bits have been processed, the conversion is complete and control logic activates its EOC output to signal that digital equivalent of V_A is now in the register i.e. 1010.

It is better than counter type ADC in the sense that average conversion time is much less than that of counter type ADC.

■■■■

3 Microprocessors

Revised Syllabus of ESE: *Microprocessor basics- interfaces and applications.*

1. Introduction to 8085 and Its Functional Organization

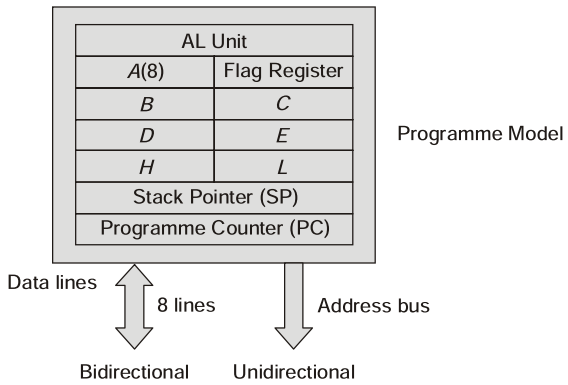
Q.1 Draw the programming model of an Intel 8085 microprocessor and explain its different parts. Explain why address bus is time multiplexed? Explain also why 'ALE' signal is used? How the microprocessor communicates with a slow speed peripherals with the help the 'Ready ' signal?

[18 marks : 2003]

Solution:

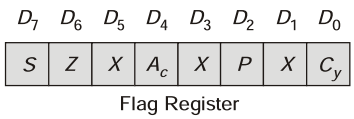
The program model of 8085:

ALU (Arithmetic and Logic Unit): It is logical unit which can perform arithmetic and logical operation. It includes accumulator, temporary register AL unit and stage register.



Flag register → It is also '8 bit register'.

5 bits used as flag



Remaining general register (*B*, *C*, *D*, *E*, *H* and *L*) above 8 bit register. Can also used as register pair.

1. PSW – Programme status word – AF
2. B – BC
3. D – DE
4. H – HL

Programme Counter: (PC) It stores the address of the next instruction to be executed.

Stack Pointer (SP):

It stores address of the top of the stack.

For a 8085, ($AD_0 - AD_7$) lines are multiplexed and the lower half of address ($A_0 - A_7$) is available only during (T_1) of the machine cycle. This lower half of address is also necessary during T_2 and T_3 of machine cycle to

access specific location in memory of I/O port. This means that the lower half of an address bus must be latched in T_1 on the machine cycle. So that it is available throughout the machine cycle. The latching of lower half of an address is done using external latch and ALE signal from 8085.
In some application, speed of input/output system is not compatible with the microprocessor timing. This means that it takes longer time to read/write data. In such situation, the microprocessor has to confirm whether a peripheral is ready to transfer data or not. If the 'Ready' pin is high, the peripheral is ready otherwise 8085 enters WAIT STATE.

Q.2 In 8085 microprocessor, how many interrupts are maskable?
(a) Two (b) Three
(c) Four (d) Five [2 marks : 2004]

Solution: (c)
In 8085 microprocessor, four interrupts are maskable (RST 7.5, RST 6.5, RST 5.5 and INTR)

Q.3 What is function of signals at pin marked $IO/\overline{M}$ in 8085 microprocessor? [4 marks : 2004]

Solution:
Signal at pin $IO/\overline{M}$ is used to select, I/O devices or memory for data transfer.
If signal at this pin is low, data transfer takes place between mp and memory.
If signal at this pin is high, data transfer takes place between mp and I/O devices.

Q.4 Which signal of 8085 microprocessor is used to insert wait states?
(a) Ready (b) ALE
(c) HOLD (d) INTR [2 marks : 2007]

Solution:
'READY' is used by the microprocessor to sense whether a pheripheral device is ready for data transfer or not. If not the processor waits, for synchronize with (slow) pheripherals.

Q.5 Explain steps followed by microprocessor, when there is an interrupt signal applied at INTR pin.
[10 marks : 2008]

Solution:
INTR is a maskable interrupt but not a vector interrupt. It has the lowest priority. The following sequence of events occur when INTR signal goes high.

1. 8085 checks the status of INTR signal during execution of each instruction.
2. If INTR signal is high, the 8085 completes its current instruction and sends an active low interrupts acknowledge signal $(\overline{INTA})$ if the interrupts is enabled, and disables the interrupt enable flip-flop.
3. In response to the $(\overline{INTA})$ signal, internal logic places an instruction OPCODE on the data bus. In the case multibyte instruction additional interrupt acknowledge machine cycles are generated by the 8085 to transfer the additional bytes into the microprocessor.
4. On receiving the instruction, the 8085 serves the address of next instruction on stack, executes received instruction. (This is done after serving the interrupt subroutine).

Q.6 In microprocessor-based systems, DMA facility is required to
(a) increase the speed of data transfer between the microprocessor and the I/O devices.
(b) increase the speed of data transfer between the microprocessor and the memory.
(c) increase the speed of data transfer between the memory and the I/O devices.
(d) improve the reliability of the system.
[2 marks : 2009]

Solution: (c)

The DMA data transfer will be useful to transfer large amount of data between memory and I/O device in a short time.

Q.7 In 8085 microprocessor, there are 3 sets of communication lines, called buses. Which are they? Explain each of them in brief.

[12 marks : 2009]

Solution:

In 8085 consist of 3 buses which are:

Address Bus: The address bus of 8085 consists of 16 parallel signal lines. On these lines the CPU sends out the address of the memory location that is to be written to or read from. If the CPU has N address lines, then it can directly address 2^N memory locations. When CPU reads data from or writes data to a port, it sends the port address out on the address bus.

Data Bus: In 8085 data bus consists of 8 parallel signal lines which are bidirectional. This means that the CPU can read data in from memory or from a port on these lines, or it can send data out to memory or to a port on these lines. Many devices in a system will have their outputs connected to the data bus, but only one device at a time will have its output enabled.

Control Bus: The CPU sends out signals on the control bus to enable the outputs of addressed memory devices or port devices. To read the byte of data from a memory location, the CPU sends out the memory address of the desired byte on the address bus and then sends out a memory read signal on the control bus. The memory read signal enables the address memory device to output a data word into the data bus. The data word from memory travels along the data bus to the CPU.

2. Microprocessor Interfacing

Q.8 In a 8085 microprocessor based system, the maximum number of memory and I/O devices that can be addressed to

(a) 2^8 (b) 2^{16}

(c) $2^8 + 2^{16}$ (d) infinite

[2 marks : 2002]

Solution: (c)

In 8085 microprocessor, we are using 8 bit address for input/output (I/O) devices and 16 bit address for memory. So the maximum number of I/O devices and memory is $(2^8 + 2^{16})$.

Q.9 Explain Memory mapped I/O. [15 marks : 2011]

Solution:

Memory Mapped I/P:

- In this type of input, the MPU uses 16 address lines to identity an input device, an ±10 is connected as if it is a memory register. This is knows as memory mapped input.
- MPU used same control signal (memory read or memory write) and instructions as those of memory.
- In some microprocessors as the motorola 6800, all input have 16 bit address, inputs and memory share the same memory map (64 K)
- In memory mapped MPU follows the same steps as if it is accessing a memory register.
- To transfer data between MPU and input devices, memory related instructions (such as LDA, STA, MOV m, LDAX an STAX) and memory control signals ($\overline{MEMR}$ and $\overline{MEMW}$) are used.
- The µp communicate with an input devices as if it were one of the memory location.
- More hardware needed decode 16 bit address.
- Arithmetic or logical operations can be directly performed with input data.

4 Communication Systems

Revised Syllabus of ESE: *Analog communication basics, Modulation and demodulation, noise and bandwidth, transmitters and receivers, signal to noise ratio, digital communication basics, sampling, quantizing, coding, frequency and time domain multiplexing, power line carrier communication systems.*

1. Introduction to Communication System

Q.1 The signal to noise ratio of one communication link is 60 dB. If three such identical links are used in tandem the overall signal to noise ratio will be

(a) 180 dB (b) 64.77 dB

(c) 55.23 dB (d) 20 dB

[4 marks : 2009]

Solution: (c)

(S/N) for one common link is = 60 dB

i.e. $$10\log_{10}\frac{S}{N} = 60$$

$$\frac{S}{N} = 10^6$$

$$S = 10^6 N$$

Let noise power added in one communication channel is P.

$\therefore$ $$S = 10^6 P$$

$\therefore$ Signal power will be constant through out the link (i.e. through three common links) if there is no attenuation provided by link.

But noise gets added every time it passes through link.

$\therefore$ Total noise power, $P_t = P + P + P = 3P$

$$\left(\frac{S}{N}\right)_{dB} = 10\log_{10}\frac{S}{P_t}$$

$$= 10\log_{10}\frac{10^6 P}{3P} = 60 - 10\log_{10} 3$$

$$= 55.23 \text{ dB}$$

So option (c) is correct.

5 Control Systems

Revised Syllabus of ESE: *Principles of feedback, transfer function, block diagrams and signal flow graphs, steady-state errors, transforms and their applications; Routh-hurwitz criterion, Nyquist techniques, Bode plots, root loci, lag, lead and lead-lag compensation, stability analysis, transient and frequency response analysis, state space model, state transition matrix, controllability and observability, linear state variable feedback, PID and industrial controllers.*

1. Modelling of a Control System and Transfer Function Approach

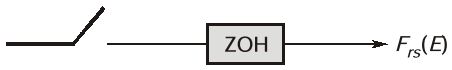
Q.1 Describe a zero-order sample and hold circuit. Obtain the Laplace transform of the output of S/H circuit when discrete inputs are sampled at regular intervals of *T* seconds.

[8 marks : 2001]

Solution:

Sampling Process:

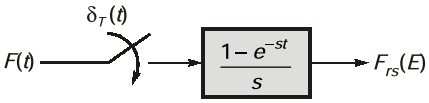
The sampling process is process in which a continuous signal into a sequence of pulses where in the magnitude of the pulse gives the value of the input signal at the instant of sampling.

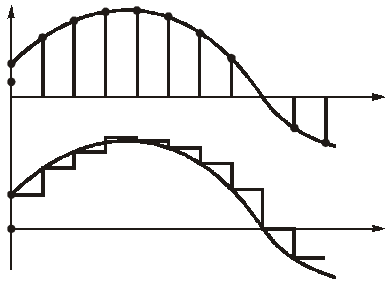


Pulse sampler with ZOH

Where (ZOH) zero order hold is a hold circuit in which the signal is reconstructed such that the value of reconstructed signal for a sampling period is same as the value of last received sample.

Consider a pulse sampler with zero-order hold (ZOH). Let the output of sampler be a pulse train width Δ. For each pulse, the ZOH produces a pulse direction *T*.





As the output of ZOH is a unit step function appearing into *T*.

$$h(t) = u(t) - u(t-T)$$

$$H(s) = \frac{1}{s}(1 - e^{-st})$$

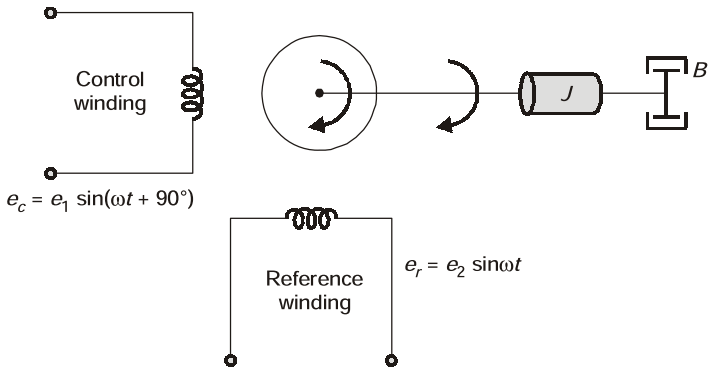
$$\text{Transfer function of (ZOH)} = \frac{L\{\text{Output of ZOH}\}}{L\{\text{Input of ZOH}\}} = \frac{\frac{1}{s} - \frac{1}{s}e^{-st}}{1} = \frac{1-e^{-st}}{s}$$

Hence the pulse sampler with ZOH can be replaced by an equivalent system consisting of an impulse sampler and a block with transfer function $\left[\left(\frac{1-e^{-sT}}{s}\right)\right]$.

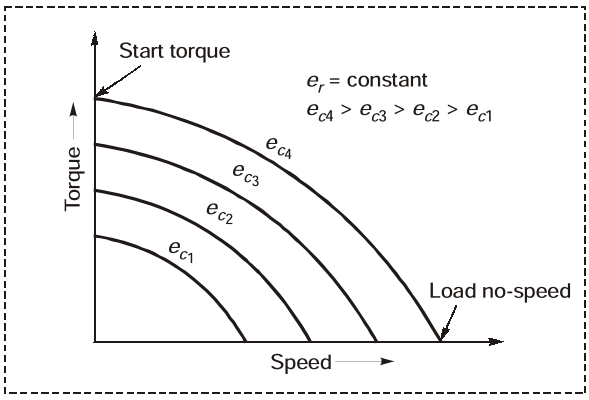
Q.2 Briefly describe the working of a two-phase servomotor. Derive its transfer function and sketch its torque-speed characteristics.

[12 marks : 2003]

Solution:



- An a.c. servomotor is basically a two-phase induction motor. The rotor is the servomotoris built with high resistance so that is X/R ratio is small and the torque-speed characteristic is nearly linear.
- The rotor construction is usually squirrel cage or drag-up type.



- The two-phase servomotor has 2 windage at right angles to each other and the two windings are supplied with voltages with 90° phase difference through a capacitor.
- One winding called reference winding is supplied with a fixed voltage and frequency from a constant voltage source. To the other winding is applied the voltage whose amplitude can be varied but of the same frequency. The axes of the coil are in space and phase quadrature and voltages in time quadrature. On account of this there will be a resultant flux. This resultant flux will be rotating at the frequency of supply at the synchronous speed, $\frac{120f}{p}$. This rotating flux cuts the conducting bars of rotor and causes a varying current. This varying current in turn produces a varying flux and reacts with the stator flux causing the rotor to rotate in a smooth manner.

Transfer Function of the Servomotor:

- Torque developed by motor

$$T_m = K_1 e_c - K_2 \frac{d\theta}{dt}$$

Load torque, $$T_l = J\frac{d^2\theta}{dt^2} + B\frac{d\theta}{dt}$$

- At equilibrium the motor torque is equal to the load torque.

$$T_l = T_m$$

$$\Rightarrow \quad J\frac{d^2\theta}{dt^2} + B\frac{d\theta}{dt} = K_1 e_c - K_2 \frac{d\theta}{dt}$$

- On taking Laplace transform of the above equation, assuming zero initial conditions,

$$Js^2\,\theta(s) + Bs\,\theta(s) = K_1\,E_c(s) - K_2 s\,\theta(s)$$

$$\Rightarrow \quad [Js^2 + Bs + K_2 s]\,\theta(s) = K_1\,E_c(s)$$

$$\text{Transfer function} = \frac{\theta(s)}{E_c(s)} = \frac{K_1}{s(Js + B + K_2)}$$

$$= \frac{K_1/(B+K_2)}{s\left(\frac{J}{K_2+B}s + 1\right)} = \frac{K_m}{s(\tau_m s + 1)}$$

where, $$K_m = \frac{K_1}{B+K_2} = \text{motor gain constant}$$

$$\tau_m = \frac{J}{K_2+B} = \text{motor time constant}$$

Q.3 Why is it necessary to truncate a Taylor series expansion of a non-linear function after the first term, if the linear approximation is desired?

[10 marks : 2004]

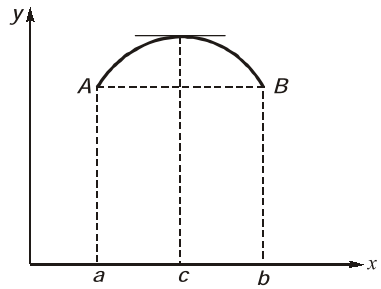
Solution:

A Taylor series expansion is given by

$$f(x) = f(a) + (x-a)\,f'(a) + \frac{(x-a)^2}{2!}f''(a) + \frac{(x-a)^3}{3!}f'''(a) + \ldots\ldots\ldots$$

Its curve may be drawn as

Taylor's series expresses the height of a curve at a distance at $a + h$ form the origin in terms of its height at a distance a from the origin.



Another method of writing Taylor's series is by writing the series in terms of 'h' rather than 'x'.

$x = a + n$ or $h = x - a$. Substituting for x in equation (i) gives,

$$f(a+h) = f(a) + h\,f'(a) + \frac{h^2}{2!}f''(a) + \frac{h^3}{3!}f'''(a) + \ldots\ldots\ldots$$

If h is considered a small increase in the non-linearity, the higher orders may be neglected as being very small.

Q.4 Draw a neat sketch of a hydraulic proportional controller and explain its working.

[10 marks : 2006]

Solution:

Hydraulic actuator:

Hydraulic actuator shown in Fig. (1) controls large displacement power at the shaft of main piston. The input power requirement is very small and provided by the displacement of the valve piston. The linear motion of the valve piston controls the flow of oil either side of the main piston.

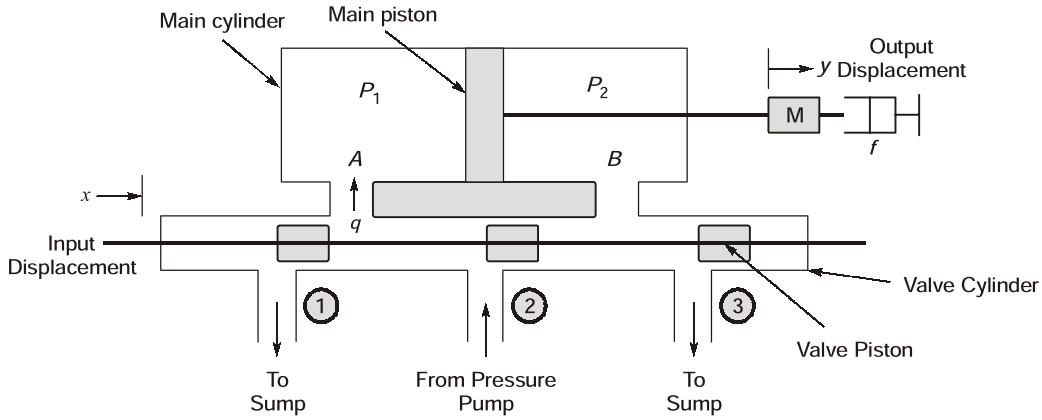


Fig. (1) : Hydraulic actuator

When the input force through the displacement x is applied to the valve piston, the valve piston moves to the right. Piston valve ports (2) and (3) are thus uncovered and oil higher pressure from port (2) enters to the left side of the main piston through main port A. At the same time the main port B is connected to the sump through port (3). The pressure P_1 on the left side of the main piston is higher than the pressure P_2 on the right side of the piston. The pressure difference $(P_1 - P_2)$ causes the main piston to move from left to right and the resulting displacement of the mass attached to main piston is y.

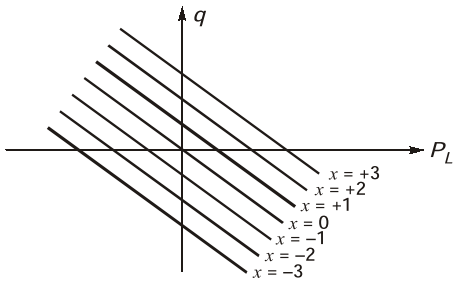


Fig. (2) : Linearized performance characteristics of hydraulic actuator

The mathematical relation between the input displacement x and the output displacement y gives the model of the system.

The linearized performance characteristics of hydraulic actuator relating the oil flow q (m^3/sec) and the pressure difference $(P_1 - P_2) = P_L$ (N/m^2) acting on the main piston as a function of valve displacement x is shown in Fig. (2).

6 Electrical Machines

Revised Syllabus of ESE: *Single phase transformers, three phase transformers - connections, parallel operation, auto-transformer, energy conversion principles, DC machines-types, windings, generator characteristics, armature reaction and commutation, starting and speed control of motors, Induction motors - principles, types, performance characteristics, starting and speed control, Synchronous machines - performance, regulation, parallel operation of generators, motor starting, characteristics and applications, servo and stepper motors.*

1. Magnetic Circuits & Electromechanical Energy Conversion Systems

Q.1 The hysteresis and eddy-current loss of 1-phase transformer working on 200 V, 50 Hz are P_h and P_e respectively. The percentage decrease in these losses when operated on a 160 V, 40 Hz supply would respectively be

(a) 32, 36 (b) 20, 36

(c) 25, 50 (d) 40, 80

[2 marks : 2001]

Solution:

Option (b) is correct.

Since $V/f \propto B_{mf}$ and hysteresis loss is $P_h = k_h f B_m^x$

then % decrease in hysteresis loss

$$= \frac{P_{h_1} - P_{h_2}}{P_{h_1}} \times 100 = \frac{f_2 \cdot B_{m_2}^x - f_1 B_{m_1}^x}{f_1 B_{m_1}^x} \times 100$$

$$= \left[1 - \frac{f_2}{f_1}\left(\frac{V_2}{V_1} \cdot \frac{f_1}{f_2}\right)^x\right] \times 100 = \left[1 - \frac{40}{50}\left(\frac{160}{200} \cdot \frac{50}{40}\right)^x\right] \times 100 = 20\%$$

Eddy current loss $= k_e f^2 B_m^2$

% decrease in eddy current loss

$$= \frac{P_{e_1} - P_{e_2}}{P_{e_2}} \times 100 = \left[1 - \left(\frac{f_2}{f_1}\right)^2 \cdot \left(\frac{V_2}{V_1} \cdot \frac{f_1}{f_2}\right)^2\right] \times 100$$

$$= \left[1 - \left(\frac{40}{50}\right)^2 \cdot \left(\frac{160}{200} \cdot \frac{50}{40}\right)^2\right] \times 100 = 36\%$$

Q.2 In a transformer core, third and fifth harmonic components of fluxes are respectively 10% and 4% of the fundamental flux. The third and fifth harmonic induced emfs in the winding, in terms of the fundamental induced emf are respectively.

(a) 30%, 20% (b) 10%, 12%
(c) 50%, 20% (d) 50%, 20%

[2 marks : 2001]

Solution:

$$E \propto f\phi$$

Option (d) is correct.

Q.3 What are the terms air-gap power, internal mechanical power developed and shaft power? How are these terms related with each other?

[4 marks : 2001]

Solution:

Air gap power (P_g): The power that is transfered from the stator to the rotor via the air-gap magnetic field, is known as the Air-gap power (P_g)

$$P_g = \frac{3I_2'^2 R_2'}{s}$$

Subtracting the rotor copper loss from Air-gap power (P_g) gives the internal mechanical power developed (P_m)

$$P_m = P_g - 3I_2'^2 R_2'^2 = \frac{3I_2'^2 R_2'^2}{s} - 3I_2'^2 R_2$$

$$= 3I_2'^2 R_2'\left(\frac{1}{s} - 1\right) = (1-s)P_g$$

The internal mechanical power developed (P_m) is three times the electrical power absorbed in resistance $R_2'\left(\frac{1}{s} - 1\right)$.

Shaft power (P_{sh}) is the power available at shaft after subtracting mechanical losses from P_m.

$$P_{sh} = P_m - \text{mechanical losses}$$

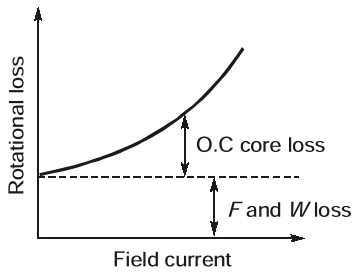
Q.4 What are the no-load rotational losses in electrical machines? How can these be determined?

[7 marks : 2001]

Solution:

The mechanical loss and open circuit core loss combined together are caused by rotor rotation. Their sum is called as no-load rotational losses.

Mechanical Loss: This loss consists of bearing friction, brush friction and windage losses. The windage or wind friction loss includes the power required to circulate air through the machine and ventilating ducts and is approximately proportional to square of the speed.



Open Circuit Core Loss: Consists of hysteresis and eddy current losses. These losses occur in case of stator and rorot carrying an alternating flux.

$$\text{Hysteresis loss } P_h = K_h f B_m^x$$

$$\text{Eddy current loss } P_e = K_e f^2 B_m^2$$

No load rotational losses can be determined by running the electrical machine as an unloaded motor at the rotor speed and with armature voltage equal to the normal generator emf. The total power input to the unloaded motor minus the no-load armature ohmic loss gives the magnitude of no-load rotational loss.

Q.5 Which of the losses in rotating electrical machines are influenced by the magnitude of the flux, the load and square of the load?
Write a general expression for all the losses occurring in rotating electrical machines and prove that maximum efficiency occurs when losses proportional to square of current = constant losses.

[7 marks : 2001]

Solution:

(a) **Constant or Fixed Losses:** These losses are influenced by the magnitude of the flux. Under this no-load core loss, friction and windage loss.

(b) **Loss Proportional to Load Current:** Brush-contact loss occurs when current is to be conducted to, or from, the rotating part of the electrical machine through sliding contacts.

(c) **Losses Proportional to the Square of Load Current:** Resistance loss in various machine winding and stray load loss are proportional to the square of load current.

losses in rotating electrical machine may be written as $a + bI + cI^2$ and output or input as AVI where,

a = constant losses
bI = loss proportional to load current
A = Constant ($\sqrt{3}$ × pf for 3-phase machines, pf for single phase machines and unity for d.c. machines)
V = machine voltage

Motor operation: Power input = AVI

$$\therefore \quad \text{Efficiency,} \qquad \eta = \frac{AVI - a - bI - cI^2}{AVI}$$

For constant voltage V,

$$\frac{d\eta}{dI} = \frac{(AV - b - 2cI)(AVI) - (AVI - a - bI - cI^2)(AV)}{(AVI)^2}$$

For efficiency to be maximum, $d\eta/dI$ must be equal to zero.

$$\therefore \quad (AV - b - 2cI)(AVI) = (AVI - a - bI - cI^2)(AV)$$

$$\therefore \quad a = cI^2$$

Generator operation: Power output = AVI

$$\therefore \quad \text{Efficiency,} \qquad \eta = \frac{AVI}{AVI + a + bI + cI^2}$$

For constant V,

$$\frac{d\eta}{dI} = \frac{(AV)(AVI + a + bI + cI^2) - (AVI)(AV + b + 2cI)}{(AVI + a + bI + cI^2)^2}$$

For maximum efficiency,

$$\frac{d\eta}{dI} = 0$$

$$\therefore \quad cI^2 = a$$

[Losses proportional to square of current = constant losses].

Q.6 The worst type of load on a supply system is

(a) rolling mill load (b) pumping load
(c) motors in paper mill (d) arc furnace load

[2 marks : 2002]

Ans. (d)

Option (d) is correct.

Q.79 A 220 V, 7 hp dc series motor is mechanically coupled to a fan. It draws 25 A and runs at 300 rpm when connected to rated supply. The torque required by the fan is proportional to the square of the speed. The resistance of armature and field windings are 0.6 Ω and 0.4 Ω, respectively. Neglect armature reaction and rotational loss:

(i) Determine the power delivered to the fan and the torque developed by the machine.

(ii) The speed is to be reduced to 200 rpm by inserting a resistance R_s in the armature circuit. Determine the value of this resistance and the power delivered to the fan.

[10 marks : 2016]

Solution:

(i) $V = 220,$

$R_a = 0.6\ \Omega,$

$R_{se} = 0.4\ \Omega,$

$I_a = 25\ \text{A}$

$E_b = V - I_a(R_a + R_{se})$

$= 220 - 25\ (0.6 + 0.4)$

$\therefore \quad E_b = 195$ volts

Power developed $= E_b I_a = 195 \times 25 = 4875$ W

$\because$ No rotational loss $\rightarrow$ Power developed = delivered

$$\text{Torque developed} = T = \frac{60}{2\pi N}P$$

$$\therefore \quad T = \frac{60}{2\pi(300)}4875 = 155.25 \text{ N-m}$$

(ii) Given: $T \propto N^2$

speed reduced to 200 rpm

$$\therefore \quad \frac{T_2}{T_1} = \left(\frac{N_2}{N_1}\right)^2$$

Series motor:

$$\therefore \quad T \propto I_a^2$$

$$\therefore \quad \left(\frac{I_{a2}}{I_{a1}}\right)^2 = \left(\frac{N_2}{N_1}\right)^2 \Rightarrow I_{a2}^2 = \left(\frac{N_2}{N_1}\right)^2 I_{a1}^2$$

$$\therefore \quad I_{a2}^2 = \left(\frac{200}{300}\right)^2 (25)^2 = 16.67 \text{ A}$$

$$\frac{N_2}{N_1} = \frac{E_{b2}}{E_{b1}} \times \frac{\phi_1}{\phi_2} \Rightarrow \frac{N_2}{N_1} = \frac{E_{b2}}{E_{b1}} \times \frac{I_{a1}}{I_{a2}}$$

$$\therefore \quad \frac{200}{300} = \frac{E_{b2}}{195} \times \frac{25}{16.67}$$

$$\therefore \quad E_{b2} = 86.684 \text{ volts}$$

$$E_{b2} = V - I_{a2}(R_a + R_{se} + R_{ext})$$

$$\therefore \quad 86.684 = 220 - 16.67\ (0.6 + 0.4 + R_{ext})$$

$$\therefore \quad R_{ext} = 7\ \Omega$$

$$\therefore \quad \text{Power delivered} = E_{b2} \cdot I_{a2}$$

$$= 86.684 \times 16.67 = 1445 \text{ Watts}$$

Q.80 A shunt motor is connected to a constant d.c. voltage source and it drives a constant load torque.

Determine the effect of back emf E_a on speed as a function of flux, when $E_a < \frac{V_t}{2}$ and $E_a > \frac{V_t}{2}$.

[20 marks : 2017]

Solution:

We know that,

$$E_b = k\phi\omega_m \quad \text{...(i)}$$

$$E_b = V - I_a R_a \quad \text{...(ii)}$$

$$T = k\phi I_a \quad \text{...(iii)}$$

From equation (i) and (ii),

$$k\phi\omega_m = V - I_a R_a$$

$$\omega_m = \frac{V - I_a R_a}{k\phi}$$

By substituting,

$$I_a = \frac{T}{k\phi} \quad \text{(From equation (iii))}$$

$$\omega_m = \frac{V}{k\phi} - \frac{T R_a}{k^2\phi^2}$$

Differentiating ω_m with respect to ϕ

Case (i):

$$\frac{d\omega_m}{d\phi} > 0$$

$$-\frac{V}{k\phi^2} + \frac{2T R_a}{k^2\phi^3} > 0$$

Again putting,

$$T = k\phi I_a$$

$$-\frac{V}{k\phi^2} + \frac{2I_a R_a}{k\phi^2} > 0$$

$$2I_a R_a > V$$

$$2V - 2E_b > V$$

$$E_b < \frac{V}{2}$$

$\therefore$ when $E_b < \frac{V_t}{2}$ speed of the motor increases with rise in flux.

Case (ii):

$$\frac{d\omega_m}{d\phi} < 0$$

$$-\frac{V}{k\phi^2} + \frac{2T R_a}{k^2\phi^3} < 0$$

Putting,

$$T = k\phi I_a$$

$$-\frac{V}{k\phi^2} + \frac{2I_a R_a}{k\phi^2} < 0$$

$$2I_a R_a < V$$

$$V - E_b < \frac{V}{2}$$

$$E_b > \frac{V}{2}$$

$\therefore$ when $E_b > \frac{V_t}{2}$ speed of the motor decreases with rise in flux.

8 Power Electronics and Drives

Revised Syllabus of ESE: *Semiconductor power diodes, transistors, thyristors, triacs, GTOs, MOSFETs and IGBTs - static characteristics and principles of operation, triggering circuits, phase control rectifiers, bridge converters - fully controlled and half controlled, principles of choppers and inverters, basis concepts of adjustable speed dc and ac drives, DC-DC switched mode converters, DC-AC switched mode converters, resonant converters, high frequency inductors and transformers, power supplies.*

1. Power Semiconductor Devices

Q.1 Describe the turn-off process in a GTO with relevant voltage and current waveforms. Enumerate the advantages and disadvantages of a GTO as compared to a conventional thyristor.

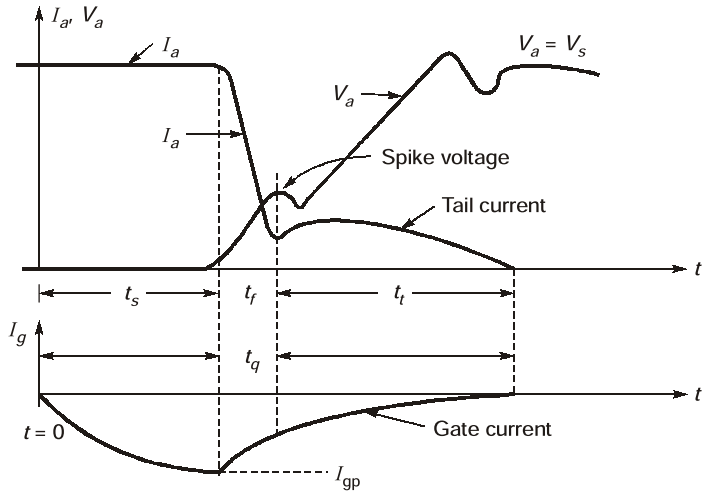
[12 marks : 2001]

Solution:

Before the initiation of turn-off process, a GTO carries a steady current I_a. This figure shows a typical turn-off dynamic characteristic for a GTO. The total turn off time t_q is subdivided into three different periods; namely the storage period (t_s), the fall period (t_f) and the tail period (t_t). In other words,

$$t_q = t_s + t_f + t_t$$

Initiation of turn-off process starts as soon as negative gate current begins to flow after $t = 0$. The rate of rise of this gate current depends upon the gate circuit inductance and the gate voltage applied. During the storage period, anode current I_a and anode voltage (equal to on-state voltage drop) remain constant. Termination of the storage period is indicated by a fall in I_a and rise in V_a.



During t_s, excess charges, i.e. holes in p-base are removed by negative gate current and the centre junction comes out of saturation. In other words, during storage time t_s, the negative gate current rises to a particular value and prepares the GTO for turning-off (or commutation) by flushing out of the stored carriers. After t_s,

anode current begins to fall rapidly and anode voltage starts rising. As shown in figure, the anode current falls to a certain value and then abruptly changes its rate of fall. Interval during which anode current falls rapidly is the fall time t_f, is of the order of 1 μsec. The fall period t_f is measured from the instant gate current is maximum negative to the instant anode current falls to its tail current.

At the time $t = t_s + t_f$, there is a spike in voltage due to abrupt current change. After t_f, anode current I_a and anode voltage V_a keep moving towards their turn-off values for a time t_t called tail time. After t_t, anode current reaches zero value.

A GTO has the following disadvantage as compared to a conventional thyristor:

(i) Magnitude of latching and holding currents is more in a GTO.

(ii) On state voltage drop and the associated loss is more in a GTO.

(iii) Due to the multicathode structure of GTO, triggering gate current is higher than that required for a conventional SCR.

(iv) Gate drive circuit losses are more

(v) Its reverse-voltage blocking capability is less than its forward-voltage blocking capability. But this is no disadvantage so far as inverter circuits are concerned.

Inspite of all these demerits, GTO has the following advantages over an SCR:

(i) GTO has faster switching speed.

(ii) Its surge current capability is comparable with an-SCR.

(iii) It has more *di*/*dt* rating at turn-on.

(iv) GTO circuit configuration has lower size and weight as compared to SCR circuit unit.

(v) GTO unit has higher efficiency because an increase gate-drive power loss and on-state loss is more than compensated by the elimination of forced commutation losses.

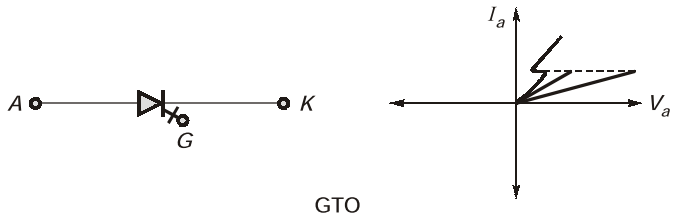
(vi) GTO unit has reduced acoustical electromagnetic noise due to elimination of commutation chokes.

Q.2 What is a GTO? Discuss its advantages over a normal thyristor. Discuss the advantage of a GTO over bipolar transistor in low power applications.

[8 marks : 2003]

Solution:

GTO is pnpn device, can be turned on like an ordinary thyristor by a pulse of positive gate current, but it can be turned off easily by a negative gate pulse of appropriate amplitude.



GTO

1. GTO has faster switching speed.
2. Its surge current capability is comparable with an SCR.
3. It has more di/dt rating at turn-on.
4. GTO unit has higher efficiency due to the elimination of forced commutation losses.
5. GTO has reduced acoustical and electromagnetic noise due to elimination of commutation chokes.
6. GTO circuit configuration has lower size and weight as compared to thyristor circuit unit.

- In BJT switching, lateral current flow is the basic limiting factor in BJT performance. It causes lateral voltage drop which leads to emitter current crowding, which causes decrease in current gain. Excessive curernt crowding causes second breakdown and destruction of the device.

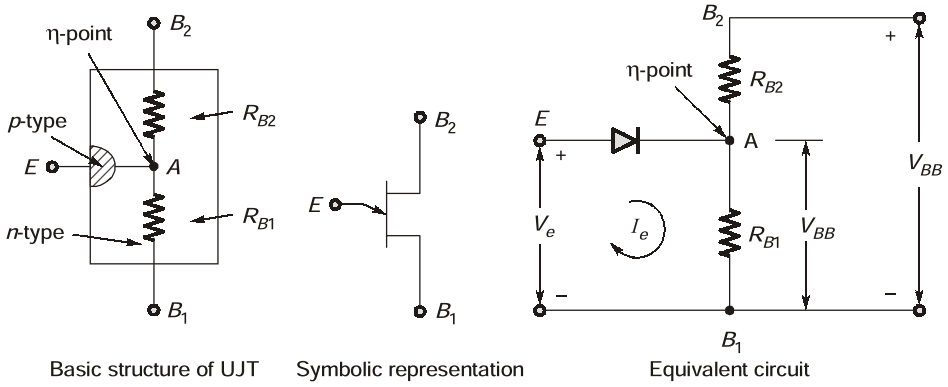
- Turning off of BJT should be done in a controlled manner of negative base current to avoid excessive stored charge which may cause long turn off time and large power dissipation. These problems are avoided in a GTO in low power applications.

Q.3 What is an Unijunction transistor? Draw a basic UJT pulse trigger circuit with typical waveforms and explain its operation.

[8 marks : 2003]

Solution:

An UJT is made up of an n-type silicon (si) base to which p-type emitter is embedded. It has three terminals the emitter (E), base one B_1 and base two B_2 between bases B_1 and B_2, the Unijunction behave like ordinary resistance.



Basic structure of UJT | Symbolic representation | Equivalent circuit

In figure (a), when source voltage V_{BB} is applied, capacitor C begins to charge through R exponentially towards V_{BB}. During this charging, emitter circuit of UJT is an open circuit.

The capacitor voltage v_c, equal to emitter voltage v_e, is given by

$$v_C = v_e = V_{BB}\,(1 - e^{-t/RC})$$

The time constant of the charge circuit is $\tau_1 = RC$.

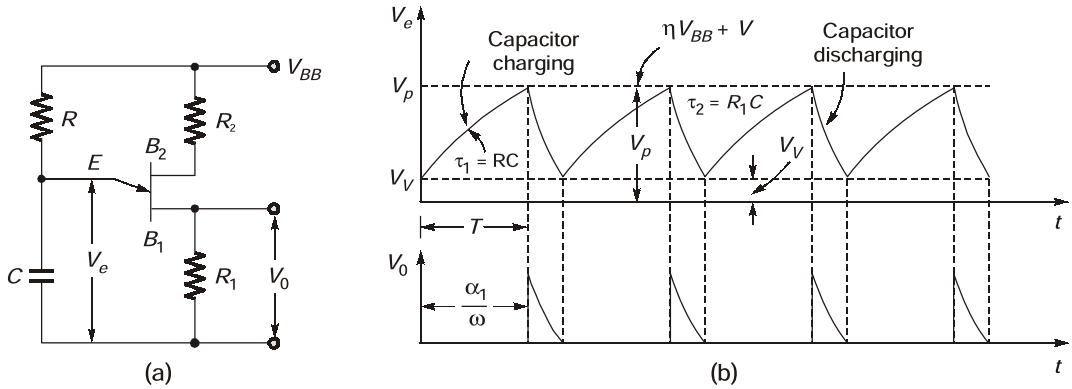


Fig. (2) UJT oscillator (a) Connection diagram and (b) Voltage waveforms

When this emitter voltage v_e (or v_c) reaches the peak-point voltage V_p ($= \eta\ V_{BB} + V_D$), the Unijunction between $E - B_1$ breaks down. As a result, UJT turns on and capacitor C rapidly discharge through low resistance R_1 with a time constant $\tau_2 = R_1\,C$. Here τ_2 is much smaller than τ_1. When the emitter voltage decays to the valley-point voltage V_v, UJT turns off. The time T required for capacitor C to charge from initial voltage V_v to peak-point voltage V_p, through large resistance R, can be obtained as under:

$$V_p = \eta\ V_{BB} + V_D = V_v + V_{BB}(1 - e^{-t/RC})$$

Assuming, $V_D = V_v$, $\eta = (1 - e^{-t/RC})$

$$T = \frac{1}{f} = RC \ln\left(\frac{1}{1-\eta}\right)$$

In case T is taken as the time period of output pulse duration (neglecting small discharge time), then the value of firing angle α_1 is given by

$$\alpha_1 = \omega T = \omega RC \ln \frac{1}{1-\eta}$$

where 'ω' is the angular frequency of UJT oscillator.

Q.4 If the turn-on time of a SCR is 7-micro sec., an ideal gate trigger pulse should have
(a) short rise-time and pulse width of 8 μsec.
(b) short rise-time and pulse width of 4 μsec.
(c) high rise-time with pulse width of 4 μsec.
(d) high rise-time with pulse width of 8 μsec.

[2 marks : 2004]

Solution: (a)

An ideal gate trigger should have short rise time and pulse width of should be greater than turn on time of a SCR.

Q.5 Two thyristors *A* and *B* have rated gate-current of 100 mA and 2 A respectively
(a) *B* is GTO and *A* is conventional SCR.
(b) *A* is GTO and *B* is conventional SCR.
(c) Thyristor *A* may operate as transistor.
(d) None of the above

[2 marks : 2004]

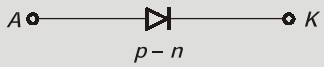
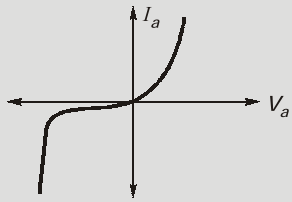
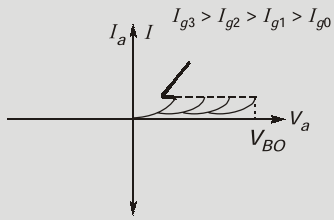
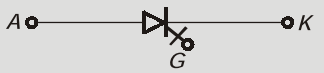
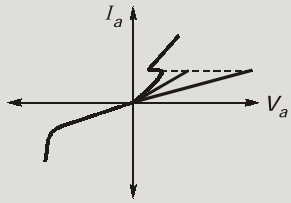
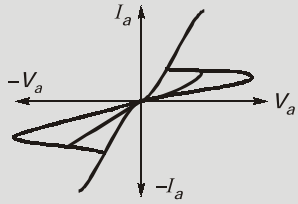
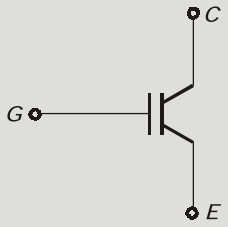
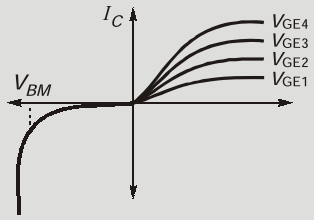
Solution: (a)

Due to multi cathode structure of GTO, triggering gate current is higher than that required for a conventional SCR.

Q.6 Draw the symbols and characteristics of the following devices:
(i) Diode, (ii) Thyristor,
(iii) GTO, (iv) Triac and
(v) IGBT

[10 marks : 2005]

Solution:

Device	Symbol	Characteristics
(i) Diode		
(ii) Thyristor		
(iii) GTO		
(iv) Triac		
(v) IGBT		

Q.7 In ac applications, a different of harmonics is needed. The total harmonic ratio (THR) is given by:

(a) $\sqrt{\dfrac{f_{rms}^2 - f_{1\,rms}^2}{f_{rms}}}$ (b) $\sqrt{\dfrac{f_{rms}^2 - f_{1\,rms}^2}{f_{1\,rms}^2}}$

(c) $\sqrt{\dfrac{f_{1\,rms}^2 - f_{rms}}{f_{rms}}}$ (d) $\sqrt{\dfrac{f_{1\,rms}^2 - f_{rms}}{f_{1\,rms}}}$

[2 marks : 2006]

Solution: (b)

$$\text{Total harmonic distortion} = \sqrt{\left(\frac{f_{(rms)\,\text{harmonic}}}{f_{1\,(rms)}}\right)^2 - 1}$$