CLASS TEST

S.No.: 01DLSK_CS_ABCDEFGH_17926

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DIGITAL LOGIC

COMPUTER SCIENCE & IT

Date of Test : 17/09/2026

ANSWER KEY

1.	(d)	7.	(c)	13.	(a)	19.	(a)	25.	(d)
2.	(d)	8.	(d)	14.	(d)	20.	(b)	26.	(c)
3.	(d)	9.	(b)	15.	(b)	21.	(c)	27.	(d)
4.	(b)	10.	(c)	16.	(c)	22.	(b)	28.	(d)
5.	(a)	11.	(a)	17.	(c)	23.	(b)	29.	(c)
6.	(d)	12.	(a)	18.	(b)	24.	(d)	30.	(a)

DETAILED EXPLANATIONS

1. (d)

$$Q = AB + \left[\overline{(B+C)(BC)}\right]$$

$$= AB + \left[\overline{BC + BC}\right]$$

$$= AB + \overline{BC}$$

$$= AB + \overline{B} + \overline{C}$$

$$Q = A + \overline{B} + \overline{C}$$

2. (d)

A	B	Q
0	0	1
0	1	1
1	0	1
1	1	0

If any one of the input is zero, output is logic '1'. Otherwise output is logic '0', which represents the NAND gate.

3. (d)

Output of ExOR Gate = $b_i \oplus b_{i+1}$

Initially $Q = 0$ assume

So,
After 1 clock, $Z = b_7 \oplus b_0$
After 2 clock, $Z = b_7 \oplus b_6$
After 3 clock, $Z = b_6 \oplus b_5$
After 4 clock, $Z = b_5 \oplus b_4$
After 5 clock, $Z = b_4 \oplus b_3$
After 6 clock, $Z = b_3 \oplus b_2$
After 7 clock, $Z = b_2 \oplus b_1$
After 8 clock, $Z = b_1 \oplus b_0$

Which is same as Binary to gray code converter.

4. (b)

$$Y = A\overline{B} + A \oplus C$$

$$= A\overline{B} + A\overline{C} + \overline{A}C$$

So, SOP $= \Sigma m(1, 3, 4, 5, 6)$

POS $= \Pi M(0, 2, 7)$

5. (a)

Given, $(5456)_8$

$$\begin{array}{cccc} 5 & 4 & 5 & 6 \\ \downarrow & \downarrow & \downarrow & \downarrow \\ 101 & 100 & 101 & 110 \end{array}$$

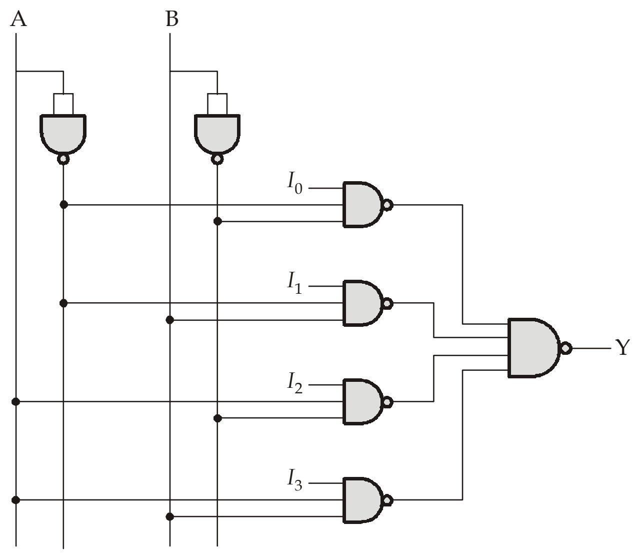
$$(101100101110)_2$$

For Hexadecimal number, grouping 4 binary bits

$$\begin{array}{ccc} 1011 & 0010 & 1110 \\ \downarrow & \downarrow & \downarrow \\ B & 2 & E \end{array}$$

$\therefore$ $(5456)_8 \longrightarrow (B2E)_{16}$

6. (d)



7. (c)

We know that for a stage change to ripple through n stages i.e. $T_C = n \times t_{pd}$.

$$f_c = \frac{1}{T_C}$$

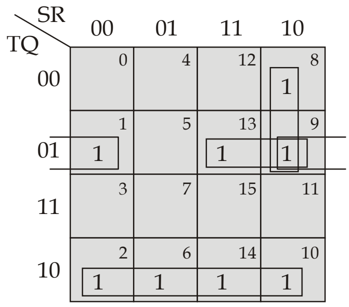
$$f_c = \frac{1}{n \times t_{pd}}$$

So, $$t_{pd} = \frac{1}{n \times f_c}$$

$$t_{pd}(\text{min}) = \frac{1}{10 \times 10 \times 10^6 \text{ Hz}} = 0.01 \times 10^{-6} \text{ sec} = 10 \times 10^{-9} \text{ sec} = 10 \text{ nsec}$$

8. (d)

S	R	T	Q	Q^+
0	0	0	0	0
0	0	0	1	1
0	0	1	0	1
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	1
0	1	1	1	0
1	0	0	0	1
1	0	0	1	1
1	0	1	0	1
1	0	1	1	0
1	1	0	0	0
1	1	0	1	1
1	1	1	0	1
1	1	1	1	0



$$Q^+ = TQ' + T'QS + T'QR' + T'SR' = TQ' + T'[Q(S + R') + SR']$$

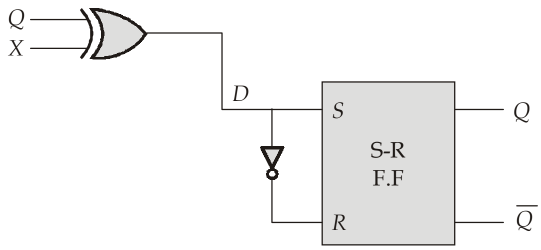
9. (b)

(i) $x > y$

(ii) $x > 6$

$$x = 8, y = 7$$
$$(673)_8 + (54)_8 = (487)_{10}$$
$$(443)_{10} + (44)_{10} = (487)_{10}$$

10. (c)

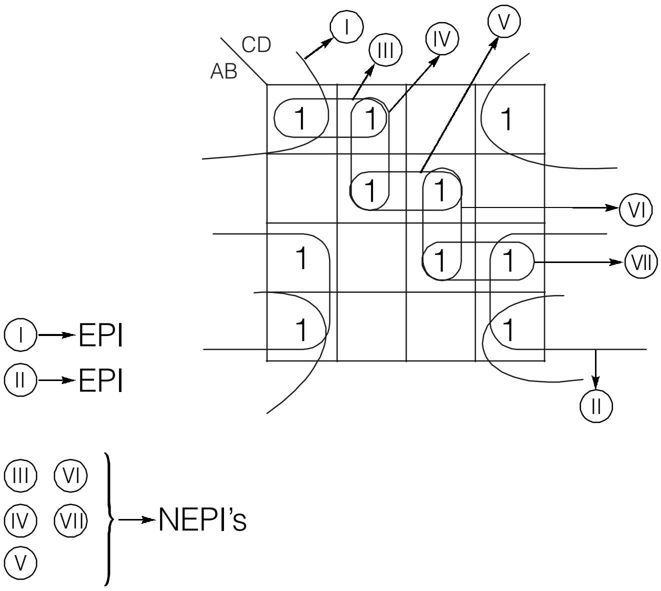


$$Q_{n+1} = D = Q \oplus X$$

For $X = 0$, $Q_{n+1} = Q_n$ and for $X = 1$, $Q_{n+1} = \overline{Q_n}$.

Therefore, the given circuit acts as T flip-flop for $T = X$.

11. (a)



EPI = Essential Prime Implicant [which cover a minterm not covered by any other prime implicants]
NEPI = Non Essential Prime Implicant. Number of EPI's = 2, number of NEPI's = 5.

12. (a)

$$Y = \bar{S}_1\bar{S}_0(I_0) + \bar{S}_1 S_0(I_1) + S_1\bar{S}_0(I_2) + S_1 S_0(I_3)$$

$$I_0 = I_3 = S_1$$

$$I_1 = I_2 = S_0$$

$\Rightarrow$

$$Y = \underbrace{\bar{S}_1\bar{S}_0(S_1)}_{0} + \bar{S}_1 S_0(S_0) + \underbrace{S_1\bar{S}_0(S_0)}_{0} + S_1 S_0(S_1)$$

$$Y = \bar{S}_1 S_0 + S_1 S_0$$

- S_0 = B, S_1 = A

$$Y = \bar{A}B + AB = (\bar{A} + A)B = B$$

- S_0 = A, S_1 = $\bar{B}$

$$Y = \bar{\bar{B}}A + \bar{B}A = BA + \bar{B}A = A(B + \bar{B}) = A$$

- S_0 = $\bar{A}$, S_1 = B

$$Y = \bar{B}\bar{A} + B\bar{A} = \bar{A}(B + \bar{B}) = \bar{A}$$

- S_0 = $\bar{A}$, S_1 = $\bar{B}$

$$Y = \bar{A}\bar{\bar{B}} + \bar{B}\bar{A} = \bar{A}B + \bar{B}\bar{A} = \bar{A}(B + \bar{B}) = \bar{A}$$

Hence option (a) is the correct answer.

13. (a)

For every combination of x, y, z the function value remains same for input $\bar{x}, y, \bar{z}$.

$x\ y\ z$	$f(x,y,z) = f(\bar{x},y,\bar{z})$
0 0 0 1 0 1	either 0 or 1
0 0 1 1 0 0	either 0 or 1
0 1 0 1 1 1	either 0 or 1
0 1 1 1 1 0	either 0 or 1

Effectively there are only four rows for the truth table of the function $f(x, y, z)$.

$\therefore$ Total Boolean expressions possible is $2^4 = 16$.

14. (d)

(a)
$$\begin{aligned}
\overline{(\bar{A}B + \bar{C})}(A+C) &= (A+\bar{B})C \\
(A+\bar{B})\cdot C\cdot(A+C) &= (A+\bar{B})C \\
(AC+\bar{B}C)(A+C) &= (A+\bar{B})C \\
AC + A\bar{B}C + \bar{B}C &= (A+\bar{B})C \\
AC + \bar{B}C &= (A+\bar{B})C \\
(A+\bar{B})C &= (A+\bar{B})C \quad \because \text{ True}
\end{aligned}$$

(b)
$$\begin{aligned}
\overline{(A+\bar{B}+\bar{C})(A+\bar{B}C)} &= \bar{A}(B+\bar{C}) \\
(\bar{A}BC) + \bar{A}(B+\bar{C}) &= \bar{A}B + \bar{A}\bar{C} \\
\bar{A}BC + \bar{A}B + \bar{A}\bar{C} &= \bar{A}B + \bar{A}\bar{C} \\
\bar{A}B(C+1) + \bar{A}\bar{C} &= \bar{A}B + \bar{A}\bar{C} \\
\bar{A}\bar{C} + \bar{A}B &= \bar{A}B + \bar{A}\bar{C} \quad \because \text{ True}
\end{aligned}$$

(c)
$$\begin{aligned}
(A+\bar{A}\bar{B}\bar{C})B + \bar{A}B &= BA + \bar{A}B \\
(A+\bar{B}\bar{C})B + \bar{A}B &= (A+\bar{A})B \\
AB + \bar{A}B &= B \\
B(A+\bar{A}) &= B \\
B &= B \quad \because \text{ True}
\end{aligned}$$

So, all the expression are correct.

15. **(b)**

$$I_1 = Q_1 \oplus Q_0$$
$$I_0 = Q_3 \odot Q_2$$

Clock	Q_3	Q_2	Q_1	Q_0	I_1	I_0	Y_2
	0	0	0	0	0	1	0
1	0	0	0	1	1	1	0
2	0	0	1	0	1	1	0
3	0	0	1	1	0	1	0
4	0	1	0	0	0	0	0
5	0	1	0	1	1	0	1
6	0	1	1	0	1	0	1
7	0	1	1	1	0	0	0
8	1	0	0	0	0	0	0
9	1	0	0	1	1	0	1
10	0	0	0	0	0	1	0

Since, in 10 clock cycle y_2 is 1 for 3 clock cycles.

16. **(c)**

Let the output of XNOR gate is Y

$$Y = (Q_3 \oplus Q_1 \oplus Q_0) \odot Q_5$$

CLK	Y	Q_5	Q_4	Q_3	Q_2	Q_1	Q_0
–		1	0	0	0	0	0
1	0	0	1	0	0	0	0
2	1	1	0	1	0	0	0
3	1	1	1	0	1	0	0
4	0	0	1	1	0	1	0
5	1	1	0	1	1	0	1

Minimum five clock pulses are required to get the sequence 101101

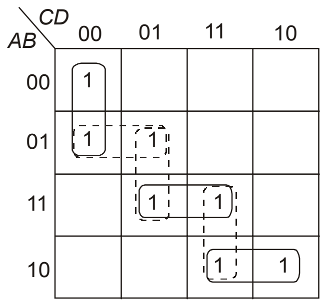
17. **(c)**

For MOD - 10 counter

X = Jhonson counter required = 5 FF's
Y = ring counter required = 10 FF's
Z = ripple counter required = 4 FF's
X + Y + Z = 5 + 10 + 4 = 19 FF's

18. **(b)**

Essential prime implicant is a prime implicant which is having atleast one minterm which is not the part of any other prime implicant.
Using *K*-map for the given function
we get



The total number of prime implicants = 6 and the number of essential prime implicants = 2.

19. (a)

J-K flip-flop will change for every clock pulse. Mod-3 counter will change whenever Q is changing from 0 to 1 because it is ripple counter.

CLK	Q	A	B
	0	0	0
1	1	1	1
2	0	1	1
3	1	0	1
4	0	0	1
5	1	1	0

20. (b)

$$\left.\begin{aligned} S_1 &= C \\ S_0 &= A \end{aligned}\right\}$$

$$\begin{aligned} E &= C \\ I_0 &= B \oplus D \\ I_1 &= 1 \\ I_2 &= \bar{D} \\ I_3 &= BD \end{aligned}$$

Mux output is

$$Y = \left[\bar{S}_1 \bar{S}_0 I_0 + \bar{S}_1 S_0 I_1 + S_1 \bar{S}_0 I_2 + S_1 S_0 I_3\right]\bar{E}$$

Substituting the values

$$\begin{aligned} f(A, B, C, D) &= \left[\bar{C}\bar{A}(B \oplus D) + \bar{C}A(1) + C\bar{A}(\bar{D}) + CA(BD)\right]\bar{C} \\ &= \bar{C}\bar{A}(B \oplus D + \bar{C}A + \underbrace{C\bar{C}\bar{A}\bar{D}}_{0} + \underbrace{C\bar{C}ABD}_{0} \\ &= \bar{C}\bar{A}(\bar{B}D + B\bar{D}) + \bar{C}A \\ &= \underset{1}{\bar{A}\bar{B}\bar{C}D} + \underset{4}{\bar{A}B\bar{C}\bar{D}} + \underset{(8,9,12,13)}{A\bar{C}} \\ &= \sum m(1, 4, 8, 9, 12, 13) \end{aligned}$$

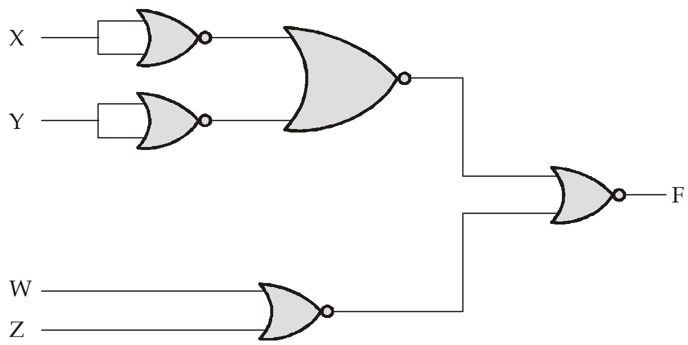
21. (c)

$$F = \bar{X}Z + \bar{X}W + \bar{Y}Z + \bar{Y}W$$

K-map

XY \ WZ	00	01	11	10
00	0	1	1	1
01	0	1	1	1
11	0	0	0	0
10	0	1	1	1

$$F = (\bar{X} + \bar{Y})(W + Z)$$



Total 5 NOR gates are required.

22. (b)

Given, Input frequency = 640 kHz

Output frequency after 4-bit ring counter = $\frac{640}{4} = 160\,\text{kHz}$

Output frequency after 4-bit Johnson counter = $\frac{160}{8} = 20\,\text{kHz}$

Output frequency after decade counter = $\frac{20}{10} = 2$ kHz

23. (b)

Number of flip-flops for mod-8 ripple counter = 3

Maximum clock frequency = $f = \frac{1}{T}$

$$\Rightarrow \quad 4 \text{ MHz} = \frac{1}{3 \times x \text{ ns}} \text{Hz}$$

$$\Rightarrow \quad 4 \times 10^6 \text{ Hz} = \frac{10^9}{3 \times x} \text{Hz}$$

$$\Rightarrow \quad x = \frac{10^9}{4 \times 10^6 \times 3} = \frac{10^3}{12} = 83.33$$

24. **(d)**

Let,

A =		a_2	a_1	a_0
B =			b_1	b_0
A × B =		a_2b_0	a_1b_0	a_0b_0
	b_1a_2	b_1a_1	b_1a_0	$\downarrow$
	b_1a_2	$(a_2b_0 + a_1b_1)$	$(a_1b_0 + b_1a_0)$	a_0b_0
	C_3	C_2	C_1	C_0

Number of AND gates required X = 6

Number of one bit full adders required Y = 3

$$X + Y = 6 + 3 = 9$$

25. **(d)**

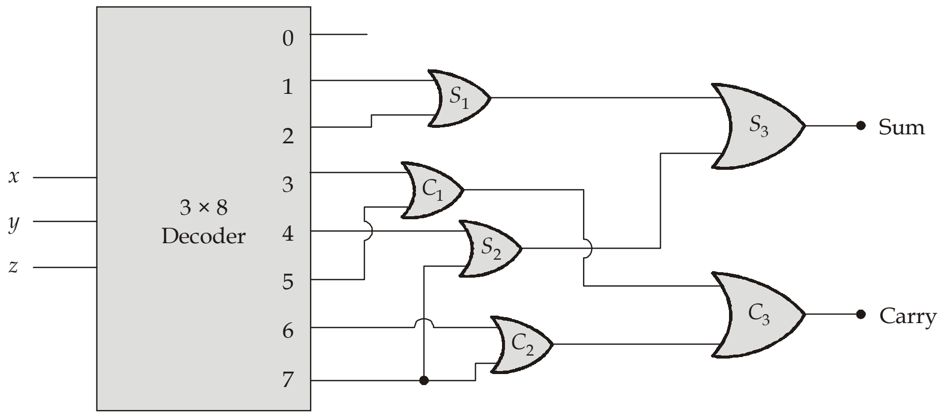
Present state (Q_n)	Input (Y)	Next state (Q_{n+1})
0	1	0
0	0	1
1	1	0
1	0	0

$$Q_{n+1} = \overline{Q_n + Y}$$

26. **(c)**

To implement full adder using 3 × 8 decoder

$$\text{Sum } (x, y, z) = \Sigma(1, 2, 4, 7)$$
$$\text{Carry } (x, y, z) = \Sigma(3, 5, 6, 7)$$



Hence 3 OR-gate is required for sum and 3-OR-gate is required for carry.

So, total 6 OR-gates is needed.

27. **(d)**

Given that,

$$D_A = Q_B,$$
$$J_B = Q_C,$$
$$K_B = \bar{Q}_C,$$
$$D_C = Q_C \odot Q_A$$

So, the state table is

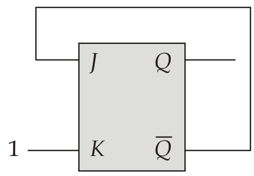
Clock	Present state Q_A	Q_B	Q_C	Next state Q_A	Q_B	Q_C	D_A	J_B	K_B	D_C
1	1	1	0	1	0	0	1	0	1	0
2	1	0	0	0	0	0	0	0	1	0
3	0	0	0	0	0	1	0	0	1	1
4	0	0	1	0	1	0	0	1	0	0
5	0	1	0	1	0	1	1	0	1	1
6	1	0	1	0	1	1	0	1	0	1

Hence 6 clock pulses are required.

28. **(d)**

All the above statements are correct.

29. **(c)**



	J	K	Q	$\overline{Q}$
			0	1
1	1	1	1	0
2	0	1	0	1
3	1	1	1	0
4	0	1	0	1
5	1	1	1	0
6	0	1	0	1

The output Q will be 101010.

30. **(a)**

The total delay for synchronous series counter

$$= t_{pd} \text{ (of FF)} + (n - 2)\, t_{pd} \text{ (of AND gate)}$$

where n = Number of flip-flops

As $M \le 2^n$ (Where M = modulus)

So, $256 \le 2^n$

$$n = 8$$

$$\text{Total delay} = 25 + (8 - 2)\, 5$$

$$= 25 + 30 = 55 \text{ nsec}$$

So, the maximum frequency of MOD-256 counter will be

$$= \frac{1}{55\,\text{nsec}} = 18.18 \text{ MHz}$$

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