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MADE EASY
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COMPUTER ORGANISATION

ELECTRONICS ENGINEERING

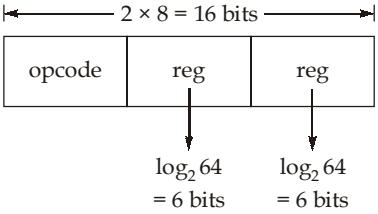
Date of Test : 17/08/2026

ANSWER KEY ➤

1.	(b)	6.	(a)	11.	(a)	16.	(b)	21.	(c)
2.	(d)	7.	(c)	12.	(b)	17.	(c)	22.	(b)
3.	(d)	8.	(b)	13.	(b)	18.	(b)	23.	(b)
4.	(b)	9.	(a)	14.	(d)	19.	(b)	24.	(a)
5.	(a)	10.	(d)	15.	(c)	20.	(a)	25.	(d)

Detailed Explanations

1. (b)



$\therefore$ Bit assigned to opcode = 16 – 6 – 6 = 4 bits

$\therefore$ No. of instructions in CPU = 2^4

= 16 instructions

2. (d)

- Serial connection of interrupt lines for establishing hardware priority is known as daisy chaining.
- During DMA, only one of the CPU or DMA can be BUS master at a time. CPU release BUS only after getting request from DMA and get after DMA release the BUS.

3. (d)

4. (b)

	4	5	7	12	4	5	13	4	5	7	13	12
0	4	4	4	4	(4)	4	4	(4)	4	4	4	12
1		5	5	5	5	(5)	5	5	(5)	5	5	5
2			7	7	7	7	13	13	13	13	(13)	13
3				12	12	12	12	12	12	7	7	7
					*	*		*	*		*	

Number of page hits = 5

Total pages = 12

$$\text{Hit ratio} = \frac{\text{Page hits}}{\text{Total pages}} = \frac{5}{12} = 0.4167$$

5. (a)

Time taken by five stage pipeline processor for executing single instruction,

T = Max(150, 120, 150, 160, 140)

T = 160 nsec

Time required to execute 100 independent instructions

= [5 + (100 – 1)]160

= (5 + 99) × 160 = 16640 nsec

= 16.64 μsec

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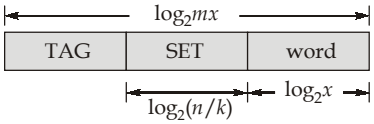
6. (a)

Number of sets = n/k

Let there are x words per block in main memory.



$$\text{No. of TAG bits} = \log_2(mx) - \left(\log_2\frac{n}{k} + \log_2 x\right)$$

$$= \log_2(mx) - \log\frac{nx}{k} = \log_2\frac{mk}{n}$$

7. (c)

In block transfer, the entire block of data is transferred then only CPU again becomes bus master. In vectored interrupt, I/O device along with interrupts send vector address of interrupt service routine which guide CPU to execute for a specific I/O device.

8. (b)

RISC is used in real time application.

9. (a)

The control data register holds the present microinstruction while next address is computed and read from memory. The data register is sometimes called a pipeline register. Microinstructions are stored in control memory in groups, with each group specifying a routine, where each routine specifies how to carry out an instruction.

10. (d)

$$\text{Avg } CPI = \Sigma(IC_i \times CPI_i), \text{ where IC is instruction count}$$
$$= 0.6 \times 1 + 0.18 \times 2 + 0.12 \times 4 + 0.1 \times 8$$
$$= 2.24$$

$$\therefore \quad \text{Avg. CPU time} = (\text{Avg. CPI}) \times \text{Cycle time}$$

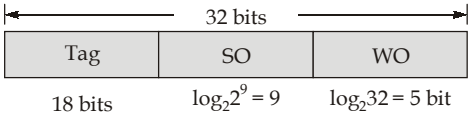
$$= 2.24 \times \frac{1}{400 \times 10^6}$$

$$\text{Avg. CPU time} = 5.6 \text{ nsec}$$

11. (a)

$$\text{Number of lines} = \frac{64K}{32} = 2^{11}$$

$$\text{Number of sets} = \frac{2^{11}}{4} = \frac{2^{11}}{2^2} = 2^9$$



$$\text{Tag memory size} = S \times P \times \#\text{ tag bits} = 2^9 \times 4 \times (18 + 1 + 1 + 2)$$
$$= 2^9 \times 2^2 \times 22 \text{ bits} = 2^{10} \times 2 \times 22 \text{ bits}$$
$$= 44 \text{ K bits}$$

12. (b)

$$T_{avg} = h_1 t_1 + (1 - h_1)h_2 (t_2 + t_1) + (1 - h_1)(1 - h_2)(t_3 + t_2 + t_1)$$
$$= 0.65 \times 0.02 + 0.35 \times 0.45 \times 0.22 + 0.35 \times 0.55 \times 2.22$$
$$= 0.013 + 0.03465 + 0.42735$$
$$= 0.475 = 475\ \mu sec$$

13. (b)

Size of memory system = 60 kB

Size of memory chip = $2^n \times m$ bits

where $n \rightarrow$ No. of address lines

$m \rightarrow$ No. of data lines

$\therefore$ Size of one memory chip = $2^{13} \times 5$ bits

$$\therefore \text{No. of chips required} = \frac{\text{Size of memory system}}{\text{Size of one memory chip}} = \frac{60 \times 2^{10} \times 8}{2^{13} \times 5} = 12$$

14. (d)

To select ROM IC $\rightarrow$ Decoder output Y_1 should be low i.e. $A_{15}\ A_{14}\ A_{13} = 001$.

Starting address: $\underbrace{A_{15}\ A_{14}\ A_{13}\ A_{12}}_{0\ 0\ 1\ 0}\ \underbrace{A_{11}\ A_{10}\ A_9\ A_8}_{0\ 0\ 0\ 0}\ \underbrace{A_7\ A_6\ A_5\ A_4}_{0\ 0\ 0\ 0}\ \underbrace{A_3\ A_2\ A_1\ A_0}_{0\ 0\ 0\ 0}$

$(2000)_H$

Ending address: $\underbrace{A_{15}\ A_{14}\ A_{13}\ A_{12}}_{0\ 0\ 1\ 1}\ \underbrace{A_{11}\ A_{10}\ A_9\ A_8}_{1\ 1\ 1\ 1}\ \underbrace{A_7\ A_6\ A_5\ A_4}_{1\ 1\ 1\ 1}\ \underbrace{A_3\ A_2\ A_1\ A_0}_{1\ 1\ 1\ 1}$

$(3FFF)_H$

$\therefore$ ROM IC address range $\Rightarrow$ 2000H to 3FFFH

To select RAM IC $\rightarrow$ Decoder output Y_6 should be zero i.e. $A_{15}\ A_{14}\ A_{13} = 110$.

Starting address: $\underbrace{A_{15}\ A_{14}\ A_{13}\ A_{12}}_{1\ 1\ 0\ 0}\ \underbrace{A_{11}\ A_{10}\ A_9\ A_8}_{0\ 0\ 0\ 0}\ \underbrace{A_7\ A_6\ A_5\ A_4}_{0\ 0\ 0\ 0}\ \underbrace{A_3\ A_2\ A_1\ A_0}_{0\ 0\ 0\ 0}$

$(C000)_H$

Ending address: $\underbrace{1\ 1\ 0\ 1}_{(DFFF)_H}\ \underbrace{1\ 1\ 1\ 1}\ \underbrace{1\ 1\ 1\ 1}\ \underbrace{1\ 1\ 1\ 1}$

$\therefore$ RAM IC address range $\rightarrow$ C000H to DFFFH

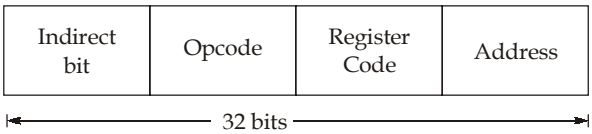
15. (c)

Memory unit = 512 K words

$= 2^9 \times 2^{10} = 2^{19}$ words

Instruction size = 32 bits

Instruction has 4 fields:



Bits required to specify one register = $\log_2 64 = 6$ bits

For address, bits required = $\log_2(2^{19}) = 19$ bits

For indirect bit, 1 bit is required.

Bits required for opcode = 32 – 1 – 19 – 6

= 6 bits

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16. (b)

Size of 8 k memory = $2^3 \times 2^{10} = 8192$ bytes

in hexadecimal, 8192 bytes = 2000

The lowest address in RAM is 1000 H, then last address will be $(1000)_H + (1FFF)_H = (2FFF)_H$

17. (c)

For the given NAND gate $A_{15} = 1$, $A_{14} = 0$, $A_{13} = 1$, then only the chip was select.

For 4k RAM = $2^2 \times 2^{10} = 2^{12}$, there are 12 Address lines (A_0 to A_{11}).

A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	.....	A_0
1	0	1	x	0	.....	0
	⋮			⋮		
1	0	1	x	1	.....	1

Memory range if x = 0

1010 0000 0000 0000 ⇒ A000 H

⋮

1010 1111 1111 1111 ⇒ AFFF H

Memory range if x = 1

1011 0000 0000 0000 ⇒ B000 H

⋮

1011 1111 1111 1111 ⇒ BFFF H

∴ The memory range : A000 H - AFFF H and B000 H - BFFF H

18. (b)

Given,

Clock frequency, $f = 2$ MHz

For execution of the instruction "STA 2019 H"

4 machine cycles (13 T-states) are required.

$$\therefore \quad T = \frac{1}{f} = \frac{1}{2\text{ MHz}} = \frac{1}{2}\ \mu\text{sec}$$

$$\text{The execution time} = 13\text{ T} = 13 \times \frac{1}{2}\ \mu\text{sec} = 6.5\ \mu\text{sec}$$

19. (b)

Load and store take 2 memory access, 1 for IF and 1 for loading/storing

= 100(IF) + 1 × 0.25 × 100 (loading/storing)

= 125 memory access.

$$\text{Avg. memory access/instruction} = \frac{125}{100} = 1.25 \text{ memory access/instruction}$$

Cycles per instruction for handling cache misses.

= (Memory access per instruction × miss rate × Cycles per miss)

= (1.25 × 0.02 × 102) = 2.55 cycles per instruction

Cycles per instruction for handling cache hits.

= Memory accesses per instruction × Hit rate × Cycles per hit

= 1.25 × 0.98 × 2 = 2.45 cycles per instruction

Effective CPI = Cycles for hits + Cycles for misses.

= 2.55 + 2.45 = 5

20. (a)

Interrupt vector gives the branch address of an interrupting device.

21. (c)

Mode field is used to locate the operands needed for the operation.

- for next instruction address program counter is used.
- opcode field is used to tell about the type of operation.

22. (b)

23. (b)

$$\text{Speed-up} = \frac{\text{Execution time of non-pipeline}}{\text{Execution time of pipeline}}$$

$$\text{Speed up factor} = \frac{4}{1+0.42\times 3} = \frac{4}{2.26} = 1.76$$

24. (a)

$$\text{Speed-up} = \frac{T_{\text{non-pipeline}}}{T_{\text{pipeline}}}$$

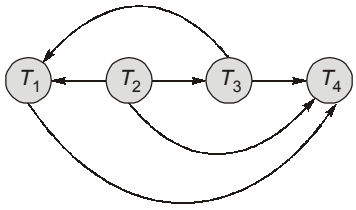
$$5 = \frac{CPI_n \times \text{No. of instructions} \times \text{Cycle time}_n}{CPI_p \times \text{No. of instructions} \times \text{Cycle time}_p}$$

$$5 = \frac{CPI_n \times (4+8+3+6+9)}{1\times \max\{4,8,3,6,9\}}$$

$$5 = \frac{CPI_n \times 30}{1\times 9}$$

$$CPI_n = \frac{45}{30} = 1.50$$

25. (d)



No cycle, so conflict serializable.

In given schedule no dirty read present so schedule is recoverable also.

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