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Delhi | Bhopal | Hyderabad | Jaipur | Pune

Web: www.madeeasy.in | E-mail: info@madeeasy.in | Ph: 011-45124612

DIGITAL ELECTRONICS

ELECTRICAL ENGINEERING

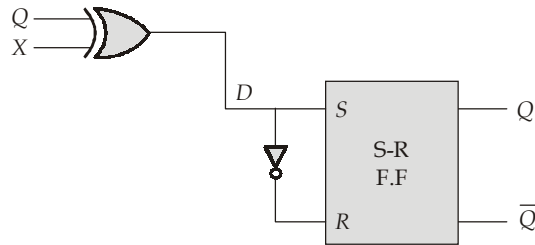
Date of Test : 26/08/2026

ANSWER KEY ➤

- | | | | | |
|--------|---------|---------|---------|---------|
| 1. (c) | 7. (b) | 13. (b) | 19. (c) | 25. (b) |
| 2. (c) | 8. (d) | 14. (b) | 20. (c) | 26. (b) |
| 3. (c) | 9. (b) | 15. (d) | 21. (d) | 27. (b) |
| 4. (b) | 10. (a) | 16. (a) | 22. (a) | 28. (b) |
| 5. (d) | 11. (c) | 17. (a) | 23. (b) | 29. (d) |
| 6. (d) | 12. (d) | 18. (b) | 24. (d) | 30. (a) |

DETAILED EXPLANATIONS

1. (c)



$$Q_{n+1} = D = Q \oplus X$$

Therefore, the given circuit acts as T flip-flop for $T = X$.

2. (c)

$$\begin{aligned}
 f &= \bar{x}\bar{y} + \bar{x}y + x\bar{y} \\
 &= x(\bar{y} + y) + x\bar{y} \\
 &= \bar{x} + x\bar{y} \\
 &= (\bar{x} + x) \cdot (\bar{x} + \bar{y}) = \bar{x} + \bar{y} = \overline{x \cdot y}
 \end{aligned}$$

Thus it works as NAND gate.

3. (c)

Number of AND gates present in n -bit carry look ahead adder is

$$= \frac{n(n+1)}{2} = \frac{6(6+1)}{2} = 21$$

4. (b)

For decoding any binary data, output must be high for that data (code) and this is possible in one 4-input AND gate, one inverter option only.

A decoder is a combinational circuit that converts n -bit binary coded data upto 2^n outputs.

5. (d)

$$\text{Resolution} = \frac{V_R}{2^n} = \frac{10}{2^8} = 39.06 \text{ mV}$$

$$\text{Count value} = (1000\ 0110)_2 = (134)_{10}$$

$$\begin{aligned}
 \text{Analog output voltage} &= 134 \times 39.06 \text{ mV} \\
 &= 5.226 \text{ Volts}
 \end{aligned}$$

6. (d)

$$\text{Output voltage} = (\text{Resolution in volts}) \times (\text{Decimal equivalent input})$$

$$0.2 = K \times 2$$

 $\Rightarrow$

$$\text{Resolution, } K = 0.1 \text{ Volt}$$

$$\begin{aligned}
 V_{\text{out}} &= 0.1 \times [30] \\
 &= 3 \text{ Volt}
 \end{aligned}$$

7. (b)

Given that,

$$\begin{array}{r} 1011001111 \\ + 1 \\ \hline 1011010000 \\ \hline \end{array}$$

Complemented
output

∴ No. of flip flop = 5

8. (d)

The flip-flop is connected in toggle mode. Thus, $Q_{n+1} = \bar{Q}_n$.

9. (b)

By properly arranging the given k -map.

		CD			
AB		00	01	11	10
	00	1	1	1	1
	01	0	1	1	0
	11	0	1	1	0
	10	1	1	1	1

D

$$\therefore f = \bar{B} + D$$

$$\therefore \text{Complement, } f^c = B\bar{D}$$

10. (a)

The given circuit is SR flip-flop.

The race around condition occurs in JK flip-flop.

11. (c)

From the given diagram,

$$J_1 = \bar{Q}_1 Q_2$$

$$K_1 = \bar{Q}_2$$

$$J_2 = K_2 = \bar{Q}_1$$

Also given, $Q_1 = 0; Q_2 = 0$ initially

Clk	Q_1	Q_2	J_1	K_1	J_2	K_2
0	0	0	0	1	1	1
1	0	1	1	0	1	1
2	1	0	0	1	0	0
3	0	0	0	1	1	1

∴ It is MOD-3 counter.

12. (d)

PS		NS		FF inputs	
Q_A	Q_B	Q_A	Q_B	J_B	k_B
0	0	1	1	1	x
1	1	1	0	x	1
1	0	0	1	1	x
0	1	0	0	x	1

On solving for J_B and k_B

Q_A	Q_B		
	0	1	
0	1	x	$J_B = 1$
1	1	x	

Q_A	Q_B		
	0	1	
0	x	1	$k_B = 1$
1	x	1	

13. (b)

From the given code converter we can write

$$x + (1\text{'s complement of } 0011) + 1 = \text{BCD}$$

$$x + 1100 + 1 = \text{BCD}$$

$$x + 1101 = \text{BCD}$$

$$x = \text{BCD} - 1101 = \text{BCD} + (2\text{'s complement of } 1101)$$

 $\therefore$

$$x = \text{BCD} + 0011 = \text{Excess-3 code}$$

14. (b)

Present State		Next State		T_B	T_A
Q_B	Q_A	Q_B^+	Q_A^+		
0	0	1	1	1	1
0	1	1	0	1	1
1	0	0	0	1	0
1	1	0	1	1	0

$$T_B = 1;$$

$$T_A = \bar{Q}_B \bar{Q}_A + \bar{Q}_B Q_A$$

$$T_A = \bar{Q}_B$$

15. (d)

Given that,

$$f(A, B, C) = \Pi M(1, 3, 4, 5) = \Sigma m(0, 2, 6, 7)$$

Now,

	I_0	I_1	I_2	I_3
$\bar{A}$	①	1	②	3
A	4	5	⑥	⑦
	$\bar{A}$	0	1	A

$\Rightarrow$ Corresponding MUX Inputs

$$\therefore \text{ Required inputs are, } I_0 = \bar{A}, I_1 = 0, I_2 = 1 \text{ and } I_3 = A$$

16. (a)

$$X\bar{Y} + \bar{X}Y = Z$$

∴

$$\begin{aligned} X\bar{Z} + \bar{X}Z &= X(\overline{X\bar{Y} + \bar{X}Y}) + \bar{X}(X\bar{Y} + \bar{X}Y) \\ &= X(\overline{X\bar{Y}} \cdot \overline{\bar{X}Y}) + \bar{X}(X\bar{Y} + \bar{X}Y) \\ &= X((\bar{X} + Y)(X + \bar{Y})) + \bar{X}Y \\ &= X(XY + \bar{X}\bar{Y}) + \bar{X}Y \\ &= XY + \bar{X}Y = Y \end{aligned}$$

17. (a)

Using Truth table:

A	B	C	D	$S_1 \times S_2$	F
0	0	0	0	$0 \times 0 = 0 \leq 2$	1
0	0	0	1	$0 \times 1 = 0 \leq 2$	1
0	0	1	0	$0 \times 2 = 0 \leq 2$	1
0	0	1	1	$0 \times 3 = 0 \leq 2$	1
0	1	0	0	$1 \times 0 = 0 \leq 2$	1
0	1	0	1	$1 \times 1 = 1 \leq 2$	1
0	1	1	0	$1 \times 2 = 2 \leq 2$	1
0	1	1	1	$1 \times 3 = 3 > 2$	0
1	0	0	0	$2 \times 0 = 0 \leq 2$	1
1	0	0	1	$2 \times 1 = 2 \leq 2$	1
1	0	1	0	$2 \times 2 = 4 > 2$	0
1	0	1	1	$2 \times 3 = 6 > 2$	0
1	1	0	0	$3 \times 0 = 0 \leq 2$	1
1	1	0	1	$3 \times 1 = 3 > 2$	0
1	1	1	0	$3 \times 2 = 6 > 2$	0
1	1	1	1	$3 \times 3 = 9 > 2$	0

∴

$F =$

		CD		
AB				
	1	1	1	1
	1	1	0	1
	1	0	0	0
	1	1	0	0

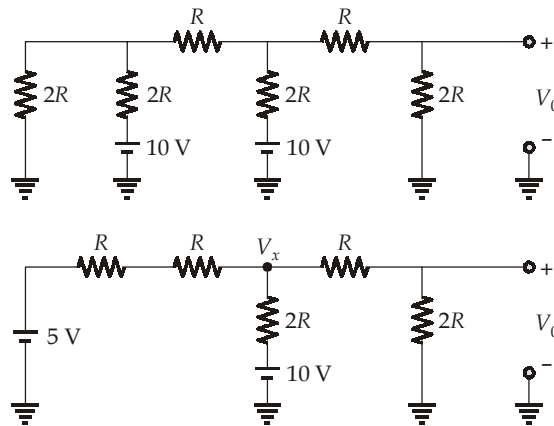
$$F = \bar{A}\bar{B} + \bar{A}\bar{C} + \bar{C}\bar{D} + \bar{A}\bar{D} + \bar{B}\bar{C}$$

18. (b)

At switch states,

$$\begin{aligned} S_0 &= 0, \\ S_2 &= 1 \end{aligned}$$

$$S_1 = 1;$$



$$\frac{V_x - 5}{2R} + \frac{V_x - 10}{2R} + \frac{V_x}{3R} = 0$$

$$V_x \left[\frac{1}{2} + \frac{1}{2} + \frac{1}{3} \right] = 7.5$$

$$V_x \left[\frac{4}{3} \right] = 7.5$$

$$\begin{aligned} V_x &= 7.5 \times 0.75 \\ &= 5.625 \text{ Volt} \end{aligned}$$

$$V_0 = \frac{2}{3} V_x = \frac{2}{3} \times 5.625 = 3.75 \text{ Volt}$$

19. (c)

D	C	A	
0	0	0	$\rightarrow I_0$
0	0	1	$\rightarrow I_1$
0	1	0	$\rightarrow I_2$
0	1	1	$\rightarrow I_3$
1	0	0	$\rightarrow I_4$

Combination selects the I_3 . Also, we have the given logic function as

$$F = AC + ABD + ACD + BCD$$

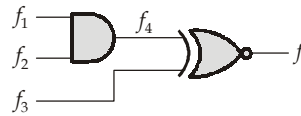
So by substituting $D = 1$; $C = 0$; $A = 0$;We get, $F = 0 + 0 + 0 + 0 = 0$ Thus, input I_4 must be equal to 0.

20. (c)

$$\begin{aligned} Y &= \bar{A}\bar{B} + B\bar{C} \\ Z &= Y + \bar{B} = \bar{A}\bar{B} + B\bar{C} + \bar{B} \\ &= \bar{B}(1 + \bar{A}) + B\bar{C} \\ &= \bar{B} + B\bar{C} = (\bar{B} + B)(\bar{B} + \bar{C}) \\ Z &= \bar{B} + \bar{C} \end{aligned}$$

BC		00	01	11	10
A	0	1	1	0	1
	1	0	0	0	1

21. (d)



$$f_4 = f_1 \cap f_2 = \Sigma(2, 8, 14)$$

EX-NOR is an equivalence circuit,

$$\begin{aligned} \therefore f &= (f_4 \oplus f_3) = f_4 f_3 \cup \bar{f}_4 \bar{f}_3 \\ &= \Sigma(0, 1, 2, 3, 4, 5, 6, 9, 10, 12, 13, 14, 15) \end{aligned}$$

22. (a)

$$\begin{aligned} F(A, B, C) &= A\bar{B} \cdot \bar{C} + (0)\bar{B}C + \bar{A}(B\bar{C}) + 1(B \cdot C) \\ &= \underset{(4)}{A\bar{B}\bar{C}} + \underset{(2)}{\bar{A}B\bar{C}} + \underset{(3,7)}{BC} \\ &= \Sigma m(2, 3, 4, 7) \end{aligned}$$

23. (b)

	$\frac{J_2}{\bar{Q}_1}$	$\frac{K_2}{Q_0}$	$\frac{J_1}{Q_2}$	$\frac{K_1}{\bar{Q}_2}$	$\frac{J_0}{Q_1}$	$\frac{K_0}{\bar{Q}_1}$	$\frac{Q_2}{0}$	$\frac{Q_1}{0}$	$\frac{Q_0}{0}$
1 st clock	1	0	0	1	0	1	1	0	0
2 nd clock	1	0	1	0	0	1	1	1	0
3 rd clock	0	0	1	0	1	0	1	1	1

24. (d)

$$D = 1, C = 1, A = 0$$

combination

Select the I_6 . Also we have the given logic function as

$$F = AC + ABD + ACD + BCD$$

So, by substituting,

$$D = 1, C = 1, A = 0$$

We get,

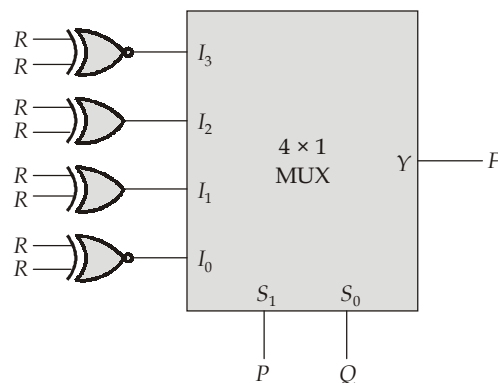
$$F = 0 + 0 + 0 + B$$

$$F = B$$

Thus, input I_6 must be equal to B .

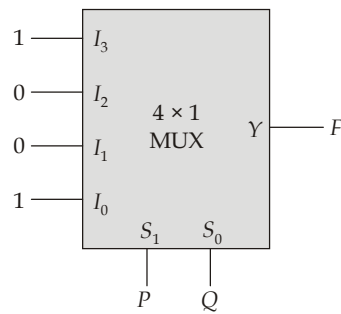
25. (b)

Redrawing the circuit as,



We get,

$$I_3 = I_0 = 1; \quad I_2 = I_1 = 0$$



∴

$$F = PQ + \bar{P}\bar{Q}$$

$$F = P \odot Q$$

26. (b)

We can write,

$$\text{Output } Y = \bar{S}I_0 + SI_1$$

where

$$S = A + B$$

$$Y = \overline{A+B}(AB) + (A+B)$$

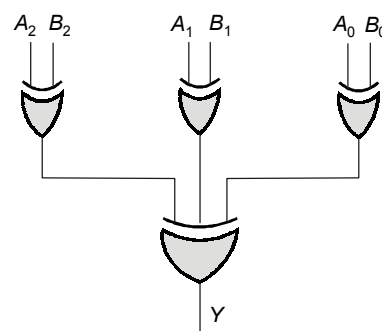
$$Y = A + B$$

27. (b)

$$\begin{aligned} \text{Output } Y &= (A + AB)(B + BC)(C + AB) \\ &= A(1 + B)B(1 + C)(C + AB) \\ &= AB(C + AB) \\ &= ABC + AB \\ &= AB(1 + C) \\ &= AB \end{aligned}$$

28. (b)

Redrawing the digital circuit



From the figure we get,

$$Y = A_0 \oplus B_0 \oplus A_1 \oplus B_1 \oplus A_2 \oplus B_2$$

So, Y is XOR of six boolean variables and Y will be 1 when odd number of variable are 1. Thus

there will be $\frac{2^6}{2} = 32$ cases for the output to be 1.

29. (d)

$$Y = \overline{Q_1 Q_3} \cdot \overline{Q_2 Q_3}$$

$$= Q_1 Q_3 + Q_2 Q_3$$

$$Y = Q_3(Q_1 + Q_2)$$

To reset the counter output Y must be one

$$Y = Q_3(Q_1 + Q_2)$$

Q_3	Q_2	Q_1	Q_0
1	0	1	0
1	1	0	0
1	1	1	0

when the counter output $Q_3 Q_2 Q_1 Q_0 = 1010$. Then the output Y will give output 1 and it will be given to inverter, so it will reset the counter and again counting will start and it will not go for further combinations.

30. (a)

In the given digital circuit each multiplexer is working as a NOT gate. Thus it is a ring oscillator with five NOT gates.

The frequency of oscillation will be $f = \frac{1}{2N t_{pd}}$.

N = number of NOT gates in cascade

t_{pd} = propagation delay of each NOT gate.

$$\therefore f = \frac{1}{2 \times 5 \times 25 \text{ ns}} = 4 \times 10^6 \text{ Hz} = 4 \text{ MHz.}$$

