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DIGITAL CIRCUITS

ELECTRONICS ENGINEERING

Date of Test : 27/07/2026

ANSWER KEY ➤

1.	(c)	7.	(b)	13.	(d)	19.	(d)	25.	(d)
2.	(b)	8.	(b)	14.	(a)	20.	(d)	26.	(b)
3.	(a)	9.	(a)	15.	(d)	21.	(a)	27.	(b)
4.	(b)	10.	(c)	16.	(b)	22.	(c)	28.	(c)
5.	(c)	11.	(b)	17.	(d)	23.	(a)	29.	(b)
6.	(b)	12.	(b)	18.	(b)	24.	(d)	30.	(b)

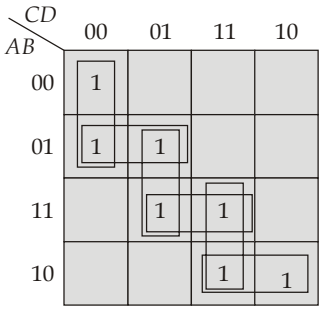
DETAILED EXPLANATIONS

1. (c)

The given logic function can be written as,

$$f(A, B, C, D) = \Sigma m(0, 4, 5, 10, 11, 13, 15)$$

Using *K*-map:



Total prime implicants = 6 ($AC'D'$, $A'BC'$, $BC'D$, ABD, ACD and $AB'C$)

Number of essential prime implicants = 2 ($A'C'D'$ and $AB'C$)

2. (b)

Given, $f_1(A, B, C) = \Sigma m(2, 3, 4)$

$f_2(A, B, C) = \pi M(0, 1, 5, 6, 7) = \Sigma m(2, 3, 4)$

For f_{out} to be zero, the function f_3 should be equal to,

$$f_3(A, B, C) = \Sigma m(2, 3, 4)$$

$\therefore$ The maximum number of possible minterms = 3.

3. (a)

From the given number, the minimum value of 'x' can be written as, "12 + 1 = 13" ($\because$ $C = 12$)

Therefore, the least decimal equivalent

$$= 10 \times 13^2 + 11 \times 13^1 + 12 \times 13^0 = 1690 + 143 + 12 = (1845)_{10}$$

5. (c)

Since, given that, $V_{out} = 0.2$ V for 00001

$\therefore$ the weight of LSB is 0.2 V.

The the weight of other bits in weighted D/A converter can be obtained as 0.4 V, 0.8 V, 1.6 V and 3.2 V respectively.

For a digital input of 11111, the value of output, $V_{out} = 3.2 + 1.6 + 0.8 + 0.4 + 0.2 = 6.2$ V.

6. (b)

Given, decimal number is $(417)_{10}$

8	417
8	52 – 1
	6 – 4

$\therefore$ $(417)_{10} = (641)_8$.

7. (b)

Output of 2 × 1 MUX, $Y = \bar{S} I_0 + S I_1$

where, $S = \bar{Q}; I_0 = \bar{X}; I_1 = X$

$\therefore$ $$Y = \overline{\overline{Q}}\,\overline{X} + \overline{Q}X$$

$$Y = Q\overline{X} + \overline{Q}X$$

Since, $Q_{n+1} = D = Y = Q\overline{X} + \overline{Q}X$

which is the characteristic equation of T flip-flop.

8. (b)

Let output of 4 × 1 MUX is P,

$\therefore$ $$P = \overline{S}_1\overline{S}_0 I_o + \overline{S}_1 S_0 I_1 + S_1\overline{S}_0 I_2 + S_1 S_0 I_3$$

where, $S_1 = A$; $S_0 = B$; $I_0 = 1$; $I_1 = 0$; $I_2 = B$, $I_3 = 1$

$$P = \overline{A}\,\overline{B}(1) + \overline{A}B(0) + A\overline{B}(B) + AB$$

$$P = \overline{A}\,\overline{B} + AB$$

Output, $$Y = \overline{S}I_0 + SI_1$$

$$= \overline{\overline{AB}}(B) + \overline{AB}\cdot P = AB + (\overline{A} + \overline{B})(\overline{A}\,\overline{B} + AB)$$

$$= AB + \overline{A}\,\overline{B} + \overline{A}\,\overline{B} = AB + \overline{A}\,\overline{B}$$

$$Y = A \odot B$$

9. (a)

In a 4-bit ripple counter, four flip-flops (FF0 to FF3) are used. The input frequency of flip-flop FF0 is 'f' and its output waveform frequency is $f/2$ which is applied as input of FF1. Consequently, the output waveform frequency of FF1 is $f/4$ which is used as input of FF2.

Then output waveform frequency of FF2 is $f/8$ which is used as input of FF3. Therefore, the output waveform frequency of FF3 is f/16 and the time period is

$$T = \frac{1}{\text{Frequency}} = \frac{16}{f}$$

Since, time period of the last flip-flop (FF3) is 128 microseconds.

$\therefore$ $$T = \frac{16}{f} = 128\times10^{-6}$$

$\therefore$ $$f = \frac{16}{128\times10^{-6}} = 125\,\text{kHz}$$

$\therefore$ The clock frequency of a 4-bit ripple counter is,

$$f = 125\ \text{kHz}$$

10. (c)

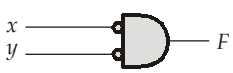
15's complement is equivalent to

$$\begin{array}{r} \text{F F F} \\ -\ \text{B B D} \\ \hline (4\ 4\ 2)_{16} \end{array}$$

11. (b)

$$F = \overline{\overline{x + \overline{y}} + x} = \overline{\overline{x + \overline{y}}\cdot\overline{x}} = (x + \overline{y})\cdot(\overline{x})$$

$$F = \overline{x}\,\overline{y}$$



12. (b)

In toggle mode of operation in *J-K* flip-flop, the output frequency is half of the clock frequency.

$$\therefore \quad f = \frac{1}{2} \times 3\,\text{MHz} = 1.5\,\text{MHz}$$

13. (d)

The *K*-map wraps around itself, so the top and bottom cells are adjacent to each other. The cells of the rightmost column are adjacent to those in the leftmost column of the map. The minterms may be grouped horizontally or vertically.

Groupings may occur in the size of 2^r where, $r = 1, 2, 3 \ldots n$.

14. (a)

Consensus theorem:

- Used to eliminate redundant term.
- A Boolean function contains 3 variables only.
- Each variable is used only 2-times.

Eg: $AB + \bar{A}C + BC = AB + \bar{A}C$

$(\bar{A} + B)(B + C)(A + C) = (\bar{A} + B)(A + C)$

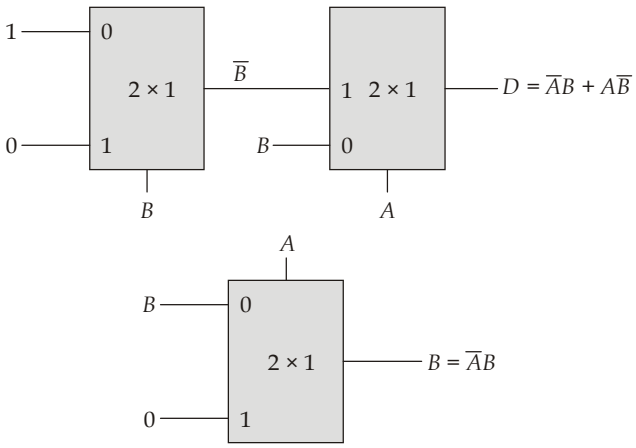
15. (d)

Half subtractor:

A	B	$D = A - B$	B
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

D = Difference, B = Borrow

$D = A \oplus B$ and $B = \bar{A}B$



Hence, Total number of 2 : 1 MUX required to implement half subtractor is "3".

16. (b)

The given circuit represents a 3-bit counter. So the count can be represented as

Clk	Q_2	Q_1	Q_0	
Initially	0	0	0	
1	0	0	1	
2	0	1	0	
3	0	1	1	
4	1	0	0	
5	1	0	1	$\Rightarrow$5th clock pulse
6	1	1	0	
7	1	1	1	

$\therefore$ $Y = Q_2 \oplus Q_1 \oplus Q_0 = 1 \oplus 0 \oplus 1 = 0$

17. (d)

Truth table of a 2-input EX-OR gate

A	B	$Y = A \oplus B$
0	0	0
0	1	1
1	0	1
1	1	0

Hence, the output is complement of second input if one input is logic '1'.

Truth table of 2-input EX-NOR gate

A	B	$Y = A \odot B$
0	0	1
0	1	0
1	0	0
1	1	1

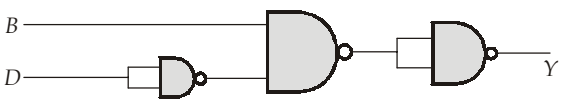
So, the output of 2-input EXNOR gate will be complement of second input if one input is at logic '0'.

18. (b)

Let $Y = \overline{\overline{\overline{(A+\bar{C})}\cdot B\bar{D}}\cdot\overline{(A+\bar{C})\cdot B\bar{D}}} = \overline{\left(\overline{\overline{(A+\bar{C})}+\overline{B\bar{D}}}\right)\cdot\overline{(A+\bar{C})}+\overline{B\bar{D}}}$

$= \overline{(A+\bar{C}+\bar{B}+D)(\bar{A}C+\bar{B}+D)} = \overline{(A+\bar{C})\bar{A}C+\bar{B}+D} = \overline{\bar{B}+D} = B\bar{D}$

$Y = \overline{\overline{B\bar{D}}}$



19. (d)

The 2421 code of decimal number 0 is 0000

9's complement of a number is obtained by subracting every digit of a decimal number from 9. 9's complement of 0000 is 1111 = $(9)_{10}$.

20. (d)

A code is said to be reflective when the code for 9 is complement of the code for 0, 8 for 1, 7 for 2, 6 for 3 and 5 for 4.

Excess-3 code is a reflective code as well as sequential code.

21. (a)

$$000 \xrightarrow{1^{st}\ CLK} 100 \xrightarrow{2^{nd}\ CLK} 010 \xrightarrow{3^{rd}\ CLK} 101$$

The op-amp circuit is a R-2R Ladder DAC with digital input 101. Therefore,

$$V_0 = -\left(\frac{R_f}{R}\right) \times \left(\frac{V_{ref}}{2^3}\right) \times (\text{Decimal equivalent of } 101)$$

$$V_0 = \frac{-R}{R} \times \frac{5}{8} \times 5$$

$$V_0 = -3.125 \text{ V}$$

22. (c)

$$Y(A, B) = \Sigma m(0, 3)$$

$$Y = \overline{A}\,\overline{B} + AB$$

	I_0 = A	I_1 = $\overline{A}$
$\overline{B}$	2	(0)
B	(3)	1
	B	$\overline{B}$

Since the select line is active low, $I_0 = B$ and $I_1 = \overline{B}$

23. (a)

- Serial adder requires less components compared to parallel adder.
- BCD to 7-segment can be constructed by one 4 × 16 decoder circuit as it requires 4 inputs and 7 outputs.

24. (d)

8	153	R
8	19	1
8	2	3
	0	2

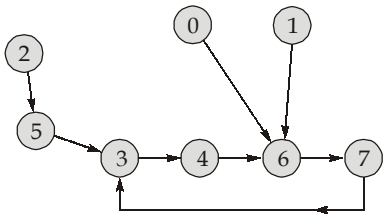
	Integer	Fraction
0.513 × 8	4	0.104
0.104 × 8	0	0.832
0.832 × 8	6	0.656
0.656 × 8	5	0.248
0.248 × 8	1	0.984
0.984 × 8	7	0.872

$$(153.513)_{10} = (231.406517)_8$$

25. (d)

Test for Lockout

Present State			Present Input				Nest State		
Q_2	Q_1	Q_0	J_2	K_2	J_1 K_1	J_0 K_0	Q_2	Q_1	Q_0
0	0	0	1	0	1 1	0 1	1	1	0
0	0	1	1	1	1 1	0 1	1	1	0
0	1	0	1	0	1 1	1 1	1	0	1
1	0	1	1	1	1 0	0 0	0	1	1



Hence, the counter does not enter into lockout state.

26. (b)

The number of self dual functions for n-variable = $(2)^{2^{n-1}} = 2^{(2^n/2)}$

For $n = 3$, No. of self dual functions = $2^{(2^3/2)} = 2^4 = 16$

27. (b)

We have, $$\frac{(19)_b + \left[\sqrt[3]{343}\right]_b}{(4)_b} = (13)_a$$

$$\frac{(b+9)+(7)}{4} = a + 3$$

$$b + 16 = 4a + 12$$

The above equation is valid for $a = 2$ and $b = 4$. Hence, $b = 2a$.

28. (c)

Excess-3 code is a 4-bit code.

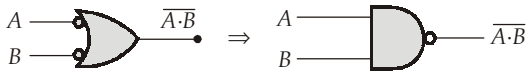
29. (b)

A	B	$A \odot B$
0	0	1
0	1	0
1	0	0
1	1	1

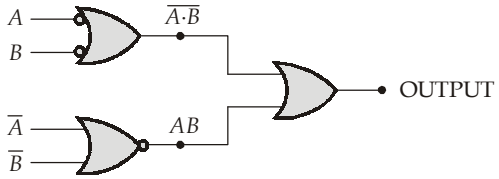
- Output is high, if both inputs are same.
- Output is low, if both inputs are different.

30. (b)

We know;



We have;



$\therefore$ Output = $\overline{A \cdot B} + A \cdot B$

= 1 ...[$\because X + \bar{X} = 1$]

■■■■