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COMPUTER ORGANIZATION

COMPUTER SCIENCE & IT

Date of Test : 27/06/2026

ANSWER KEY ➤

1.	(c)	7.	(b)	13.	(a)	19.	(d)	25.	(c)
2.	(d)	8.	(a)	14.	(d)	20.	(d)	26.	(c)
3.	(c)	9.	(b)	15.	(b)	21.	(b)	27.	(b)
4.	(a)	10.	(b)	16.	(c)	22.	(d)	28.	(d)
5.	(d)	11.	(b)	17.	(d)	23.	(b)	29.	(c)
6.	(c)	12.	(d)	18.	(b)	24.	(b)	30.	(c)

DETAILED EXPLANATIONS

1. (c)

Control word:

Flags	Control signal	Control word offset
$\log_2 18$ = 5 bit	$\log_2 85$ = 7 bit	$\log_2 (450 \times 20)$ = 14 bit

Length of control word = Flag + Control signal + Address
= 5 bit + 7 bit + 14 bit = 26 bit

2. (d)

Jump instruction is at address 4096 and is 4 bytes.
Therefore PC will point to 5000 on execution of this instruction.

Branch target address = PC + (–15)
= 5000 – 15 = 4985

3. (c)

When instruction is a computation:

Memory reference : Fetch instruction
Fetch reference of the operand
Fetch operand

Total 3 memory references.

When instruction is a branch:

Memory reference : Fetch instruction
Fetch operand reference and loading program counter

Total 2 memory references.

4. (a)

- **Implied addressing mode:** Specified implicitly in the definition of instruction.
- **Immediate addressing mode:** Specified in the address field of an instruction.
- **Register addressing mode:** Registers which are in CPU.
- **Register indirect addressing mode:** Register specifies the address of the operand.

5. (d)

Instruction pipelining is a technique that implements a form of parallelism called instruction level parallelism with a single processor.
It therefore allows faster CPU thoughput.

6. (c)

I_1 : 8000 – 8004
I_2 : 8005 – 8008
I_3 : 8009 – 8012
I_4 : 8013 – 8017
I_5 : 8018 – 8021
I_6 : 8022 – 8025
I_7 : 8026 – 8027
I_8 : 8028 – 8031
I_9 : 8032 – 8036

Return address (8026) is pushed onto the stack.

7. (b)

For 1 second it take 10^9 byte

$$\text{So for 64 kbyte it takes} = \frac{64k}{10^9} = 64\ \mu\text{sec}$$

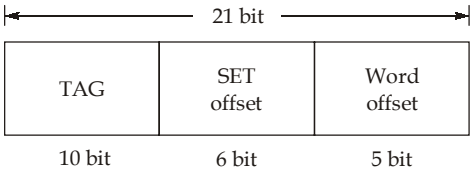
$$\text{Main memory latency} = 64\ \mu\text{sec}$$

$$\text{Total time required to fetch} = 64\ \mu\text{sec} + 64\ \mu\text{sec} = 128\ \mu\text{sec}$$

8. (a)

- Word offset = 1 block = 32 words = 5 bit
- CM size = 8 K-word
- $\text{Number of lines} = \dfrac{\text{CM Size}}{\text{Block Size}} = \dfrac{2^{13}}{2^5} = 2^8$
- $\text{Number of set} = \dfrac{\text{Number of lines}}{\text{Number of blocks per set}} = \dfrac{2^8}{2^2} = 2^6$

2M word MM $\rightarrow \log_2 2M = 21$ bit



9. (b)

The effective CPI of the pipeline can be calculated using the formula:

Effective CPI = 1 + Average stalls per instruction

Given that the pipeline is stalled due to a data hazard for every 3 out of 5 instructions, the average stalls per instruction is $\frac{3}{5}$.

$$\text{Effective CPI} = 1+\frac{3}{5}=1.6$$

Therefore, the correct answer is option (b).

10. (b)

1 bit	8 bits	23 bits
1	10000101	11000 ... 0
Sign	Exponent	Mantissa

Bias exponent value = 10000101

Actual exponent = 10000101 – 127 [$\because$ 127 is bias]

= 133 – 127 = 6

Normalized mantissa bits = 11000000000000000000000

Actual value = 1.11000000000000000000000

Decimal number = 1.11000×2^6

= $-(1110000)_2$

= $-(112)_{10}$

11. (b)

- **Isolated Input/Output:** This configuration uses the common bus and common address space but different control signal for both memory and input/output, so that memory address range is not affected by interface address assignment.
- **Memory Mapped Input/Output:** This configuration uses common bus and common control signals but unique address space.
- In synchronous clock is common and in asynchronous clock is different.

12. (d)

	1	2	3	4	5	6	7	8	9	10	11
I_1	IF	ID	EX	MM	WB						
I_2		IF	ID	ID	EX	MM	WB				
I_3			IF	IF	ID	EX	MM	WB			
I_4					IF	ID	EX	MM	WB		
I_5						IF	ID	ID	EX	MM	WB

Total 11 cycles are required.

13. (a)

Given: Total instruction length = 32 bits
Opcode field width = 6 bits
Memory address width = 2^{16}

The number of bits available for specifying memory addresses can be calculated as follows:

Address bits = Total bits – Opcode bits
Address bits = 32 – 6 = 26

The maximum number of directly addressed instructions that can be represented is equal to $2^{\text{Address bits}}$.

Max number of register = 2^{26}

However, the memory address width is limited to 2^{16} different memory locations. Therefore, the maximum number of instructions that can be directly addressed is 2^{10}.

14. (d)

(i) is true, it is logically done.
(ii) is false, structural dependency resolved using re-naming.
(iii) Delayed branch re-arranges code to reduce control dependency.

15. (b)

Considering each statement :

S_1 : Delayed control transfer, also known as delayed branching, is an attempt to cope with control hazards.

S_2 : The branch target stores the previous target address for the current branch, other algorithms for branch prediction also exist.

S_3 : For any given instruction set architecture implemented on a *N*-stage pipelined processor, *N* registers probably is not enough registers to completely prevent structural hazards involving a shortage of register hardware.

16. (c)

Consider each statement :

S_1 : Microprogrammed control unit uses variable logic to interrupt instruction since its uses encoded scheme for the instruction.

S_2 : Horizontal microprogramming control unit does not requires an additional hardware (like a decoder) because a fixed logic is associated with the instructions.

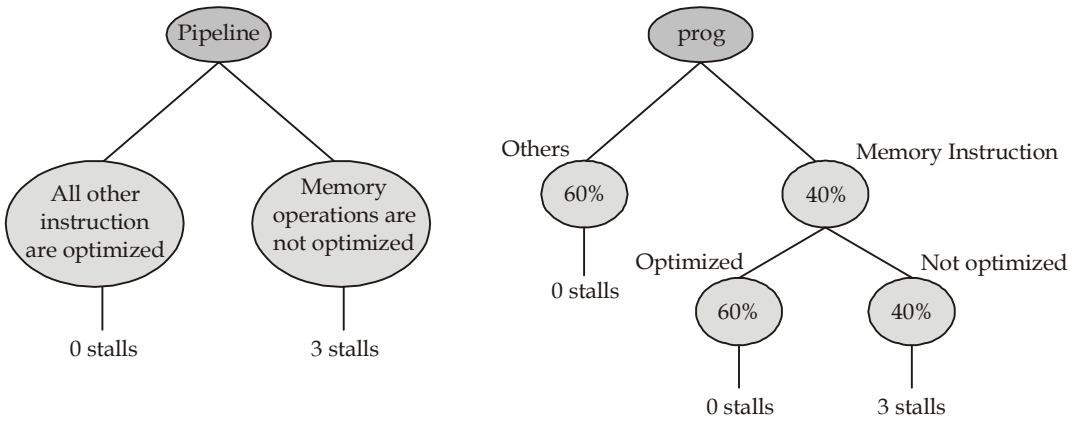
S_3 : The performance of a system depends on the direct proportion of memory accesses satisfied by cache.

17. (d)

WAR	WAW
$I_1(R_2) - I_0(R_2)$	$I_3(R_1) - I_0(R_1)$
$I_2(R_5) - I_1(R_5)$	
$I_3(R_1) - I_0(R_1)$	

So, WAR = 3 and WAW = 1

18. (b)



Number of stalls/Instruction = (0.4 × 0.4 × 3) = 0.48

Average instruction ET = (1 + # stalls / Instruction) × Cycle time

= (1 + 0.48) × 8 ns = 11.84 ns

19. (d)

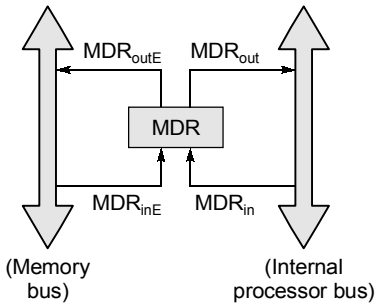
Increasing the cache line size brings in more from memory when a miss occurs. If accessing a certain byte suggests that nearby bytes are likely to be accessed soon (locality), then increasing the cache line essentially prefetches those other bytes. This, in turn, forestalls a later cache miss on those other bytes. If misses occur because the cache is too small, then the designers should increase the size!

Conflict misses occur when multiple memory locations are repeatedly accessed but map to the same cache location. Consequently, when they are accessed, they keep kicking one another out of the cache. Increasing the associativity implies that each chunk of the cache is effectively doubled so that more than one memory item can rest in the same cache chunk.

20. (d)

Considering each statement :

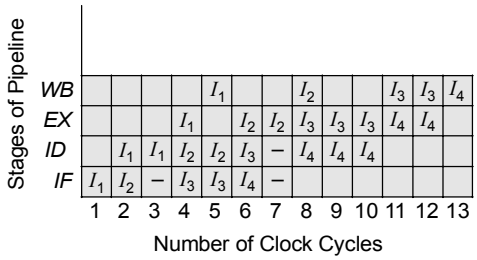
S_1 : 4-control signals are needed for each data register.



MDR is directly connected to data lines of the processor. It has 2 input and 2 output. Data may be loaded into MDR either from memory or from internal bus. Data present in MDR may be placed on either bus are memory. It requires total 4 control signals.

S_2 : The main disadvantage of direct mapping is that cache hit ratio decreases sharply if two or more frequently used blocks map on the same region.

21. (b)



22. (d)

IF	ID	OF	PD and WB
I_1 : 1 memory reference	2 memory reference	1 memory reference	–
I_2 : 1 memory reference	3 memory reference	2 memory reference	–
I_3 : 1 memory reference	1 memory reference	–	1 ALU operation
I_4 : 1 memory reference	3 memory reference	2 memory reference	–
I_5 : 1 memory reference	–	–	1 ALU operation

Total Execution Time = (Number of memory reference × 3 cycles + Number of ALU operation × 1 cycles) × cycle time

$$= (19 \times 3 + 2 \times 1) \times \frac{1}{5\ \text{GHz}} = \frac{59}{5}\ \text{ns} = 11.8\ \text{ns}$$

23. (b)

The required probability = $^{10}C_3 (0.35)^3 (0.65)^7 = 0.252$

24. (b)

Time taken by I/O device = $\frac{16\,\text{MB}}{128\,\text{kB}} = 128\,\text{sec}$

Percentage time CPU is busy = $\frac{128}{128+28} \times 100 = 82.05$

25. (c)

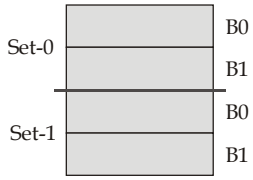
Register file size = $W(L + C) + G$

where,
W = 24 (number of register windows)
L = 30 (Local register)
C = 20 (= number of In or number of Out)
G = 40 (number of global register)

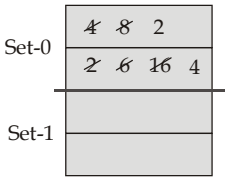
$\therefore$ Register file size = 24 (30 + 20) + 40 = 1240

26. (c)

Cache will be divided as,

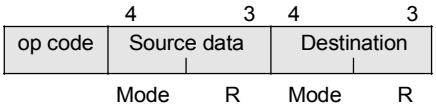


Since block addresses 4 and 2 are already there,



Total number of misses= 5

27. (b)



Register = 5 = 3 bits

Modes = 14 =4 bits

Type	Single operand or No operand	Double operand
Arithmetic (10)	2	8
Logic (15)	9	6
Data moving (20)	12	8
Branch (10)	5	5

Total 27 double operands = 5 bits

Size of instruction word = 5 + 7 + 7 = 19

28. (d)

$$T_{avg} = H_c T_c + (1 - H_c)(T_m + T_c)$$
$$= (0.9 \times 10) + (1 - 0.9)(100 + 10)$$
$$= 9 + 11 = 20 \text{ ns}$$

29. (c)

Number of tracks = Number of cylinders

Total size = (Number of surfaces) × (Number of tracks per surface) × (Number of sector per track) × (Size of a sector)

$= 32 \times 256 \times 512 \times 1024$

$= 2^5 \times 2^8 \times 2^9 \times 2^{10}$ bytes

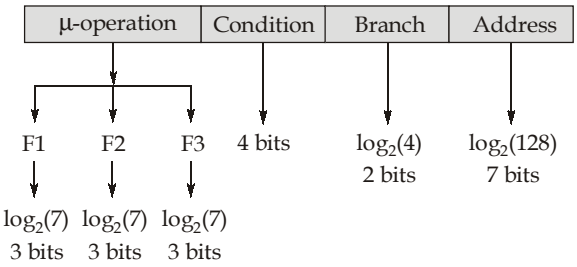
$= 2^{32}$ bytes

$= 2^2 \times 2^{30}$ bytes

= 4 GB

30. (c)

μ-instruction format:



Size of one micro-instruction = (3 + 3 + 3) + 4 + 2 + 7 = 22 bits

So, option (c) is correct answer.

■■■■