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DIGITAL LOGIC

COMPUTER SCIENCE & IT

Date of Test : 20/05/2026

ANSWER KEY >

- | | | | | |
|--------|---------|---------|---------|---------|
| 1. (b) | 7. (c) | 13. (a) | 19. (a) | 25. (d) |
| 2. (b) | 8. (d) | 14. (d) | 20. (b) | 26. (b) |
| 3. (d) | 9. (b) | 15. (b) | 21. (c) | 27. (d) |
| 4. (b) | 10. (c) | 16. (c) | 22. (b) | 28. (a) |
| 5. (a) | 11. (a) | 17. (c) | 23. (b) | 29. (c) |
| 6. (d) | 12. (a) | 18. (d) | 24. (d) | 30. (a) |

DETAILED EXPLANATIONS

1. (b)

$$\begin{aligned} X \oplus Y &= \overline{X \odot Y} = \overline{\overline{XY} + XY} \\ &= \overline{(\overline{XY})(\overline{XY})} \\ &= (X + Y)(\overline{X} + \overline{Y}) \\ &= \overline{X} + \overline{Y} \quad (\because X + Y = 1 \text{ which is given}) \end{aligned}$$

2. (b)

$$\begin{aligned} T &= 2 \times t_{pd} \\ T &= \text{Time period} \\ t_{pd} &= \text{Sum of propagation delay of all the gates} \\ 30 \text{ nsec} &= 2 \times t_{pd} \\ t_{pd} &= 15 \text{ nsec} \end{aligned}$$

i.e. total delay of the logic gates must be 15 nsec.

(Number of NAND gates (x) \times NAND gates propagation delay + Number of NOR gates (y) \times NOR gates propagation delay) = 15 nsec

$$= x \times \frac{3}{2} \text{ nsec} + y \times \frac{3}{2} \times 2 \text{ nsec}$$

Using option (b)

$$= 2 \times \frac{3}{2} \text{ nsec} + 4 \times \frac{3}{2} \times 2 \text{ nsec}$$

$$\Rightarrow 3 \text{ nsec} + 12 \text{ nsec} = 15 \text{ nsec}$$

Hence option (b) is correct.

3. (d)

Output of ExOR Gate = $b_i \oplus b_{i+1}$

Initially $Q = 0$ assume

So,

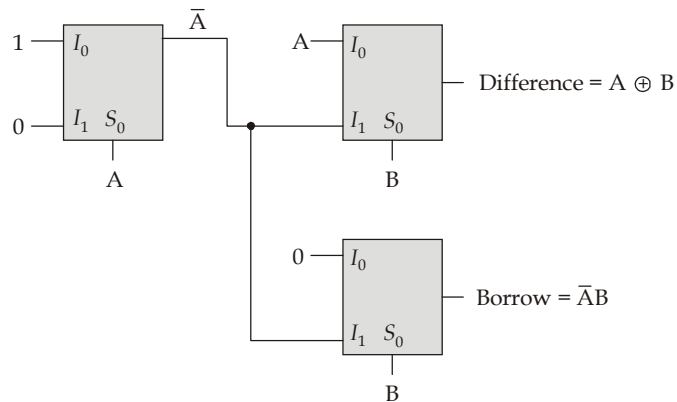
$$\begin{aligned} \text{After 1 clock, } Z &= b_7 \oplus b_0 \\ \text{After 2 clock, } Z &= b_7 \oplus b_6 \\ \text{After 3 clock, } Z &= b_6 \oplus b_5 \\ \text{After 4 clock, } Z &= b_5 \oplus b_4 \\ \text{After 5 clock, } Z &= b_4 \oplus b_3 \\ \text{After 6 clock, } Z &= b_3 \oplus b_2 \\ \text{After 7 clock, } Z &= b_2 \oplus b_1 \\ \text{After 8 clock, } Z &= b_1 \oplus b_0 \end{aligned}$$

Which is same as Binary to gray code converter.

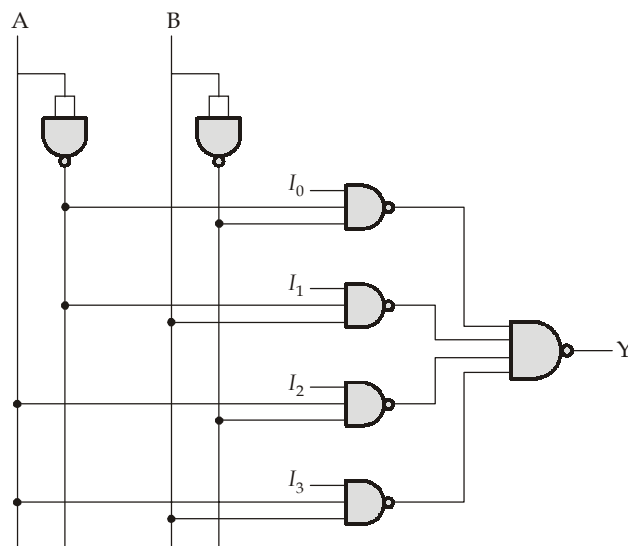
4. (b)

$$\begin{aligned} Y &= \overline{A}B + A \oplus C \\ &= \overline{A}B + \overline{A}C + \overline{A}C \\ \text{So, SOP} &= \sum m(1, 3, 4, 5, 6) \\ \text{POS} &= \prod M(0, 2, 7) \end{aligned}$$

5. (a)



6. (d)



7. (c)

We know that for a stage change to ripple through n stages i.e. $T_C = n \times t_{pd}$

$$f_c = \frac{1}{T_C}$$

$$f_c = \frac{1}{n \times t_{pd}}$$

So,

$$t_{pd} = \frac{1}{n \times f_c}$$

$$t_{pd}(\text{min}) = \frac{1}{10 \times 10 \times 10^6 \text{ Hz}} = 0.01 \times 10^{-6} \text{ sec} = 10 \times 10^{-9} \text{ sec} = 10 \text{ nsec}$$

8. (d)

S	R	T	Q	Q ⁺
0	0	0	0	0
0	0	0	1	1
0	0	1	0	1
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	1
0	1	1	1	0
1	0	0	0	1
1	0	0	1	1
1	0	1	0	1
1	0	1	1	0
1	1	0	0	0
1	1	0	1	1
1	1	1	0	1
1	1	1	1	0

SR \ TQ	00	01	11	10
00	0	4	12	8
01	1	5	13	9
11	3	7	15	11
10	2	6	14	10

$$Q^+ = TQ' + T'QS + T'QR' + T'SR' = TQ' + T'[Q(S + R') + SR']$$

9. (b)

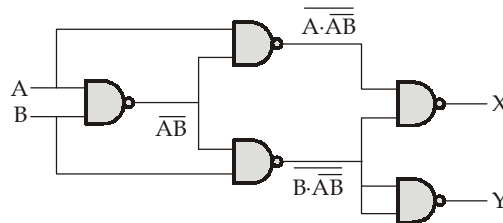
- (i) $x > y$
- (ii) $x > 6$

$$x = 8, y = 7$$

$$(673)_8 + (54)_8 = (487)_{10}$$

$$(443)_{10} + (44)_{10} = (487)_{10}$$

10. (c)



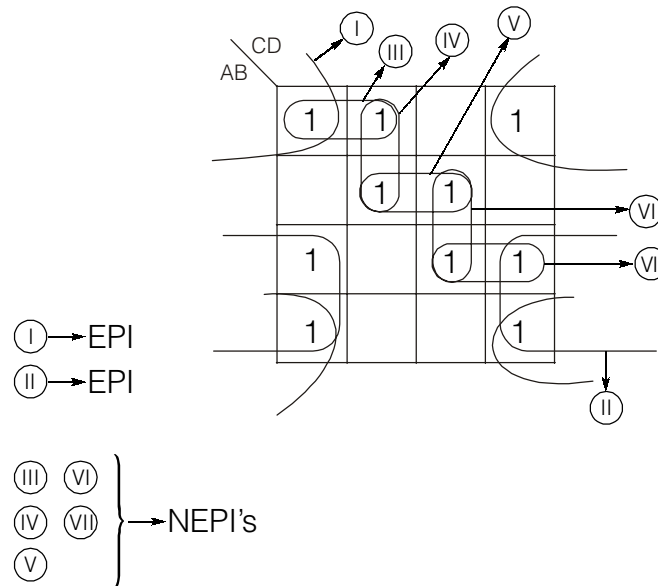
$$X = \bar{B}(A + B) + \bar{A}(A + B) = A\bar{B} + \bar{A}B = A \oplus B$$

$$Y = B(\bar{A}B) = B(\bar{A} + \bar{B}) = \bar{A}B$$

The above circuit represents a half subtractor constructed using only NAND gates. Thus the truth table can be written as

A	B	Difference (X)	Difference (Y)
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

11. (a)



EPI = Essential Prime Implicant [which cover a minterm not covered by any other prime implicants]
 NEPI = Non Essential Prime Implicant. Number of EPI's = 2, number of NEPI's = 5.

12. (a)

$$Y = \bar{S}_1\bar{S}_0(I_0) + \bar{S}_1S_0(I_1) + S_1\bar{S}_0(I_2) + S_1S_0(I_3)$$

$$I_0 = I_3 = S_1$$

$$I_1 = I_2 = S_0$$

⇒

$$Y = \frac{\bar{S}_1\bar{S}_0(S_1)}{0} + \bar{S}_1S_0(S_0) + \frac{S_1\bar{S}_0(S_0)}{0} + S_1S_0(S_1)$$

$$Y = \bar{S}_1S_0 + S_1S_0$$

- $S_0 = B, S_1 = A$

$$Y = \bar{A}B + AB = (\bar{A} + A)B = B$$

- $S_0 = A, S_1 = \bar{B}$

$$Y = \bar{\bar{B}}A + \bar{B}A = BA + \bar{B}A = A(B + \bar{B}) = A$$

- $S_0 = \bar{A}, S_1 = B$

$$Y = \bar{\bar{A}}B + \bar{A}B = \bar{A}B + \bar{A}B = \bar{A}(B + \bar{B}) = \bar{A}$$

- $S_0 = \bar{A}, S_1 = \bar{B}$

$$Y = \bar{\bar{A}}\bar{\bar{B}} + \bar{\bar{A}}\bar{B} = \bar{A}\bar{B} + \bar{B}\bar{A} = \bar{A}(\bar{B} + \bar{B}) = \bar{A}$$

Hence option (a) is the correct answer.

13. (a)

For every combination of x, y, z the function value remains same for input \bar{x}, y, \bar{z} .

x	y	z	$f(x, y, z) = f(\bar{x}, y, \bar{z})$
0	0	0	} either 0 or 1
1	0	1	
0	0	1	} either 0 or 1
1	0	0	
0	1	0	} either 0 or 1
1	1	1	
0	1	1	} either 0 or 1
1	1	0	

Effectively there are only four rows for the truth table of the function $f(x, y, z)$.

\therefore Total Boolean expressions possible is $2^4 = 16$.

14. (d)

$$(a) \quad \overline{(\bar{A}B + \bar{C})}(A + C) = (A + \bar{B})C$$

$$(A + \bar{B}) \cdot C \cdot (A + C) = (A + \bar{B})C$$

$$(AC + \bar{B}C)(A + C) = (A + \bar{B})C$$

$$AC + A\bar{B}C + \bar{B}C = (A + \bar{B})C$$

$$AC + \bar{B}C = (A + \bar{B})C$$

$$(A + \bar{B})C = (A + \bar{B})C \quad \therefore \text{True}$$

$$(b) \quad \overline{(A + \bar{B} + \bar{C})(A + \bar{B}C)} = \bar{A}(B + \bar{C})$$

$$(\bar{A}BC) + \bar{A}(B + \bar{C}) = \bar{A}B + \bar{A}\bar{C}$$

$$\bar{A}BC + \bar{A}B + \bar{A}\bar{C} = \bar{A}B + \bar{A}\bar{C}$$

$$\bar{A}B(C + 1) + \bar{A}\bar{C} = \bar{A}B + \bar{A}\bar{C}$$

$$\bar{A}\bar{C} + \bar{A}B = \bar{A}B + \bar{A}\bar{C} \quad \therefore \text{True}$$

$$(c) \quad (A + \bar{A}\bar{B}\bar{C})B + \bar{A}B = BA + \bar{A}B$$

$$(A + \bar{B}\bar{C})B + \bar{A}B = (A + \bar{A})B$$

$$AB + \bar{A}B = B$$

$$B(A + \bar{A}) = B$$

$$B = B \quad \therefore \text{True}$$

So, all the expression are correct.

15. (b)

$$I_1 = Q_1 \oplus Q_0$$

$$I_0 = Q_3 \odot Q_2$$

Clock	Q ₃	Q ₂	Q ₁	Q ₀	I ₁	I ₀	Y ₂
	0	0	0	0	0	1	0
1	0	0	0	1	1	1	0
2	0	0	1	0	1	1	0
3	0	0	1	1	0	1	0
4	0	1	0	0	0	0	0
5	0	1	0	1	1	0	1
6	0	1	1	0	1	0	1
7	0	1	1	1	0	0	0
8	1	0	0	0	0	0	0
9	1	0	0	1	1	0	1
10	0	0	0	0	0	1	0

Since, in 10 clock cycle y_2 is 1 for 3 clock cycles.

16. (c)

Let the output of XNOR gate is Y

$$Y = (Q_3 \oplus Q_1 \oplus Q_0) \odot Q_5$$

CLK	Y	Q ₅	Q ₄	Q ₃	Q ₂	Q ₁	Q ₀
-		1	0	0	0	0	0
1	0	0	1	0	0	0	0
2	1	1	0	1	0	0	0
3	1	1	1	0	1	0	0
4	0	0	1	1	0	1	0
5	1	1	0	1	1	0	1

Minimum five clock pulses are required to get the sequence 101101

17. (c)

For MOD - 10 counter

$$X = \text{Johnson counter required} = 5 \text{ FF's}$$

$$Y = \text{ring counter required} = 10 \text{ FF's}$$

$$Z = \text{ripple counter required} = 4 \text{ FF's}$$

$$X + Y + Z = 5 + 10 + 4 = 19 \text{ FF's}$$

18. (d)

$$S(J, K, Q_n) = J\bar{Q}_n$$

$$R(J, K, Q_n) = KQ_n$$

So, option (d) matches correct as per equation.

19. (a)

J-K flip-flop will change for every clock pulse. Mod-3 counter will change whenever Q is changing from 0 to 1 because it is ripple counter.

CLK	Q	A	B
	0	0	0
1	1	1	1
2	0	1	1
3	1	0	1
4	0	0	1
5	1	1	0

20. (b)

$$\left. \begin{aligned} S_1 &= C \\ S_0 &= A \end{aligned} \right\}$$

$$E = C$$

$$I_0 = B \oplus D$$

$$I_1 = 1$$

$$I_2 = \bar{D}$$

$$I_3 = BD$$

Mux output is

$$Y = [\bar{S}_1 \bar{S}_0 I_0 + \bar{S}_1 S_0 I_1 + S_1 \bar{S}_0 I_2 + S_1 S_0 I_3] \bar{E}$$

Substituting the values

$$\begin{aligned} f(A, B, C, D) &= [\bar{C}\bar{A}(B \oplus D) + \bar{C}A(1) + C\bar{A}(\bar{D}) + CA(BD)] \bar{C} \\ &= \bar{C}\bar{A}(B \oplus D + \bar{C}A + \underbrace{C\bar{C}\bar{A}\bar{D}}_0 + \underbrace{CCABD}_0) \\ &= \bar{C}\bar{A}(\bar{B}D + B\bar{D}) + \bar{C}A \\ &= \bar{A}\bar{B}\bar{C}D + \bar{A}B\bar{C}\bar{D} + A\bar{C} \\ &\quad \quad \quad 1 \quad \quad 4 \quad (8,9,12,13) \\ &= \sum m(1, 4, 8, 9, 12, 13) \end{aligned}$$

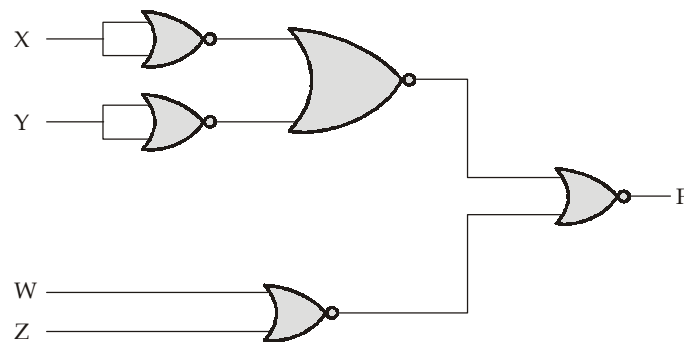
21. (c)

$$F = \bar{X}Z + \bar{X}W + \bar{Y}Z + \bar{Y}W$$

K-map

		WZ			
		00	01	11	10
XY	00	0	1	1	1
	01	0	1	1	1
	11	0	0	0	0
	10	0	1	1	1

$$F = (\bar{X} + \bar{Y})(W + Z)$$



Total 5 NOR gates are required.

22. (b)

Given, Input frequency = 640 kHz

$$\text{Output frequency after 4-bit ring counter} = \frac{640}{4} = 160 \text{ kHz}$$

$$\text{Output frequency after 4-bit Johnson counter} = \frac{160}{8} = 20 \text{ kHz}$$

$$\text{Output frequency after decade counter} = \frac{20}{10} = 2 \text{ kHz}$$

23. (b)

Number of flip-flops for mod-8 ripple counter = 3

$$\text{Maximum clock frequency} = f = \frac{1}{T}$$

$$\Rightarrow 4 \text{ MHz} = \frac{1}{3 \times x \text{ ns}} \text{ Hz}$$

$$\Rightarrow 4 \times 10^6 \text{ Hz} = \frac{10^9}{3 \times x} \text{ Hz}$$

$$\Rightarrow x = \frac{10^9}{4 \times 10^6 \times 3} = \frac{10^3}{12} = 83.33$$

24. (d)

Let,

$$\begin{array}{r}
 A = \quad \quad \quad a_2 \quad \quad a_1 \quad \quad a_0 \\
 B = \quad \quad \quad \quad \quad b_1 \quad \quad b_0 \\
 \hline
 A \times B = \quad \quad a_2b_0 \quad a_1b_0 \quad a_0b_0 \\
 \quad \quad \quad b_1a_2 \quad b_1a_1 \quad b_1a_0 \quad \downarrow \\
 \hline
 \quad \quad \quad b_1a_2 \quad (a_2b_0 + a_1b_1) \quad (a_1b_0 + b_1a_0) \quad a_0b_0 \\
 \quad \quad \quad C_3 \quad \quad C_2 \quad \quad C_1 \quad \quad C_0
 \end{array}$$

Number of AND gates required X = 6

Number of one bit full adders required Y = 3

$$X + Y = 6 + 3 = 9$$

25. (d)

Present state (Q_n)	Input (Y)	Next state (Q_{n+1})
0	1	0
0	0	1
1	1	0
1	0	0

$$Q_{n+1} = \overline{Q_n + Y}$$

26. (b)

Addend will be = 1010

$$\begin{aligned} S_3 S_2 S_1 S_0 &= 1010 + A_3 A_2 A_1 A_0 + C_{in} \\ &= 1010 + 1001 \\ &= 0011 \quad (C_4 = 1) \end{aligned}$$

$$AB = 00$$

and $E = C_4 = 1$

So, $Y = 1$

27. (d)

Given that,

$$D_A = Q_{B'}$$

$$J_B = Q_{C'}$$

$$K_B = \overline{Q_{C'}}$$

$$D_C = Q_C \odot Q_A$$

So, the state table is

Clock	Present state			Next state			D_A	J_B	K_B	D_C
	Q_A	Q_B	Q_C	Q_A	Q_B	Q_C				
1	1	1	0	1	0	0	1	0	1	0
2	1	0	0	0	0	0	0	0	1	0
3	0	0	0	0	0	1	0	0	1	1
4	0	0	1	0	1	0	0	1	0	0
5	0	1	0	1	0	1	1	0	1	1
6	1	0	1	0	1	1	0	1	0	1

Hence 6 clock pulses are required.

28. (a)

$$\text{Decimal input} = 89$$

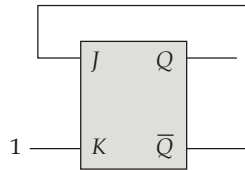
$$\text{BCD} = 1000 \ 1001$$

$$\text{Gray code output} = 11001101$$

$$\text{Select lines } (S_{n-1} \dots S_1 S_0) = (11001101)_2 = 205$$

Y_{out} corresponds to I_m so the $m = 205$.

29. (c)



	J	K	Q	\bar{Q}
			0	1
1	1	1	1	0
2	0	1	0	1
3	1	1	1	0
4	0	1	0	1
5	1	1	1	0
6	0	1	0	1

The output Q will be 101010.

30. (a)

The total delay for synchronous series counter

$$= t_{pd} \text{ (of FF)} + (n - 2) t_{pd} \text{ (of AND gate)}$$

where n = Number of flip-flops

As $M \leq 2^n$ (Where M = modulus)

So, $256 \leq 2^n$

$$n = 8$$

$$\text{Total delay} = 25 + (8 - 2) 5$$

$$= 25 + 30 = 55 \text{ nsec}$$

So, the maximum frequency of MOD-256 counter will be

$$= \frac{1}{55 \text{ nsec}} = 18.18 \text{ MHz}$$

