



**MADE EASY**

Leading Institute for IES, GATE & PSUs

Delhi | Bhopal | Hyderabad | Jaipur | Pune

Web: [www.madeeasy.in](http://www.madeeasy.in) | E-mail: [info@madeeasy.in](mailto:info@madeeasy.in) | Ph: 011-45124612

# ANALOG ELECTRONICS

## ELECTRONICS ENGINEERING

Date of Test : 30/06/2026

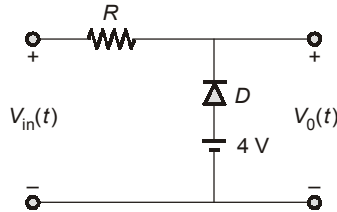
### ANSWER KEY >

- |        |         |         |         |         |
|--------|---------|---------|---------|---------|
| 1. (b) | 7. (a)  | 13. (a) | 19. (b) | 25. (c) |
| 2. (b) | 8. (d)  | 14. (b) | 20. (d) | 26. (b) |
| 3. (b) | 9. (b)  | 15. (c) | 21. (b) | 27. (b) |
| 4. (d) | 10. (b) | 16. (d) | 22. (b) | 28. (c) |
| 5. (a) | 11. (c) | 17. (a) | 23. (a) | 29. (b) |
| 6. (a) | 12. (b) | 18. (a) | 24. (d) | 30. (a) |

**DETAILED EXPLANATIONS**

1. (b)

The circuit can be redrawn as



**Case (I):** when  $V_{in}(t) > 4\text{ V}$

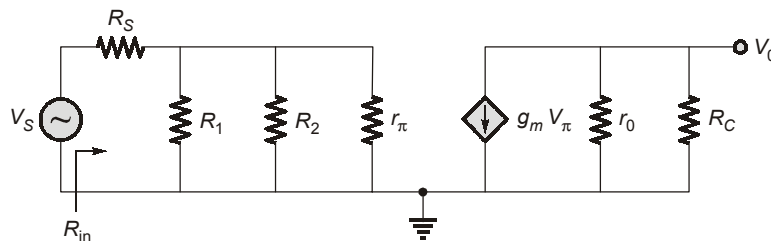
The diode  $D$  will be in OFF state and  $V_{in}(t) = V_0(t)$ .

**Case (II):** when  $V_{in}(t) < 4\text{ V}$

The diode  $D$  will be in ON state and  $V_{out}(t) = 4\text{ V}$ .

2. (b)

By drawing the small signal equivalent model of the transistor by deactivating all the supply voltages, we get,



Now, the resistance seen by the source is equal to,

$$R_{in} = R_s + (R_1 \parallel R_2 \parallel r_{\pi})$$

$$r_{\pi} = 2.74\text{ k}\Omega \quad (\text{given})$$

Thus,

$$R_{in} = 0.5 \times 10^3 + (2.74\text{ k} \parallel 93.7\text{ k} \parallel 6.3\text{ k})$$

$$= (0.5 + 1.87) \times 10^3 \Omega = 2.37\text{ k}\Omega$$

3. (b)

The current through base resistor,

$$I_B = I_1 - 1\text{ mA}$$

$$= \frac{6}{3\text{ k}} - 1\text{ mA} = 1\text{ mA}$$

Apply KVL in base circuit,

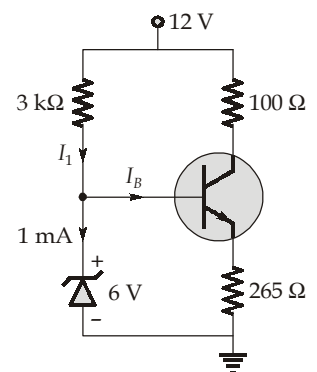
$$-6 + 0.7 + 265(1 + \beta)I_B = 0$$

$$265(1 + \beta)I_B = 5.3$$

$$(1 + \beta) = \frac{5.3}{265 \times 10^{-3}}$$

$$1 + \beta = \frac{5.3}{0.265}$$

$$\beta = 20 - 1 = 19$$



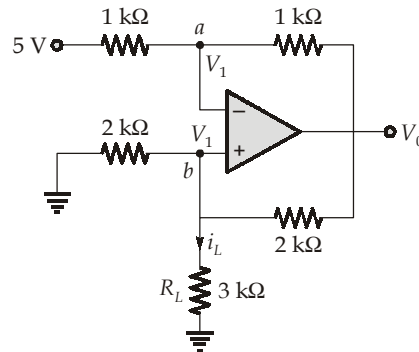
4. (d)

$$I_{D1} = I_{D2} = K_n (V_{GS} - V_t)^2$$

$$I_D = \frac{\mu_n C_{ox}}{2} \cdot \frac{W}{L} (V_{GS} - V_t)^2$$

$$= 0.1 (5 - 2)^2 = 0.9 \text{ mA}$$

5. (a)



Apply KCL at node 'a'

$$\frac{5 - V_1}{1} = \frac{V_1 - V_0}{1}$$

$$5 - V_1 = V_1 - V_0$$

$$-V_0 = 5 - 2V_1$$

$$V_0 = 2V_1 - 5 \quad \dots(i)$$

Apply KCL at node 'b'

$$\frac{V_1}{2} + \frac{V_1}{3} + \frac{V_1 - V_0}{2} = 0$$

$$V_1 \left[ \frac{1}{2} + \frac{1}{3} + \frac{1}{2} \right] = \frac{V_0}{2}$$

$$V_1 \left[ \frac{4}{3} \right] = \frac{V_0}{2}$$

$$V_1 = \frac{3}{8} V_0 \quad \dots(ii)$$

From equation (i) and (ii), we get

$$V_1 = \frac{3}{8} (2V_1 - 5)$$

$$8V_1 = 6V_1 - 15$$

$$2V_1 = -15$$

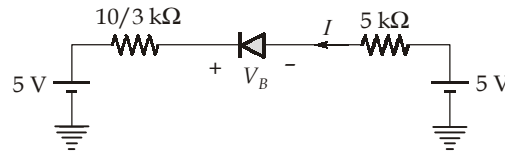
$$V_1 = -7.5 \text{ Volt}$$

Load current,

$$i_L = \frac{V_1}{3K} = \frac{-7.5}{3K} = -2.5 \text{ mA}$$

6. (a)  
The PIV rating of full-wave rectifier with centre tap is  $2 V_m = 2 \times 100 = 200 \text{ V}$

7. (a)  
Drawing the Thevenin equivalent circuit, we get



Applying KVL we get  $V_D = 0 \text{ V}$ , thus no current will flow through the diode  $D_1$ .  
Hence,  $I = 0 \text{ A}$

8. (d)  
BJTs can supply more current than MOSFETs because the channel formed in the MOS is smaller than the channel in BJTs.

9. (b)

10. (b)

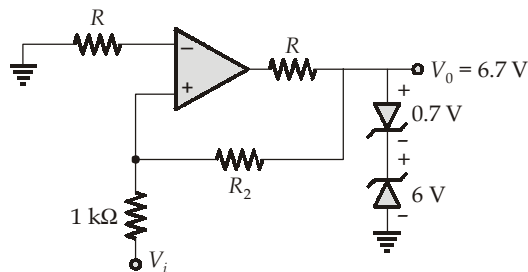
11. (c)

Voltage gain,

$$\frac{V_0}{V_{in}} \approx \frac{-h_{fe} \cdot R_C}{h_{ie}}$$

$$A_V \approx \frac{-150 \times 3 \text{ k}\Omega}{3 \text{ k}\Omega} \approx -150$$

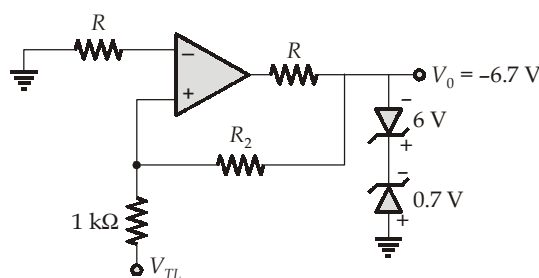
12. (b)  
At upper Threshold point,



$$\therefore \frac{R_2 V_{TH} + 6.7(1)}{R_2 + 1} = 0$$

$$V_{TH} = \frac{-6.7}{R_2}$$

At lower Threshold point,



$$\frac{R_2 V_{TL} - 6.7(1)}{R_2 + 1} = 0$$

$$V_{TL} = \frac{6.7}{R_2}$$

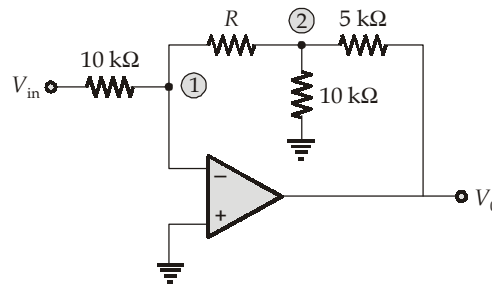
Given that,

$$|V_{TH} - V_{TL}| = 2$$

$$\frac{13.4}{R_2} = 2$$

$$R_2 = 6.7 \text{ k}\Omega$$

13. (a)



$$V_1 = 0$$

Apply KCL at node-1

$$\frac{V_{in} - 0}{10} = \frac{0 - V_2}{R}$$

$$-\left[\frac{V_{in}}{10} \times R\right] = V_2 \quad \dots(i)$$

Apply KCL at node-2

$$\frac{V_2}{R} + \frac{V_2}{10} + \frac{V_2 - V_0}{5} = 0$$

$$V_2 \left[ \frac{1}{R} + \frac{1}{10} + \frac{1}{5} \right] = \frac{V_0}{5} \quad \dots(ii)$$

From equation (i) and (ii), we get

$$\frac{-V_{in} \cdot R}{10} \left[ \frac{1}{R} + \frac{3}{10} \right] = \frac{V_0}{5}$$

$$\frac{R}{10} \left[ \frac{10 + 3R}{10R} \right] = \frac{-V_0}{V_{in}} \times \frac{1}{5}$$

$$\frac{10 + 3R}{20} = \left( \frac{-V_0}{V_{in}} \right)$$

Given that,

$$\frac{V_0}{V_{in}} = -6$$

$$\frac{10 + 3R}{20} = 6$$

$$10 + 3R = 120$$

$$R = \frac{110}{3} \text{ k}\Omega$$

$$R = 36.66 \text{ k}\Omega$$

14. (b)

**Case I :** When  $V_{in} < 0 \text{ V}$

When  $V_{input} < 0 \text{ V}$ , then the diode  $D_1$  will be in forward biased and diode  $D_2$  will be OFF, hence the output is equal to 0 V, which is shown in figure-1.

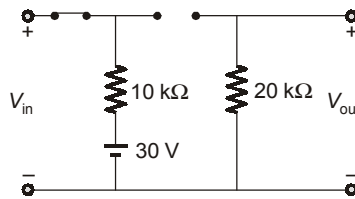


Figure (1)

**Case II :**  $0 < V_{in} < 20 \text{ V}$

$D_1$  is ON and  $D_2$  is ON.

The equivalent circuit is shown in figure (2).

From the figure it is clear that the output

$$V_{out} = V_{in}$$

Thus it will be a straight line when plotted in the transfer curve [part (2)].

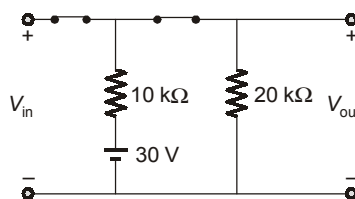


Figure (2)

**Case III :** For  $V_{input} > 20 \text{ V}$

$D_1 = \text{OFF}$  and  $D_2 = \text{ON}$

Thus, the output will be a constant voltage  $V_{out}$ .

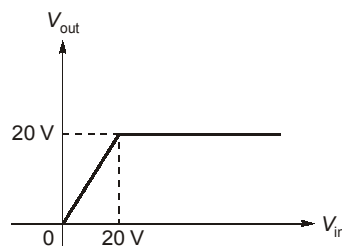
$$V_{out} = \frac{20}{20 + 10} \times 30 \text{ V}$$

( $\because$  voltage division)

Thus,

$$V_{out} = 20 \text{ V}$$

Hence, the output response can be drawn as



15. (c)

Now,  
and

$$I_{in} = I_{D1} + I_{D2}$$

$$V_{D1} = V_{D2}$$

(∵ diodes are in parallel)

thus, 
$$V_T \ln\left(\frac{I_{D1}}{I_{s1}}\right) = V_T \ln\left(\frac{I_{D2}}{I_{s2}}\right)$$

⇒ 
$$\frac{I_{D1}}{I_{s1}} = \frac{I_{D2}}{I_{s2}}$$

$$I_{D1} = \left(\frac{I_{D2}}{I_{s2}}\right) \cdot I_{s1}$$

Now, 
$$I_{in} = I_{D1} + I_{D2} = I_{D2} \left(\frac{I_{s1}}{I_{s2}} + 1\right)$$

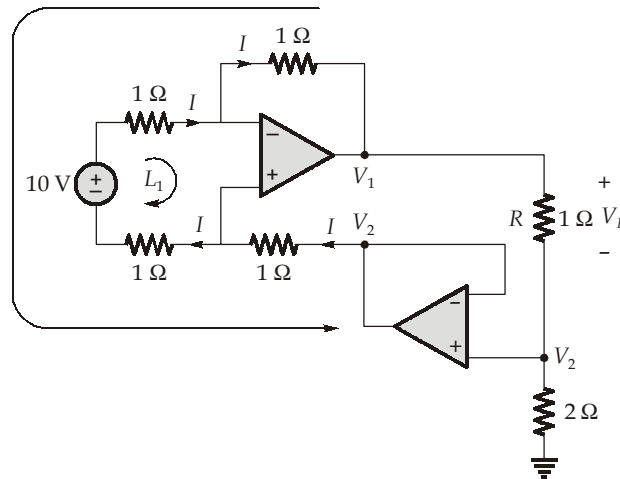
$$I_{in} = \left(1 + \frac{I_{s1}}{I_{s2}}\right) I_{D2}$$

⇒ 
$$I_{D2} = \frac{I_{in}}{1 + \frac{I_{s1}}{I_{s2}}}$$

Now,  $I_{s1}$  and  $I_{s2}$  are reverse saturation currents of the diodes and  $I_s \propto A$ . Thus the above equation can be written as,

$$I_{D2} = \frac{I_{in}}{1 + \frac{I_{s1}}{I_{s2}}} = \left(\frac{I_{in}}{1 + \frac{A_1}{A_2}}\right)$$

16. (d)



Apply KVL in loop-1,

$$\begin{aligned} -10 + I + I &= 0 \\ 2I &= 10 \\ I &= 5 \text{ A} \end{aligned}$$

Applying KVL in the loop shown,

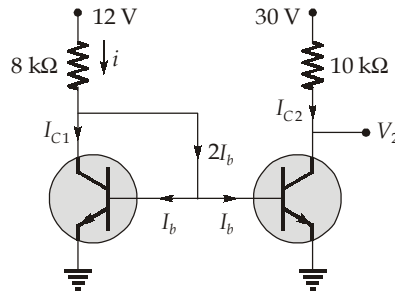
we get, 
$$V_1 = -5 - 5 + 10 - 5 - 5 + V_2$$

$$V_1 - V_2 = -10 \text{ V}$$

∴ voltage across resistor,

$$R = V_R = V_1 - V_2 = -10 \text{ V}$$

17. (a)



$$12 - i \times 8 \times 10^3 - 0.7 = 0$$

Now,

$$i = \frac{12 - 0.7}{8 \times 10^3} = 1.4125 \text{ mA}$$

$$i = I_{c1} + 2I_b = (\beta + 2)I_b$$

$$I_b = \frac{i}{\beta + 2} = \frac{1.4125}{202} = 6.99 \text{ } \mu\text{A} \approx 7 \text{ } \mu\text{A}$$

$$I_{c2} = 200I_b = 200 \times 7 \text{ } \mu\text{A} = 1.4 \text{ mA}$$

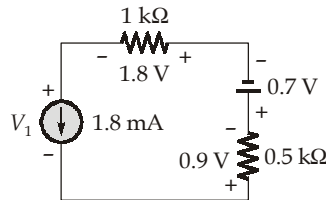
∴

$$V_2 = 30 - I_{c2} \times 10k$$

$$V_2 = 30 - 1.4 \times 10 = 16 \text{ V}$$

18. (a)

From the circuit given, after observation, we can conclude that  $D_2$  will be ON and  $D_1$  will be OFF.



∴

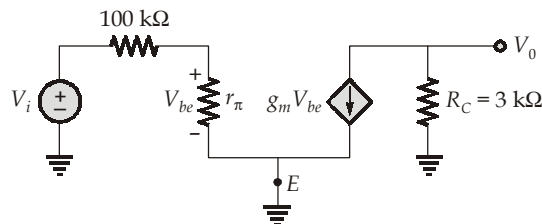
$$V_1 = -0.9 - 0.7 - 1.8 = -3.4 \text{ V}$$

19. (b)

The first step in the analysis consists of determining the quiescent operating point. For this purpose we assume that  $V_i = 0$ .

∴

$$I_B = \frac{V_{BB} - 0.7}{100k} = \frac{3 - 0.7}{100k} = 23 \text{ } \mu\text{A}$$



∴

$$I_C = \beta I_B = 100 \times 23 \text{ } \mu\text{A} = 2.3 \text{ mA}$$

$$V_C = 10 - I_C \cdot R_C$$

$$= 10 - 2.3 \times 3 = 3.1 \text{ V}$$

$$r_e = \frac{V_T}{I_E} = \frac{25 \text{ mV}}{(2.3 / 0.99) \text{ mA}} = 10.8 \Omega$$

$$g_m = \frac{I_C}{V_T} = \frac{2.3 \text{ mA}}{25 \text{ mV}} = 92 \text{ mA/V}$$

$$r_\pi = \frac{\beta}{g_m} = \frac{100}{92} = 1.09 \text{ k}\Omega$$

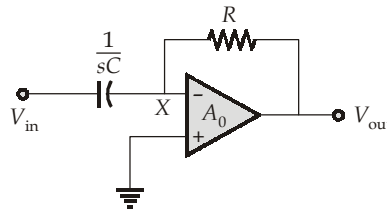
$$\therefore V_{be} = V_i \times \frac{r_\pi}{r_\pi + R_{BB}}$$

$$V_{be} = V_i \times \frac{1.09}{101.09} = 0.011 V_i$$

$$\begin{aligned} \therefore V_0 &= -g_m V_{be} R_C \\ &= -92 \times 0.011 V_i \times 3 \\ &= -3.04 V_i \end{aligned}$$

$$\therefore A_V = \frac{V_0}{V_i} = -3.04 \approx -3$$

20. (d)



Applying KCL at node 'X', we get,

$$\frac{V_{in} - V_x}{1/sC} = \frac{V_x - V_{out}}{R_1}$$

$$\text{now, } \frac{-V_{out}}{A_0} = V_x$$

$$\therefore \frac{-V_{out}}{V_{in}} = \frac{-RCs}{1 + \frac{1}{A_0} + \frac{sRC}{A_0}}$$

$$\frac{s_p RC}{A_0} + \frac{1}{A_0} + 1 = 0$$

$$\frac{s_p RC}{A_0} = -1 - \frac{1}{A_0}$$

$$\text{Pole, } s_p = \frac{-(1 + A_0)}{RC}$$

Hence option (d) is correct.

21. (b)

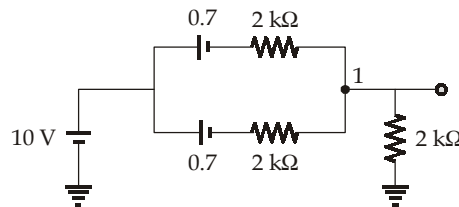
$$A_{CL} = \frac{A_{OL}}{1 + A_{OL}\beta} = \frac{\frac{A_0}{(1 + j\omega/\omega_0)}}{1 + \frac{A_0}{\left(1 + \frac{j\omega}{\omega_0}\right)} \cdot \beta} = \frac{A_0}{1 + j\frac{\omega}{\omega_0} + A_0\beta}$$

$$= \frac{\frac{A_0}{1 + A_0\beta}}{1 + j\frac{\omega}{\omega_0(1 + A_0\beta)}} = \frac{A'_{CL}}{1 + j\frac{\omega}{\omega'_0}}$$

$$\therefore \omega'_0 = \omega_0(1 + A_0\beta)$$

22. (b)

The above circuit can be represented as,



Applying KCL at node 1,

$$\frac{V_0}{2k} + \frac{V_0 - 10 + 0.7}{2k} + \frac{V_0 - 10 + 0.7}{2k} = 0$$

$$V_0 \left[ \frac{3}{2k} \right] = \frac{9.3}{1k}$$

$$V_{out} = \frac{9.3}{3} \times 2 = 6.2 \text{ V}$$

23. (a)

The output voltage of differential amplifier is given as,

$$V_0 = A_d V_d + A_c V_c$$

Where,

$A_d$  = Differential gain

$A_c$  = Common mode gain

$V_d$  = Differential input voltage =  $V_1 - V_2$

$V_c$  = Common mode input voltage =  $\frac{V_1 + V_2}{2}$

$$V_0 = A_d V_d \left[ 1 + \frac{A_c V_c}{A_d V_d} \right] = A_d V_d \left[ 1 + \frac{1}{\rho} \cdot \frac{V_c}{V_d} \right]$$

Where,

$$\rho = \frac{A_d}{A_c} = \text{common mode rejection ratio}$$

Set of signal 1,

$$V_d = 50 \mu\text{V} - (-50 \mu\text{V}) = 100 \mu\text{V}$$

$$V_c = \frac{50 \mu\text{V} - 50 \mu\text{V}}{2} = 0$$

$$V_{01} = 100\mu\text{V} A_d [1 + 0] = 100 A_d \mu\text{V}$$

$$V_c = \frac{1050\mu\text{V} + 950\mu\text{V}}{2} = 1000\mu\text{V}$$

$$V_d = 1050\mu\text{V} - 950\mu\text{V} = 100\mu\text{V}$$

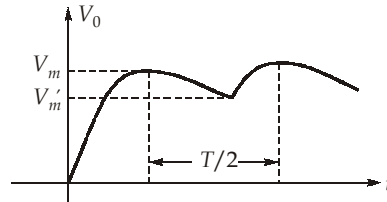
$$\therefore V_{02} = A_d 100\mu\text{V} \left[ 1 + \frac{1}{100} \times \frac{1000\mu\text{V}}{100\mu\text{V}} \right] = 110 A_d \mu\text{V}$$

$$\% \text{ difference} = \frac{V_{02} - V_{01}}{V_{01}} \times 100 = \frac{110 - 100}{100} \times 100 = 10\%$$

24. (d)

$$V_{\max} = \sqrt{2} \times 220 = 311.12 \text{ V}$$

Since output is a rectified wave we have,



$$V'_m = V_m \left( 1 - \frac{T}{2RC} \right)$$

$$V_m - V'_m = \frac{V_m T}{2RC}$$

$$\text{ripple} = V_m - V'_m = \frac{V_m T}{2RC}$$

Peak to peak ripple voltage,

$$= 0.01 \times V_{\max}$$

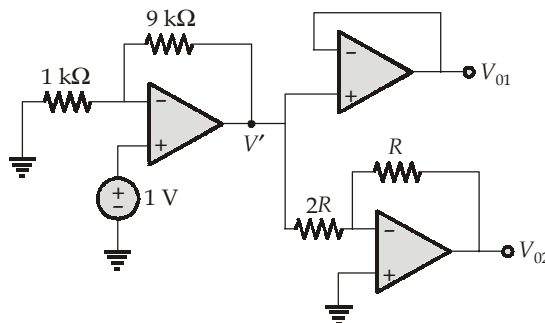
$$= 0.01 \times 311.12$$

$$\text{ripple} = 3.11$$

$$3.11 = \frac{311.12}{2 \times 50 \times 10 \times 10^3 \times C}$$

$$C = 100 \mu\text{F}$$

25. (c)



$$V' = \left(1 + \frac{9 \text{ k}\Omega}{1 \text{ k}\Omega}\right) \times 1 \text{ V} \quad (\because \text{non-inverting amplifier})$$

$$V' = 10 \text{ V}$$

now,

$$V_{01} = V' = 10 \text{ V} \quad (\because \text{it is a voltage buffer})$$

and

$$V_{02} = -\frac{R}{2R} V'$$

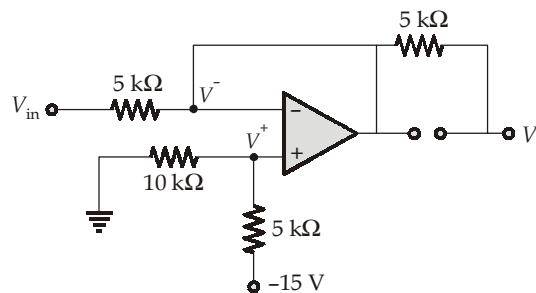
( $\because$  inverting amplifier)

$$V_{02} = -\frac{1}{2} V' = -\frac{10 \text{ V}}{2} = -5 \text{ V}$$

$$\therefore V_{02} - V_{01} = -5 \text{ V} - 10 \text{ V} = -15 \text{ V}$$

26. (b)

**Case -I :** When  $V_{in} > -10 \text{ V}$ , then the voltage across diode  $D_1$  is positive so diode  $D_1$  is in ON state, and therefore the equivalent circuit can be drawn as



$$V^+ = -15 \times \frac{10}{15} = -10 \text{ V}$$

Due to virtual ground,

$$V^+ = V^- = -10 \text{ V}$$

and

$$V_0 = V^- = -10 \text{ V}$$

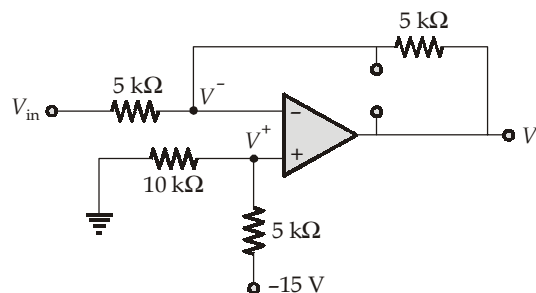
$\therefore$

$$V_0 = -10 \text{ V}$$

**Case -II :** When  $V_{in} < -10 \text{ V}$

$$V_0 = +V_{sat}$$

Thus,



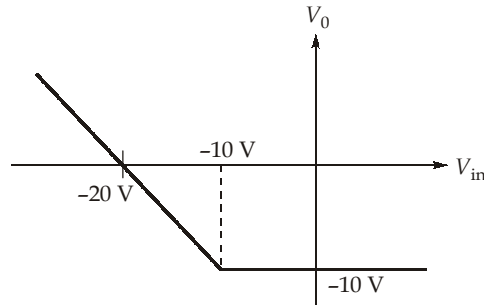
$$\therefore V_0 = -\frac{5}{5} \times V_{in} = -V_{in} \quad (\text{for } V_{in} < -10 \text{ V})$$

Alternately, we can write the equation of the graph by applying KCL at node  $V^-$

$$\therefore V^- = V^+ = -10 \text{ V}$$

$$\frac{-10 - V_{in}}{5 \text{ k}\Omega} + \frac{-10 - V_0}{5 \text{ k}\Omega} = 0$$

$$\begin{aligned} -20 - V_{in} - V_0 &= 0 \\ V_0 &= -V_{in} - 20 \end{aligned}$$



27. (b)

Applying KVL in the circuit shown below, we get,

$$2V_{BE1} = V_{BE3} + I_0 R_E$$

(∵ both the transistor are matched with negligible base current thus  $V_{BE1} = V_{BE2}$  for same  $I_{\text{reff}}$ ).

Now,

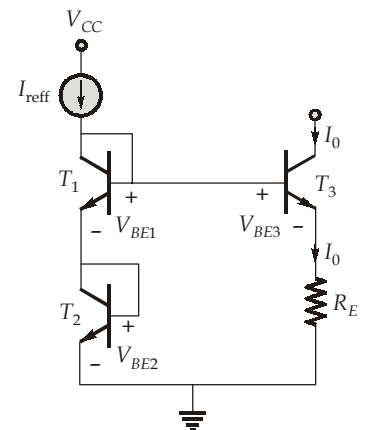
$$V_{BE1} = V_T \ln\left(\frac{I_{\text{reff}}}{I_s}\right)$$

$$V_{BE3} = V_T \ln\left(\frac{I_0}{I_s}\right)$$

$$2V_T \ln\left(\frac{I_{\text{reff}}}{I_s}\right) - V_T \ln\left(\frac{I_0}{I_s}\right) = I_0 R_E$$

$$V_T \ln\left(\frac{I_{\text{reff}}^2}{I_0 I_s}\right) = I_0 R_E$$

$$R_E = \frac{V_T}{I_0} \ln\left(\frac{I_{\text{reff}}^2}{I_0 I_s}\right) = 0.208 \ln\left(\frac{625}{10 \times 120 \times 10^{-3}}\right) = 15.638 \text{ k}\Omega$$



28. (c)

Assuming all the diodes are forward biased,

$$V_B = -0.7 \text{ V}$$

$$V_A = 0 \text{ V}$$

∴

$$I_2 = \frac{10 - 0}{10 \text{ k}} = 1 \text{ mA}$$

and

$$I_1 = \frac{-0.7 - (-10)}{10 \text{ k}} = 0.93 \text{ mA}$$

∴

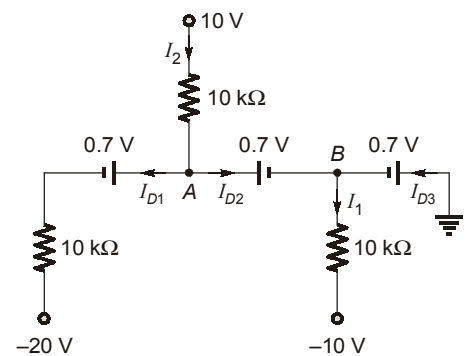
$$I_2 = I_{D1} + I_{D2}$$

and

$$I_1 = I_{D2} + I_{D3}$$

applying KVL in the outer loop, we get,

$$10 \text{ k} I_2 + 0.7 + 10 \text{ k} I_{D1} - 20 = 10$$



$$10 \text{ k}(I_{D_1} + I_{D_2}) + 10 \text{ k}I_{D_1} = 30 - 0.7 = 29.3$$

$$20 \text{ k}I_{D_1} + 10 \text{ k}I_{D_2} = 29.3$$

$$2I_{D_1} + I_{D_2} = 2.93 \text{ mA}$$

...(i)

also,

$$I_{D_1} + I_{D_2} = I_2 = 1 \text{ mA}$$

...(ii)

from (i) and (ii)

$$I_{D_1} = 1.93 \text{ mA and } I_{D_2} = -0.93 \text{ mA}$$

$$\therefore I_{D_2} + I_{D_3} = 0.93 \text{ mA}$$

$$\Rightarrow I_{D_3} = -I_{D_2} + 0.93 \text{ mA} = 1.86 \text{ mA}$$

Here  $I_{D_2}$  is negative, Hence, our assumption is incorrect.

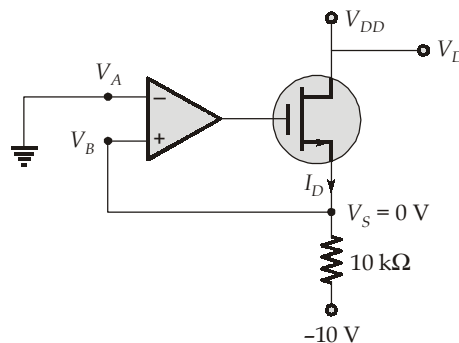
Therefore,  $D_2$  is reverse biased

and  $\therefore I_{D_1}$  and  $I_{D_3}$  are positive,

$D_1, D_3$  are forward biased.

29. (b)

For the transistor



$$V_S = V_B = V_A$$

due to virtual ground,

thus,

$$V_S = 0 \text{ V}$$

Hence,

$$I_D = \frac{0 - (-10)}{10 \times 10^3} = 1 \text{ mA}$$

$$I_D = \frac{\mu_n C_{ox} W}{2L} (V_{GS} - V_T)^2$$

$$\therefore V_{GS} - V_T = \sqrt{\frac{I_D}{\frac{\mu_n C_{ox} W}{2L}}}$$

$$V_{GS} - V_T = \sqrt{\frac{1 \times 10^{-3}}{\frac{0.5 \times 10^{-3}}{2}}}$$

$$V_{GS} - V_T = 2 \text{ V}$$

For the MOSFET to be in saturation region

$$V_{DS} \geq V_{GS} - V_T$$

∴ at the edge of saturation

$$V_{DS} = V_{GS} - V_T = 2 \text{ V}$$

$$\therefore V_S = 0$$

$$\therefore V_D = V_G - V_T$$

$$\Rightarrow V_{DD} = 2 \text{ V}$$

30. (a)

For upper MOSFET,

$$V_{DS} = 8 - V_a$$

$$V_{GS} - V_T = 6 - V_a - 2 = 4 - V_a$$

Upper MOS will be in saturation because

$$V_{DS} > V_{GS} - V_T$$

For lower MOS,

$$V_{DS} = V_a$$

$$V_{GS} - V_T = V_a - 2$$

So,

$$V_{DS} > V_{GS} - V_T$$

Hence both MOS will be in saturation

$$I_D = \mu_n C_{ox} \left( \frac{W}{L} \right) (V_{GS} - V_T)^2$$

$$I_{D1} = \mu_n C_{ox} (9)(4 - V_a)^2$$

$$I_{D2} = \mu_n C_{ox} (4)(V_a - 2)^2$$

But

$$I_{D1} = I_{D2}$$

$$\therefore \mu_n C_{ox} (9)(4 - V_a)^2 = \mu_n C_{ox} (4)(V_a - 2)^2$$

$$\frac{9}{4} = \left( \frac{V_a - 2}{4 - V_a} \right)^2$$

$$\frac{3}{2} = \frac{V_a - 2}{4 - V_a}$$

$$12 - 3V_a = 2V_a - 4$$

$$16 = 5V_a$$

$$V_a = \frac{16}{5} = 3.2 \text{ Volts}$$

