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DIGITAL CIRCUITS

EC-EE

Date of Test : 20/05/2026

ANSWER KEY ➤

1.	(b)	7.	(a)	13.	(d)	19.	(d)	25.	(c)
2.	(d)	8.	(c)	14.	(c)	20.	(a)	26.	(a)
3.	(a)	9.	(b)	15.	(b)	21.	(a)	27.	(a)
4.	(b)	10.	(c)	16.	(c)	22.	(c)	28.	(a)
5.	(d)	11.	(a)	17.	(c)	23.	(a)	29.	(b)
6.	(b)	12.	(a)	18.	(c)	24.	(a)	30.	(d)

DETAILED EXPLANATIONS

1. (b)

$$X = 1010.010$$
$$X + (-Y)$$
$$Y = 0111.111$$

Taking 2's complement of Y

$$\begin{aligned} Y &= 1000.000 \\ &\quad\ \ +1 \\ &\quad\ \ 1000.001 \end{aligned}$$

$$\begin{aligned} X + (-Y) &= 1010.010 \\ &\quad +1000.001 \\ &\quad\ \ 0010.011 \end{aligned}$$

2. (d)

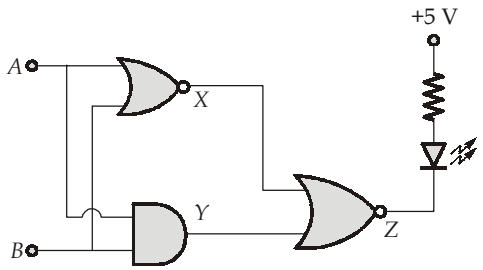
By checking the options, we found that only option (d) meets both the requirements

$$Y = (A \odot B) + C$$

When A and B are same then $Y = 1 + C = 1$.
When A and B are different then $Y = 0 + C = C$.

3. (a)

Bubbled OR Gate is equivalent to NAND Gate and Bubbled AND Gate is equivalent to NOR Gate. Hence, the circuit can be redrawn as



LED will emit light when $Z = 0$.

(i) For $A = 0$, $B = 0$: $X = 1$, $Y = 0$. Hence, $Z = 0$
(ii) For $A = 1$, $B = 0$: $X = 0$, $Y = 0$. Hence, $Z = 1$
(iii) For $A = 0$, $B = 1$: $X = 0$, $Y = 0$. Hence, $Z = 1$
(iv) For $A = 1$, $B = 1$: $X = 0$, $Y = 1$. Hence, $Z = 0$

Therefore, LED emits light for $A = 0$, $B = 0$ and $A = 1$, $B = 1$.

4. (b)

We know that, For dual slope integrating type ADC,

$$\text{analog input, } V_a = \frac{V_R}{2^n} \times N$$

where, $V_a = 5$ V, $V_R = 10$ V, $n = 4$

the equivalent digital number, $N = 2^n \times \dfrac{V_a}{V_R}$

$$N = 2^4 \times \frac{5}{10} = 8 = (1000)_2$$

5. (d)

Clear signal is $\overline{Q_A \cdot Q_D}$

As it is a synchronous clear.

$\therefore$ The counter will get clear on the next positive edge of the clock pulse.

Counter counts states from 0 to 9.

$\therefore$ It is decade counter.

6. (b)

In successive approximation analog to digital converter, the conversion time is independent of input analog voltage.

7. (a)

$$\text{Maximum delay} = \frac{t_{PHL} + t_{PLH}}{2} \cdot n$$

$$= \frac{(22+15)}{2} \times 4 = 37 \times 2 = 74 \text{ nsec}$$

8. (c)

$$F = (A + D)(B \oplus C) + AD'$$

$$F = (A + D)(B'C + BC') + AD'$$

$$F = DB'C + DBC' + AB'C + ABC' + AD'$$

Using redundancy theorem, $XY + \bar{X}Z + YZ = XY + \bar{X}Z$. Hence,

$$D(B'C) + D'A + A(B'C) = DB'C + D'A$$

Therefore, $$F = DB'C + DBC' + D'A + ABC'$$

Again using redundancy theorem,

$$F = DB'C + DBC' + D'A$$

$$F = BC'D + B'CD + AD'$$

9. (b)

$$\bar{Z} = (P + A) \cdot (Q + \bar{A})$$

$$\bar{Z} = PQ + \bar{A}P + AQ$$

We have, $\bar{Z} = \overline{\bar{A} + B} = A \cdot \bar{B}$. Comparing, we get

$$P = 0, \; Q = \bar{B}$$

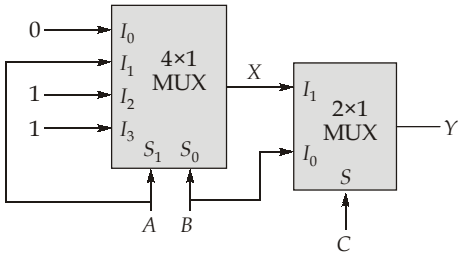
10. (c)

$$(2 \times 2048) + (6 \times 128) + 22 = (2^1 \times 2^{11}) + [(2^2 + 2^1) \times 2^7] + (2^4 + 2^2 + 2^1)$$

$$= 2^{12} + 2^9 + 2^8 + 2^4 + 2^2 + 2^1$$

$$= (1001100010110)_2$$

11. (a)



Let the output of 4 × 1 MUX is X,

$$\therefore \quad X = \bar{S}_1\bar{S}_0 I_0 + \bar{S}_1 S_0 I_1 + S_1\bar{S}_0 I_2 + S_1 S_0 I_3$$

where, $S_1 = A,\ S_0 = B,\ I_1 = A$

$$X = \bar{A}\bar{B}(0) + \bar{A}B(A) + A\bar{B}(1) + AB(1)$$

$$= A\bar{B} + AB$$

$$X = A$$

Output of 2 × 1 MUX, $Y = \bar{S}I_0 + SI_1$

where, $S = C;\ I_1 = X,\ I_0 = B$

$$\therefore \quad Y = \bar{C}B + CX$$

$$Y = \bar{C}B + CA$$

12. (a)

Given, Full scale input voltage

$$V_{FS} = 10 \text{ V}$$

resolution = 5 mV

We know that,

Resolution of ADC, $$R = \frac{V_{FS}}{2^n - 1}$$

$$5 \times 10^{-3} = \frac{10}{2^n - 1}$$

$$2^n - 1 = \frac{10}{5 \times 10^{-3}}$$

$$2^n - 1 = 2000$$

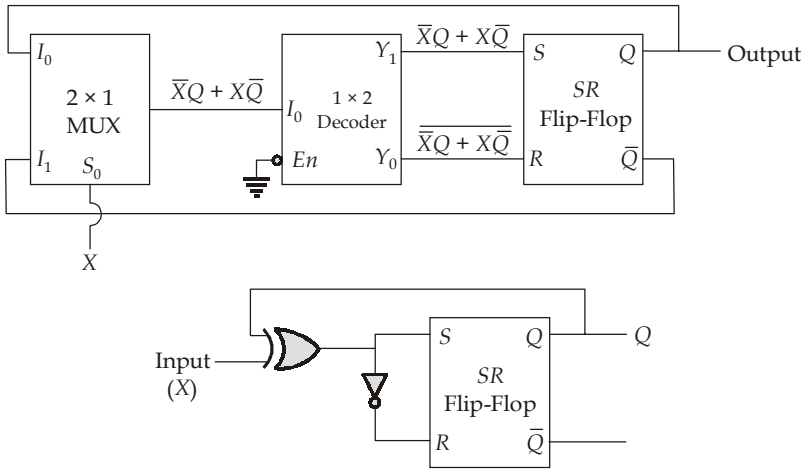
$$2^n = 2001$$

$$n = 11$$

[2 Marks, MCQ]

13. (d)

The MUX in the circuit is working as an EX-OR gate and the 1 × 2 decoder as a NOT gate. Thus the circuit could be redrawn as



Thus, the circuit will function as a T-flip flop

$\because$ $S = X \oplus Q_n$

$R = \overline{X \oplus Q_n}$

For SR-flip flop, $Q_{n+1} = S + \bar{R}Q_n = (Q_n \oplus X) + \overline{(Q_n \oplus X)}Q_n = (X \oplus Q_n)(1 + Q_n)$

$Q_{n+1} = X \oplus Q_n$

Excitation equation for T-flip flop.

14. (c)

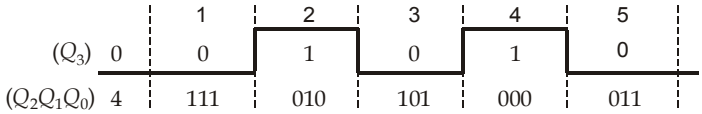
A \ BQ	00	01	11	10
0	0	0	0	0
1	1	1	0	1

$A\bar{B}$ $A\bar{Q}$

$\therefore$ $Q^+ = A\bar{B} + A\bar{Q} = A(\bar{B} + \bar{Q}) = A\overline{BQ}$

15. (b)

Cycles of clock

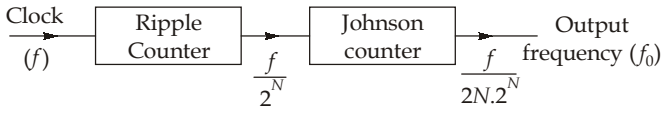


So, value of counter output after five clock pulses will be number of times count has increased from 0 i.e., 2.

16. (c)

D_0	D_1	Q_0	Q_1
$\bar{Q}_0$	$Q_0 \oplus \bar{Q}_1$	0	0
1	1	1	1
0	1	0	1
1	0	1	0
0	0	0	0

17. (c)



$$100 = \frac{32 \times 10^3}{2N \times 2^N}$$

$2N \times 2^N = 32 \times 10$

$2 \times N \times 2^N = 2^5 \times 5 \times 2$

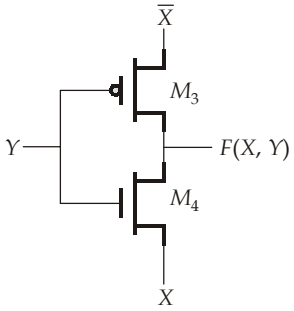
$\therefore$ $N = 5$

Number of flip flops required = N for ripple counter + N for Johnson counter

$5 + 5 = 10$

18. (c)

First stage of the circuit behaves as inverter. Hence, the circuit can be redrawn as below:



X	Y	M_3	M_4	F
0	0	ON	OFF	1
0	1	OFF	ON	0
1	0	ON	OFF	0
1	1	OFF	ON	1

$F = \overline{X}\overline{Y} + XY$

19. (d)

$$F_1 = \overline{A}\overline{C} + \overline{B}C = \overline{A}\overline{C}(B + \overline{B}) + (A + \overline{A})\overline{B}C$$

$$= \overline{A}B\overline{C} + \overline{A}\overline{B}\overline{C} + A\overline{B}C + \overline{A}\overline{B}C$$

$$= \Sigma m(0, 1, 2, 5)$$

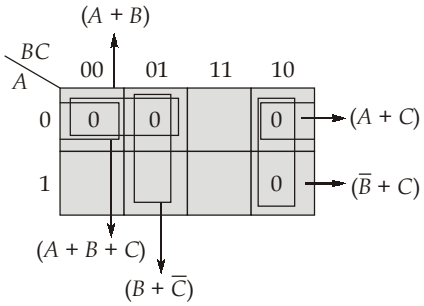
$$F_2 = \overline{A}\overline{B} + B\overline{C} = \overline{A}\overline{B}(C + \overline{C}) + B\overline{C}(A + \overline{A})$$

$$= \overline{A}\overline{B}C + \overline{A}\overline{B}\overline{C} + AB\overline{C} + \overline{A}B\overline{C}$$

$$= \Sigma m(0, 1, 2, 6)$$

Hence, $F' = F_1 + F_2 = \Sigma m(0, 1, 2, 5, 6)$

$$F = \Sigma m(3,4,7) = \pi M(0,1,2,5,6)$$



$$f = (A + B + C)\cdot(B + \overline{C})\cdot(\overline{B} + C)$$

20. (a)

When $F = 0$, the output of latch does not change i.e.,

$$Q^+ = Q$$

When $F = 1$, the latch is in the toggle mode i.e.,

$$Q^+ = \overline{Q}$$

Hence, $$Q^+ = \overline{F}Q + F\overline{Q} = F \oplus Q$$

21. (a)

$$000 \xrightarrow{1^{st}\ CLK} 100 \xrightarrow{2^{nd}\ CLK} 010 \xrightarrow{3^{rd}\ CLK} 101$$

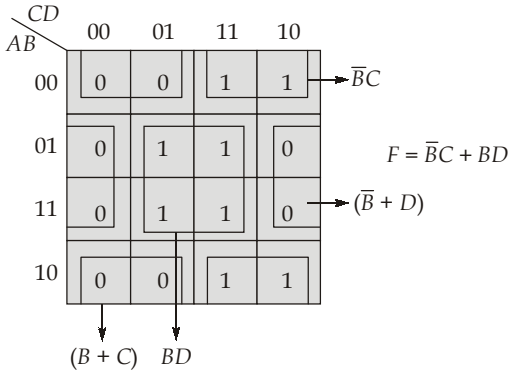
The op-amp circuit is a R-2R Ladder DAC with digital input 101. Therefore,

$$V_0 = -\left(\frac{R_f}{R}\right) \times \left(\frac{V_{ref}}{2^3}\right) \times (\text{Decimal equivalent of } 101)$$

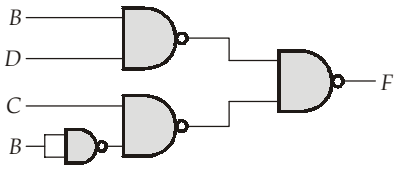
$$V_0 = \frac{-R}{R} \times \frac{5}{8} \times 5$$

$$V_0 = -3.125 \text{ V}$$

22. (c)

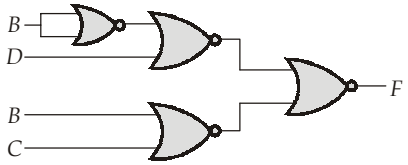


Using NAND Gates,



By grouping 0's in K-Map and writing F in maxterms, we get

$$F = (B+C)\cdot(\bar{B}+D)$$



Therefore, $m + n = 4 + 4 = 8$

23. (a)

There are three data paths (flop A to flop B, flop A to flop C, flop B to flop C). Setup time is used for deriving the maximum clock frequency.

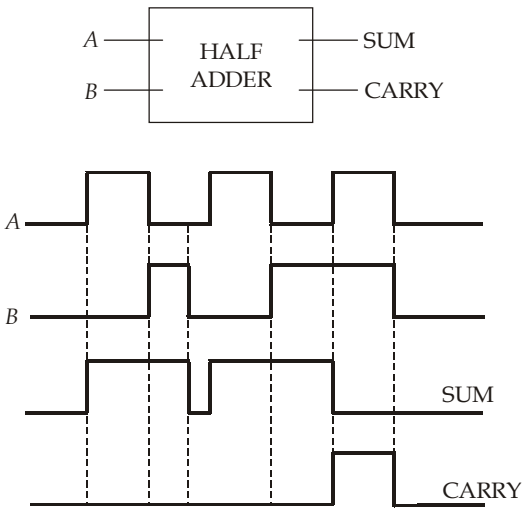
Path $A \to B$: $t_{CLK} > t_{CLK \to Q} + t_s = 9 + 2 \Rightarrow t_{CLK} > 11$ ns

Path $A \to C$: $t_{CLK} > t_{CLK \to Q} + t_s + t_{pd} = 9 + 2 + 4 \Rightarrow t_{CLK} > 15$ ns

$$t_{clk} > 15 \text{ nsec}$$

$$f_{max} = \frac{1}{t_{clk}(\text{min})} = \frac{1}{15 \times 10^{-9}} = 66.67 \text{ MHz}$$

24. (a)



25. (c)

$$\text{Sum, } S = A \oplus B$$

$$\text{Difference} = S \oplus C = A \oplus B \oplus C$$

$$= \overline{(\bar{A}B + A\bar{B})}C + (\bar{A}B + A\bar{B})\bar{C}$$

$$= (\bar{A}\bar{B} + AB)C + (\bar{A}B + A\bar{B})\bar{C}$$

$$= \bar{A}\bar{B}C + ABC + \bar{A}B\bar{C} + A\bar{B}\bar{C}$$

$$\text{Borrow, } B = \bar{S}C$$

$$= (\overline{A \oplus B})C$$

$$= (AB + \bar{A}\bar{B})C$$

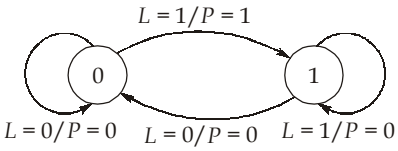
$$= ABC + \bar{A}\bar{B}C$$

$$B = \Sigma m(1, 7)$$

and $$D = \Sigma m(1, 2, 4, 7)$$

26. (a)

Present State	Input	Next State	Output
S	L	S^+	P
0	0	0	0
0	1	1	1
1	0	0	0
1	1	1	0



27. (a)

Clk	Output
0	0 1 1 0
1	0 0 1 1
2	0 0 0 1
3	0 0 0 0

28. (a)

In serial-in/serial-out shift register, one bit of data is shifted one at a time. From Q_0 to Q_3 total 4-bit shifting takes place.

$\therefore$ The time delay between serial input, and the Q_3 output, $d = \dfrac{4}{200\,\text{kHz}} = 20\times10^{-6}\,\text{sec}$.

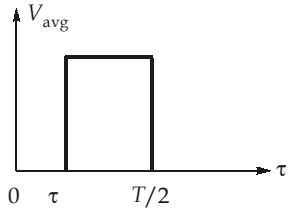
29. (b)

Present state		FF Input		Next state	
Q_1	Q_0	T_1	T_0	Q_1^+	Q_0^+
0	0	0	1	0	1
0	1	1	1	1	0
1	0	1	0	0	0

Hence, the counter counts the sequence 00, 01, 10.

30. (d)

The output signal can be plotted as below:



$$V_{avg} = \frac{1}{(T/2)}\int_{\tau}^{T/2} 1\cdot dt = \frac{2}{T}\left[\frac{T}{2}-\tau\right] = 1-\frac{2\tau}{T}$$

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