S.No.: 01DKSK_EC+EE_I_260526

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DIGITAL CIRCUITS

EC-EE

Date of Test : 26/05/2026

ANSWER KEY ➤

1.	(a)	7.	(c)	13.	(c)	19.	(c)	25.	(c)
2.	(d)	8.	(c)	14.	(b)	20.	(b)	26.	(b)
3.	(a)	9.	(c)	15.	(c)	21.	(c)	27.	(a)
4.	(a)	10.	(c)	16.	(d)	22.	(b)	28.	(a)
5.	(c)	11.	(c)	17.	(a)	23.	(b)	29.	(c)
6.	(a)	12.	(c)	18.	(a)	24.	(c)	30.	(c)

DETAILED EXPLANATIONS

1. (a)

$$\text{output, } f = I_0\bar{S}_1\bar{S}_0 + I_1\bar{S}_1S_0 + I_2S_1\bar{S}_0 + I_3S_1S_0$$

where, $S_0 = A;\ S_1 = B$

$$I_0 = C;\ I_1 = \overline{C+D};\ I_2 = CD;\ I_3 = 1$$

$\therefore$ $f = C\bar{B}\bar{A} + (\overline{C+D})(\bar{B}A) + CDB\bar{A} + AB$

$= C\bar{B}\bar{A} + (\bar{C}\bar{D})(\bar{B}A) + CDB\bar{A} + AB$

$= \bar{A}\bar{B}C + A\bar{B}\bar{C}\bar{D} + \bar{A}BCD + AB$

$f = A\bar{B}\bar{C}\bar{D} + \bar{A}C\bar{B} + \bar{A}CD + AB$ $\quad [\because \bar{B} + BD = \bar{B} + D]$

$= A[B + \bar{C}\bar{D}] + \bar{A}C\bar{B} + \bar{A}CD$

$f = AB + A\bar{C}\bar{D} + \bar{A}C\bar{B} + \bar{A}CD$

2. (d)

$$Q = AB + \left[\overline{(B+C)(BC)}\right]$$

$= AB + \left[\overline{BC + BC}\right]$

$= AB + \overline{BC}$

$= AB + \bar{B} + \bar{C}$

$Q = A + \bar{B} + \bar{C}$

3. (a)

We have, $S = AB$

$\therefore$ output of 2 × 1 MUX is,

$$f = \bar{S}I_0 + SI_1 = \overline{AB}(A \oplus B) + AB(A \oplus B)$$

$= (A \oplus B)\left[\overline{AB} + AB\right] = (A \oplus B)[1]$

$f = A \oplus B$

4. (a)

Given, $(5456)_8$

5	4	5	6
↓	↓	↓	↓
101	100	101	110

$(101100101110)_2$

For Hexadecimal number, grouping 4 binary bits

1011	0010	1110
↓	↓	↓
B	2	E

$\therefore$ $(5456)_8 \longrightarrow (B2E)_{16}$

5. **(c)**

Number of quantization levels for 12-bit DAC

$$= 2^{12} = 4096$$

$$\text{Resolution} = \frac{1}{2^{12}-1} = 0.244\times10^{-3}$$

The smallest reading possible which corresponds to 1 LSB is $0.244 \times 10^{-3} \times 10$

$$= 2.44 \text{ mV}$$

6. **(a)**

A	B	C	
0	0	0	(Q_1: OFF, Q_2: OFF, Q_3:ON)
0	1	1	(Q_1: OFF, Q_2: ON, Q_3:OFF)
1	0	1	(Q_1: ON, Q_2: OFF, Q_3:OFF)
1	1	1	(Q_1: ON, Q_2: ON, Q_3:OFF)

7. **(c)**

$$(0\ 0\ 1\ 1\ 0\ 0\ 1\ 0) = (50)_{10}$$

$$1 \text{ V} = K \times 50 \Rightarrow K = 20 \text{ mV}$$

The largest output will occur for an input of $(1\ 1\ 1\ 1\ 1\ 1\ 1\ 1)_2 = (255)_{10}$

$$V_{\text{out(max)}} = 20 \text{ mV} \times (255)_{10}$$

$$= 5.10 \text{ V}$$

8. **(c)**

The given circuit is a Binary Ripple Up Counter. The output is cleared when Q_BQ_C =11 corresponding to the state

$$\begin{array}{ccc} Q_C & Q_B & Q_A \\ 1 & 1 & 0 \end{array} \longrightarrow \text{Mod 6 ripple counter}$$

9. **(c)**

When, $P = 0$,

$$Q_1 \rightarrow \text{ON},\ Q_2 \rightarrow \text{OFF} \Rightarrow Y = Q$$

When, $P = 1$,

$$Q_1 \rightarrow \text{OFF},\ Q_2 \rightarrow \text{ON} \Rightarrow Y = \bar{Q}$$

$$\text{Output} = \bar{P}Q + P\bar{Q}$$

$$Y = \bar{P}Q + P\bar{Q}$$

$$Y = P \oplus Q$$

$$Y = P \odot \bar{Q}$$

10. **(c)**

$$f = \bar{x}\,\bar{y} + \bar{x}y + x\bar{y}$$

$$= \bar{x}(\bar{y} + y) + x\bar{y}$$

$$= \bar{x} + x\bar{y}$$

$$= (\bar{x} + x)\cdot(\bar{x} + \bar{y}) = \bar{x} + \bar{y} = \overline{x \cdot y}$$

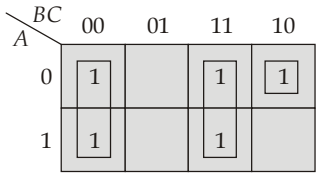
Thus it works as NAND gate.

11. **(c)**

Given output of 4 × 1 MUX,

$$f = \Sigma m(0, 2, 3, 4, 7)$$

By using K-map,



$$\therefore \quad f = \bar{B}\bar{C} + BC + \bar{A}B\bar{C}$$

The output function of 4 × 1 MUX can be written as,

$$f = I_0\bar{B}\bar{C} + I_1\bar{B}C + I_2B\bar{C} + I_3BC$$

On comparing,

$I_0 = 1$

$I_1 = 0$

$I_2 = \bar{A}$

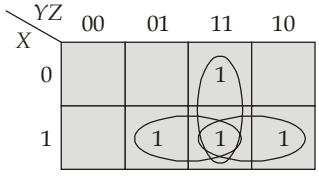
$I_3 = 1$

12. **(c)**

The truth table is,

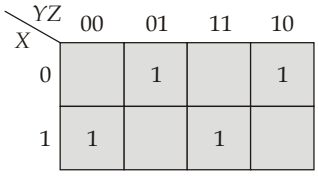
X	Y	Z	A	B	C
0	0	0	0	0	1
0	0	1	0	1	0
0	1	0	0	1	1
0	1	1	1	0	0
1	0	0	0	1	1
1	0	1	1	0	0
1	1	0	1	0	1
1	1	1	1	1	0

For A:



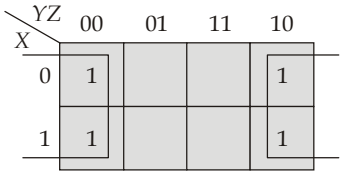
$$A = YZ + XY + XZ$$

For B:



$$B = \Sigma m(1, 2, 4, 7) = X \oplus Y \oplus Z$$

For C:



$C = \overline{Z}$

13. (c)

$(10)_{10} = (1010)_2$ [Switches D_3 and D_1 are closed]

The current flowing in 12.5 kΩ branch,

$$I_3 = \frac{5\text{ V}}{12.5\text{ k}\Omega} = 0.4\text{ mA}$$

The current flowing in 50 kΩ branch,

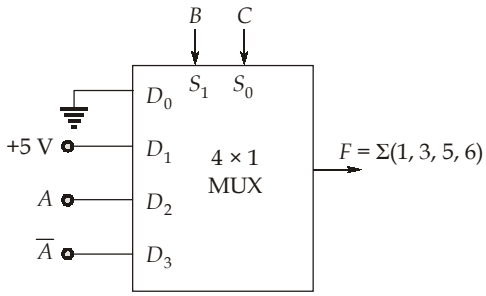
$$I_1 = \frac{5V}{50\text{ k}\Omega} = 0.1\text{ mA}$$

$$V_{out} = -[(0.4)\text{mA} + 0.1\text{ mA}] \times 20\ (\text{k}\Omega)$$
$$= -10\text{ V}$$

14. (b)

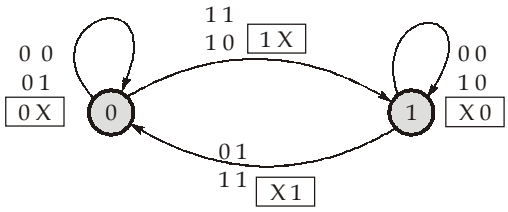
$F(A, B, C) = \Sigma(1, 3, 5, 6)$

	D_0	D_1	D_2	D_3
$\overline{A}$	0	①	2	③
A	4	⑤	⑥	7
	0	1	A	$\overline{A}$



15. (c)

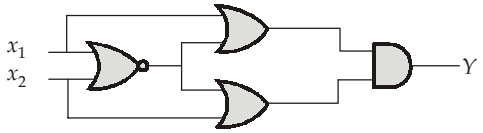
Present State	Inputs		Next State
Q_n	J	K	Q_{n+1}
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	0



16. (d)

OR-AND logic is equivalent to NOR-NOR logic, hence we get

$$Y = (X_1 + \overline{X_1 + X_2}) \cdot (X_2 + \overline{X_1 + X_2})$$



$$Y = (X_1 + \overline{X_1} \cdot \overline{X_2}) \cdot (X_2 + \overline{X_1} \cdot \overline{X_2})$$

$$Y = (X_1 + \overline{X_2})(X_1 + \overline{X_1})(X_2 + \overline{X_1})(X_2 + \overline{X_2})$$

$$Y = (X_1 + \overline{X_2})(X_2 + \overline{X_1})$$

$$Y = X_1X_2 + \overline{X_1} \cdot \overline{X_2} = X_1 \odot X_2 = \overline{X_1 \oplus X_2}$$

17. (a)

$$\% \text{ resolution} = \frac{1}{2^n - 1} \times 100$$

$$0.4 = \frac{1}{2^n - 1} \times 100$$

$$2^n - 1 = \frac{100}{0.4} = 250$$

$$2^n = 251$$

$$\Rightarrow \quad n = \log_2 251 \approx 8$$

$$n = 8$$

18. (a)

The output B for the given full subtractor can be written in K-Map as,

B \ ca / b	00	01	11	10
0	0	1	1	1
1	0	0	1	0

Borrow, $B = ca + \overline{b}a + \overline{b}c$

19. (c)

$$Y = \left[(A \cdot B + C) \cdot \overline{D}\right] \cdot \left[AB\overline{C}\right]$$

$$= (AB\overline{D} + C\overline{D}) \cdot (AB\overline{C})$$

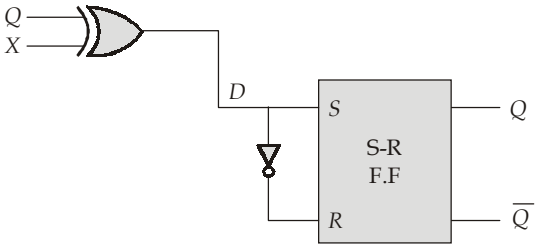
$$= AB\overline{C}\,\overline{D} + ABC \cdot \overline{C}\,\overline{D}$$

$$Y = AB\overline{C}\,\overline{D}$$

20. (b)

Option	Signed Magnitude	2's Complement
(a)	–0	–32
(b)	–16	–16
(c)	–24	–8
(d)	–31	–1

21. (c)

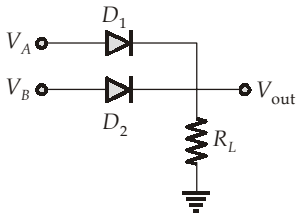


$$Q_{n+1} = D = Q \oplus X$$

For $X = 0$, $Q_{n+1} = Q_n$ and for $X = 1$, $Q_{n+1} = \overline{Q_n}$.

Therefore, the given circuit acts as T flip-flop for $T = X$.

22. (b)



If V_A = +3 V and V_B = 0, D_1 is ON and D_2 is OFF,

Thus, $V_{out} = V_A$ = +3 V

If uncertain we can assume both D_1 and D_2 are forward-biased immediately facing a conflict: D_1 enforces a voltage of + 3V at the output whereas D_2 shorts V_{out} to V_B = 0. This assumption is therefore incorrect.

The symmetry of the circuit with respect to V_A and V_B suggest that V_{out} = +3 V if V_A = 0 and V_B = +3 V. If $V_A = V_B$ = 0, both the diodes D_1 and D_2 are OFF, with V_{out} = 0 V. The circuit, thus operates as a logical OR - gate.

23. (b)

From the given digital circuit,

$$D_0 = \overline{Q_0 + Q_2}$$

Initially, $Q_0 = 0$; $Q_1 = 0$, $Q_2 = 0$

$\therefore$ $D_0 = 1$

Clk	Q_0	Q_1	Q_2
0	0	0	0
1	1	0	0
2	0	1	0
3	1	0	1
4	0	1	0
5	1	0	1
6	0	1	0

The given circuit is MOD-2 counter.

24. (c)

Given, input frequency, $f_i = 96$ kHz

After MOD-6 counter, $f' = \frac{f_i}{6} = \frac{96\text{ K}}{6} = 16\text{ kHz}$

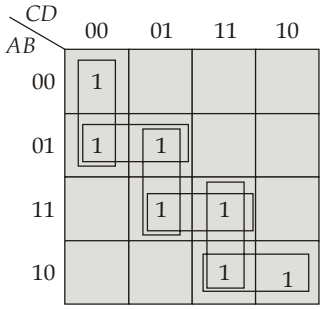
After Decade counter, $f_0 = \frac{f'}{10} = \frac{16\text{ kHz}}{10} = 1.6\text{ kHz}$

25. (c)

The given logic function can be written as,

$$f(A, B, C, D) = \Sigma m(0, 4, 5, 10, 11, 13, 15)$$

Using *K*-map:



Total prime implicants = 6 ($AC'D'$, $A'BC'$, $BC'D$, ABD, ACD and $AB'C$)

Number of essential prime implicants = 2 ($A'C'D'$ and $AB'C$)

26. (b)

Given, $f_1(A, B, C) = \Sigma m(2, 3, 4)$

$f_2(A, B, C) = \pi M(0, 1, 5, 6, 7) = \Sigma m(2, 3, 4)$

For f_{out} to be zero, the function f_3 should be equal to,

$$f_3(A, B, C) = \Sigma m(2, 3, 4)$$

$\therefore$ The maximum number of possible minterms = 3.

27. (a)

From the given number, the minimum value of 'x' can be written as, "12 + 1 = 13" ($\because$ $C = 12$)

Therefore, the least decimal equivalent

$$= 10 \times 13^2 + 11 \times 13^1 + 12 \times 13^0$$
$$= 1690 + 143 + 12 = (1845)_{10}$$

28. (a)

In a 4-bit ripple counter, four flip-flops (FF0 to FF3) are used. The input frequency of flip-flop FF0 is 'f' and its output waveform frequency is $f/2$ which is applied as input of FF1. Consequently, the output waveform frequency of FF1 is $f/4$ which is used as input of FF2.

Then output waveform frequency of FF2 is $f/8$ which is used as input of FF3. Therefore, the output waveform frequency of FF3 is f/16 and the time period is

$$T = \frac{1}{\text{Frequency}} = \frac{16}{f}$$

Since, time period of the last flip-flop (FF3) is 128 microseconds.

$$\therefore \quad T = \frac{16}{f} = 128 \times 10^{-6}$$

$$\therefore \quad f = \frac{16}{128 \times 10^{-6}} = 125\,\text{kHz}$$

$\therefore$ The clock frequency of a 4-bit ripple counter is,

$$f = 125 \text{ kHz}$$

29. (c)

15's complement is equivalent to

$$\begin{array}{r} \text{F F F} \\ -\,\underline{\text{B B D}} \\ (4\,4\,2)_{16} \end{array}$$

30. (c)

Since, given that, V_{out} = 0.2 V for 00001

$\therefore$ the weight of LSB is 0.2 V.

The the weight of other bits in weighted D/A converter can be obtained as 0.4 V, 0.8 V, 1.6 V and 3.2 V respectively.

For a digital input of 11111, the value of output, V_{out} = 3.2 + 1.6 + 0.8 + 0.4 + 0.2 = 6.2 V.

■■■■