CLASS TEST

S.No.: 01DLSK_ABCDEFG_290426

MADE EASY
Leading Institute for IES, GATE & PSUs
Delhi | Bhopal | Hyderabad | Jaipur | Pune
Web: www.madeeasy.in | **E-mail:** info@madeeasy.in | **Ph:** 011-45124612

COMPUTER ORGANISATION

ELECTRONICS ENGINEERING

Date of Test : 29/04/2026

ANSWER KEY

1.	(d)	7.	(b)	13.	(d)	19.	(a)	25.	(d)
2.	(b)	8.	(a)	14.	(b)	20.	(b)	26.	(b)
3.	(d)	9.	(d)	15.	(d)	21.	(b)	27.	(b)
4.	(b)	10.	(a)	16.	(d)	22.	(b)	28.	(d)
5.	(d)	11.	(b)	17.	(a)	23.	(b)	29.	(c)
6.	(d)	12.	(a)	18.	(b)	24.	(b)	30.	(a)

Detailed Explanations

1. (d)

Arithmetic operations and logical operations are performed by ALU. The function of CU in a CPU is to generate control signals based on decoded program instructions.

2. (b)

Vertical microprogrammed control unit is highly encoded scheme and supports shorter control word.

3. (d)

Hierarchical access memory organisation or cache memory access organisation is an example of locality of reference.

4. (b)

Swap space is an area on disk that temporarily holds a process memory image. When physical memory demand is sufficiently low, process memory images are brought back into physical memory from the swap area. Having sufficient swap space enables the system to keep some physical memory free at all times.

5. (d)

6. (d)

$$\text{No. of chips required} = \frac{1\text{ KB}}{256 \times 1\text{ bits}} = \frac{2^{10} \times 8}{2^8 \times 1} = 32$$

7. (b)

8. (a)

Little endian is used when lower addresses are used to contain lower byte whereas in the Big-endian, lower addresses are used to contain higher byte. Be default, little endian technique is used.

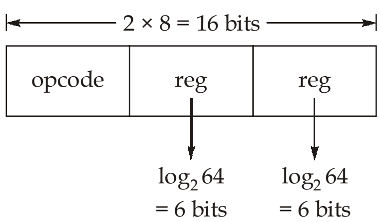
9. (d)

Cache memory, also called as CPU memory, is high speed RAM that a computer microprocessor can access more quickly than it can access regular RAM.

10. (a)

The control data register holds the present microinstruction while next address is computed and read from memory. The data register is sometimes called a pipeline register. Microinstructions are stored in control memory in groups, with each group specifying a routine, where each routine specifies how to carry out an instruction.

11. (b)



$\therefore$ Bit assigned to opcode = 16 – 6 – 6 = 4 bits

$\therefore$ No. of instructions in CPU = 2^4

= 16 instructions

12. (a)

Time taken by five stage pipeline processor for executing single instruction,

$$T = \text{Max}(150, 120, 150, 160, 140)$$
$$T = 160 \text{ nsec}$$

Time required to execute 100 independent instructions

$$= [5 + (100 - 1)]160$$
$$= (5 + 99) \times 160 = 16640 \text{ nsec} = 16.64\ \mu\text{sec}$$

13. (d)

$$\text{EMAT} = H_1T_1 + (1 - H_1)\, T_2$$
$$= 0.8 \times 50 + (1 - 0.8) \times 750 = 40 + 0.2 \times 750 = 40 + 150$$
$$\text{EMAT} = 190 \text{ nsec}$$

14. (b)

Sequential program = 2.5%

Let time taken to execute whole program without pipeline = 100 sec

Parallel program = 97.5%

But it is having infinite number of processors.

$\therefore$ Ideally time taken to execute 97.5% part of program is zero.

$$\therefore \quad \text{Speedup} = \frac{\text{time without pipeline}}{\text{Time with pipeline}} = \frac{100}{0+2.5}$$

$$\text{Speedup} = 40$$

15. (d)

$$\text{Avg } CPI = \Sigma(IC_i \times CPI_i), \text{ where IC is instruction count}$$
$$= 0.6 \times 1 + 0.18 \times 2 + 0.12 \times 4 + 0.1 \times 8$$
$$= 2.24$$

$$\therefore \quad \text{Avg. CPU time} = (\text{Avg. CPI}) \times \text{Cycle time}$$

$$= 2.24 \times \frac{1}{400 \times 10^6}$$

$$\text{Avg. CPU time} = 5.6 \text{ nsec}$$

16. (d)

PC holds the value of next instruction to be executed. We store the value of PC to MBR and then to memory. We are saving the value of PC in memory and new address value is loaded into PC. This can be done only in interrupt service.

17. (a)

The control data register holds the present microinstruction while next address is computed and read from memory. The data register is sometimes called a pipeline register. Microinstructions are stored in control memory in groups, with each group specifying a routine, where each routine specifies how to carry out an instruction.

18. (b)

$$T_c = 50 \text{ nsec}$$
$$T_m = 1000 \text{ nsec}$$
$$T_e = T_c + \frac{T_c \times 20}{100}$$
$$T_e = 1.2\ T_c$$
$$T_e = 1.2T_c = HT_c + (1 - H)(T_c + T_m)$$
$$1.2 \times 50 = H \times 50 + (1 - H)(1050)$$
$$60 = 50\text{H} + 1050 - 1050\text{H}$$
$$1000H = 1050 - 60$$
$$H = 0.99$$

19. (a)

Cache memory stores commonly used data, which is copied from main memory, temporarily.

20. (b)

$$\text{speedup} = \frac{\text{Original time taken}}{\text{New time taken}}$$

Let x be time for a fixed point operation.

$\therefore$ Original average time taken for an operation $= \dfrac{3x + 2 \times 2x}{5} = \dfrac{7x}{5}$

New average time taken for an operation $= \dfrac{\dfrac{3x}{1.1} + \dfrac{4x}{1.2}}{5} = \dfrac{8x}{1.32 \times 5}$

Hence, $\quad \text{speedup} = \dfrac{7x/5}{8x/1.32 \times 5} = \dfrac{7 \times 1.32}{8} = 1.155$

21. (b)

The cache is a smaller, faster memory which copies the data from frequently used main memory location.

Interleaved memory is designed to compensate for the relatively slow speed of dynamic random access memory (DRAM) or core memory by spreading memory addresses evenly across memory banks which can be accessed individually without any dependency on the other.

22. (b)

$$\begin{aligned} T_{avg} &= h_1 t_1 + (1 - h_1)h_2 (t_2 + t_1) + (1 - h_1)(1 - h_2)(t_3 + t_2 + t_1) \\ &= 0.65 \times 0.02 + 0.35 \times 0.45 \times 0.22 + 0.35 \times 0.55 \times 2.22 \\ &= 0.013 + 0.03465 + 0.42735 \\ &= 0.475 = 475\ \mu\text{sec} \end{aligned}$$

23. (b)

Instruction received by the CPU is decoded by control unit not by arithmetic unit.

24. (b)

Architecture = 32 bit, mean 1 word = 32 bits

Number of distinct instructions supported = 25

$\Rightarrow$ $$\text{Opcode} = \lceil \log_2(25) \rceil = 5 \text{ bits}$$

Number of addressing modes = 32 $\Rightarrow$ Mode field = $\log_2 32$ = 5 bits

Memory size = 1 MB $\Rightarrow$ Memory address = 20 bits (2^{20} = 1 MB)

Instruction format:

32

opcode	Addressing Mode	Register reference	Memory address
5	5		20

Register reference = 32 – (20 + 5 + 5)

= 2 bits

Maximum number of registers possible = 2^2 = 4

25. (d)

Hardwired control unit uses fixed logic to interrupt instruction and generate appropriate control signal. Micro-programmed control unit is flexible in nature as a code is used to generate the control signals.

Since, the control signals in horizontal microprogram control unit are not encoded, 1 bit is required per control signal. Hence, no signal decoder is needed.

26. (b)

$A \leftarrow 73$ H

$CY \leftarrow 1$

SBI 56 H

$\Downarrow$

$A \leftarrow A$ – [56 H] – [CY]

$A \leftarrow$ 73H – 56H – 01H

A $\Rightarrow$ 1C H

$$\begin{array}{r} 0111\ 0011 \\ -\,0101\ 0110 \\ \hline 0001\ 1101 \\ -1 \\ \hline 0001\ 1100 \\ \hline (1\ \text{C})\text{H} \end{array}$$

27. (b)

$$(55)_{10} = (37)_H$$

ACI instruction adds the data with the accumulator content with carry.

i.e.,
$$\begin{array}{r} 37\ \text{H} \\ 56\ \text{H} \\ +\ \ 1\ \ \ \ \\ \hline 8\text{E H} \end{array}$$

28. (d)

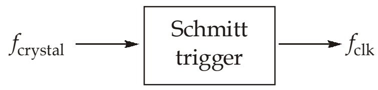
- Instruction cycle $\rightarrow$ to fetch and execute a given instruction.
- Machine cycle $\rightarrow$ to perform an operation eg. memory or I/O access. 1 machine cycle is equivalent to 1 memory cycle and consists of 3 to 6 clock cycles.
- Clock cycle $\rightarrow$ 1 clock period or 1 T-state.

29. (c)

- Maskable interrupts are those which can be disabled or ignored by the microprocessor. Maskable interrupts are INTR, RST 7.5, RST 6.5 and RST 5.5.
- TRAP is a non-maskable interrupt.

30. (a)

8085 microprocessor uses a divide-by-two circuit to generate its internal clock. Hence, the frequency of the crystal/driving network connected between pin 1 and pin 2 must be twice the desired clock frequency.



■■■■