CLASS TEST

S.No. : 01JP_CS_COA_08092025

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COMPUTER SCIENCE & IT

Computer Organization

Duration : 1:00 hr. **Maximum Marks : 50**

Read the following instructions carefully

1. This question paper contains **30** objective questions. **Q.1-10** carry one mark each and **Q.11-30** carry two marks each.
2. Answer all the questions.
3. Questions must be answered on Objective Response Sheet (**ORS**) by darkening the appropriate bubble (marked **A**, **B**, **C**, **D**) using HB pencil against the question number. Each question has only one correct answer. In case you wish to change an answer, erase the old answer completely using a good soft eraser.
4. There will be **NEGATIVE** marking. For each wrong answer **1/3rd** of the full marks of the question will be deducted. More than one answer marked against a question will be deemed as an incorrect response and will be negatively marked.
5. Write your name & Roll No. at the specified locations on the right half of the **ORS**.
6. No charts or tables will be provided in the examination hall.
7. Choose the **Closest** numerical answer among the choices given.
8. If a candidate gives more than one answer, it will be treated as a **wrong answer** even if one of the given answers happens to be correct and there will be same penalty as above to that questions.
9. If a question is left blank, i.e., no answer is given by the candidate, there will be **no penalty** for that question.

DO NOT OPEN THIS TEST BOOKLET UNTIL YOU ARE ASKED TO DO SO

Q. No. 1 to Q. No. 10 carry 1 mark each

Q.1 Consider a CPU, where all the instructions require 6 clock cycles to complete their execution. Under the instruction set there are 215 instructions and a total of 125 control signals are needed to be generated by the control unit. While designing the horizontal micro-programmed control unit, single address field format is used for branch control logic.

What is the minimum size of control word and control address register.

(a) 136, 11 (b) 7, 12
(c) 7, 11 (d) 125, 11

Q.2 Consider a scenario where instruction operation codes are represented in 8 bits, memory addresses are 64 bits and register addresses are 6 bits and data values are 32 bit integers.

Consider the code sequence for "C = A + B" is as follows:

Stack	Accumulator	Register (Register-Memory)	Register (Load-store)
Push A Push B Add Pop C	Load A Add B Store C	Load R_1, A Add R_3, R_1, B Store R_3, C	Load R_1, A Load R_2, B Add R_3, R_1, R_2 Store R_3, C

Note that the add instruction has implicit operands for stack and accumulator architectures explict operands for register architectures. It is assumed that A, B and C all being in memory and that the values of A and B can not be destroyed. The total code size is _____ (in bits).

(a) 880 (b) 1040
(c) 940 (d) 1080

Q.3 Consider the following statements:

S_1: Comparing the time T_1 taken for a single instruction on a pipelined CPU with time T_2 taken on a non-pipelined but identical CPU we can say that $T_1 \le T_2$.

S_2: The performance of pipelined processor suffers if the pipeline stages have different delays.

Which of the following option is correct?

(a) Both S_1 and S_2 are correct
(b) only S_1 is correct
(c) Only S_2 is correct
(d) None of S_1 or S_2 is correct

Q.4 A computer system that uses memory mapped I/O configuration, has a 32 bit address space. Address with 1's in 4 MSB refers to devices. What is the maximum amount of memory and port addresses that can be referenced in such system respectively?

(a) 15×2^{25} and 1×2^{28}
(b) 15×2^{32} and 1×2^{32}
(c) 15×2^{28} and 1×2^{30}
(d) 12×2^{28} and 1×2^{28}

Q.5 In a vectored interrupt:

(a) the interrupting device supplies the branch information to the processor through an interrupt vector.
(b) the CPU does not know, which device cause the interrupt without polling each I/O interface.
(c) the branch address is always assigned to a fixed location in memory.
(d) None of the above.

Q.6 The average seek time and rotational delay in a disk system are 6 ms and 3 ms, respectively. The rate of data transfer to or from the disk is 30 MBps and all disk accesses are of 8 KB of data. Disk DMA controller, the processor, and the main memory are all attached to a single bus. The data bus width is 32 bits, and a bus transfer to or from the main memory takes 10 nanoseconds. How many disk units are there that can be simultaneously transferring data to or from the main memory?

(a) 11 (b) 12
(c) 13 (d) 14

Q.7 A DMA module is transferring characters to memory using cycle stealing mode, from a device which is transmitting at a rate of 19200 bps. The rate at which processor is fetching the instruction is 2 million instructions per second (2 MIPS). Due to DMA, CPU slowed down by _____ (in %)

(a) 1% (b) 0.11%
(c) 0.22% (d) 2%

Q.8 Consider a CPU that executes at a clock rate of 200 MHz (5 ns per cycle) with a single level of cache. $CPI_{execution}$ i.e. CPI with ideal memory is 1.1. Instruction mix are 50% arithmetic / logical, 30% load / store, 20% control instruction. Assume the cache miss rate is 15% and a miss penalty of 5 cycles. The number of times cpu with ideal memory is faster when no miss-occurs _____.

(a) 1.58 (b) 2
(c) 1.88 (d) 3.48

Q.9 Consider the following statement. Out of the statements choose the one which best characterize computers that use memory mapped I/O.

(a) the computer provides special instruction for manipulating I/O port.
(b) I/O ports are placed at address on bus and as accessed just like other memory location.
(c) to perform an I/O operation, it is sufficient to place the data in an address and call the channel to perform the operation.
(d) ports are referenced only by memory mapped instruction of the computer and are located at hardwired memory location.

Q.10 Match **List-I** with **List-II** and select the correct option accordingly.

List-I	List-II
A. Thrashing	1. Direct Cache
B. Expand-OPcode technique	2. Inclusion
C. Write Back Protocol	3. Coherence
D. Write through Protocol	4. Fixed Length Instruction

Codes:

	A	B	C	D
(a)	2	4	3	1
(b)	1	4	3	2
(c)	3	1	2	4
(d)	4	2	3	1

Q. No. 11 to Q. No. 30 carry 2 marks each

Q.11 Consider two cache organizations. The first one is 64 kB, 4-way associative with 64 byte block size. The second one is of the 64 kB direct mapped cache. The size of an address is 32 bits in both organization. A 4 to 1 multiplexer has latency of 0.8 ns which k bit comparator has latency of k/5 nsec. The difference between the hit latencies of both cache organization (i.e. associative hit latency – direct mapped hit latency) (in nsec) is _____.

(a) 2.2 (b) 1.2
(c) 3.2 (d) 4.4

Q.12 Suppose that in 500 memory references there are 100 misses in first level and 50 miss in second level cache. Assume that miss penalty from L_2 cache to memory is 100 cycles. The hit time of L_2 cache is 20 cycles. If there are 2 memory references per instruction, the average stall per instruction is _____.

(a) 30 (b) 20
(c) 32 (d) 28

Q.13 Consider 4-way set associative cache of a 64 KB organized into a 32 bytes blocks. Main memory size is 4 GB. In the cache controller, each line in the set contain 1 valid, 1 modified and 2 replacement bits along with a tag. How much space is required in the cache controller to store the tag information (Meta data) (in Kb)?

(a) 44 (b) 22
(c) 32 (d) 18

Q.14 A hypothetical CPU supports 400 instructions. Each instruction takes 4 cycles to accomplish the execution. The control unit is designed using vertical programming which has 150 control signals, 45 flags and 20 branch conditions. The number of bits required for Control Address Register (CAR) and Control Data Register (CDR) is

(a) 16 bit and 11 bit respectively
(b) 10 bit and 28 bit respectively
(c) 11 bit and 30 bit respectively
(d) 15 bit and 25 bit respectively

Q.15 Consider a modified 8-bit floating point representation in which 1-bit for sign, 3-bit for exponent and 4-bit for significant. What will be representation for decimal value –12?

(a) 11111000 (b) 11101000
(c) 11110000 (d) 11111100

Q.16 Consider 4 stage instruction pipeline executed on a system:

	S_1	S_2	S_3	S_4
I_1	1	3	1	1
I_2	2	1	2	1
I_3	1	2	1	2
I_4	2	1	2	1

If all instructions are executed only once, what is the throughput of system?

(a) $\frac{4}{9}$ cycles (b) $\frac{4}{10}$ cycles

(c) $\frac{4}{12}$ cycles (d) $\frac{4}{11}$ cycles

Q.17 A processor supports 256 kW of memory and uses memory mapped I/O for I/O Port. Address to the I/O Port is assigned when 3 MSB bits of address is high. The number of memory address available for I/O port is _____.

(a) 34768 (b) 32768

(c) 30748 (d) 38648

Q.18 Consider the following set of instructions executed for a program to be accomplish.

Instruction	Meaning
I_1 : STORE M[100], R_1	$M[100] \leftarrow R_1$
I_2 : MOV R_2,M[700]	$R_2 \leftarrow M[700]$
I_3 : DIV R_1,R_2,R_1	$R_1 \leftarrow R_2 / R_1$
I_4 : ADD R_2,R_1,R_2	$R_2 \leftarrow R_1 + R_2$
I_5 : STORE M[500],R_2	$M[500] \leftarrow R_2$
I_6 : STORE M[200],R_1	$M[200] \leftarrow R_1$

How many number of anti data dependency and true data dependency in the above instructions?

(a) 2 and 3 (b) 2 and 2

(c) 2 and 1 (d) 1 and 3

Q.19 Consider the following instruction sequence with there meaning given below:

Instruction	Meaning of Instruction
I_0 : MUL R_2, R_5, R_1	$R_2 \leftarrow R_5 \times R_1$
I_1 : DIV R_5, R_3, R_4	$R_5 \leftarrow R_3/R_4$
I_2 : ADD R_2, R_5, R_2	$R_2 \leftarrow R_5 + R_2$
I_3 : SUB R_5, R_2, R_6	$R_5 \leftarrow R_2 - R_6$

What is the number of Write After Read (WAR) and Write After Write (WAW) hazards for the above instruction sequence?

(a) 3, 2 (b) 2, 1

(c) 3, 1 (d) 1, 2

Q.20 Consider the following program codes:

I_1 : Load R_1, (R_2)
I_2 : MUL R_1, R_3
I_3 : SUB R_3, R_0
I_4 : Load (R_0), R_3
I_5 : DIV R_5, R_6
I_6 : SUB R_2, R_5
I_7 : HALT
I_8 : ADD R_2, R_4
I_9 : LOAD (R_3), R_0

Assume the data transfer instruction size is 48 bit, ALU operation instruction size 40 bit and branch instruction size is 24 bit. The program starts from the location 5000 decimal onwards. Assume if the interrupt occurs during the execution of I_7, the return address pushed onto the stack is _____.

(a) 5032 (b) 5027

(c) 5048 (d) 5045

Q.21 A device with data transfer rate 40 KB/sec is connected to a CPU, where data transfer time between interfaces to memory or CPU is neglected. If the interrupt overhead is 2 μsec, then minimum performance gain of operating the device under interrupt mode over operating it under program controlled mode _____. (Assume data transferred Byte wise)

(a) 13.5 (b) 12.5

(c) 14.5 (d) 11.5

Q.22 The access time of cache memory is 45 nsec and that of main memory is 750 nsec. It is found that 75% of memory requests are for read and remaining for write. If the hit access for read and write is 0.9 and 1 respectively and write through protocol is used, then the average memory access time is _____. (in nsec)

(a) 271.125 (b) 274.125

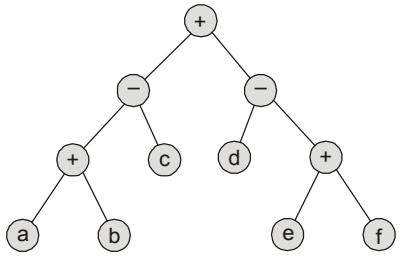
(c) 273.625 (d) 278.625

Q.23 Consider a CPU where all the instruction require 10 clock cycles to complete execution. There are 258 instructions in instruction set. It is found that 129 control signals are needed to be generated by control unit. While designing the vertical μ-programmed control unit, single address field format is used for branch control logic. The size of control memory in byte is ___.

(a) 6250 (b) 6650

(c) 6450 (d) 6850

Q.24 Consider the evaluation of the following expression tree on a machine in which memory can be accessed only through load and store instructions. The variables *a*, *b*, *c*, *d*, *e*, and *f* are initially stored in memory. The binary operators used in this tree can be evaluated by the machine only when the operands are in registers. The instructions produce result only in a register.



If no intermediate results can be stored in memory, what is the minimum number of registers needed to evaluate this expression?

(a) 2 (b) 3
(c) 4 (d) 5

Q.25 Consider a 2-way set associative cache with 8 cache blocks. If the memory block requests are accessed 2 time in the following order 0, 4, 8, 4, 0, 4, 8, 4, 3, 15, 19, 15, 3, 15, 19, 15. If LRU replacement policy is used, then the total number of misses are _____.

(a) 15 (b) 16
(c) 14 (d) 18

Q.26 Consider a pipeline processor with 5 stages, Instruction Fetch (IF). Instruction Decode and Operand Fetch (ID), Operation performed (OP). Data memory access (MA) and Write back (WB). The IF, ID, MA and WB stages takes 1 clock cycle each for any instruction. The OP stage takes 1 clock cycle for ADD and SUB instructions and takes 3 clock cycles for MUL instruction. The minimum number of clock cycles are needed to complete following sequence of instruction if operand forwarding is used _____.

Instruction	Meaning of Instruction
I_0 : ADD R_2, R_0, R_1	$R_2 \leftarrow R_0 + R_1$
I_1 : SUB R_1, R_2, R_1	$R_1 \leftarrow R_2 + R_1$
I_2 : MUL R_2, R_1, R_0	$R_2 \leftarrow R_1 + R_0$
I_3 : SUB R_0, R_2, R_0	$R_0 \leftarrow R_2 + R_0$
I_4 : ADD R_3, R_1, R_0	$R_3 \leftarrow R_1 + R_0$

(a) 10 (b) 11
(c) 12 (d) 13

Q.27 Consider the floating point Arithmetic for single precision, match the following pairs if E′ = Biased exponent and M = Mantissa:

List-1	List-2
P. E′ = 0, M = 0	(i) $\pm\infty$
Q. E′ = 0, M ≠ 0	(ii) ± 0
R. E′ = 255, M = 0	(iii) Denormal numbers
S. E′ = 255, M ≠ 0	(iv) Not a number (NaN)

Which of the following is the correct match between the **List-1** and **List-2**?

	P	Q	R	S
(a)	(ii)	(iii)	(iv)	(i)
(b)	(ii)	(iv)	(i)	(iii)
(c)	(ii)	(iii)	(i)	(iv)
(d)	(ii)	(iv)	(iii)	(i)

Q.28 The main difference between a CISC and RISC processor are that RISC processor has:

S_1 : Hardwired Control Unit

S_2 : No memory unit so uses a separate hardware

S_3 : Require external memory for calculation

S_4 : Implements pipelining

(a) S_1, S_2 and S_4 (b) S_2, S_3 and S_4

(c) S_1 and S_4 (d) All the statements

Q.29 Consider a machine with a byte addressable main memory of 256 MB, block size of 128 bytes and 8-way set associative cache of size 64 kB. If the address of one of the memory location AB01C23H accessed by the CPU. What are the tag field of the corresponding cache line is

(a) 101010110000000

(b) 101110100000

(c) 101010110000

(d) 101101010100000

Q.30 A CPU has 24 bit instructions and we have to calculate the sum of n number by using below code:

	MOV N, R_1
	Clear R_0, R_2
Loop:	$R_0 \leftarrow [R_0] + R_2[PC]$
	Dec R_1
	$R_2 = [R_2] + 1$;
	Branch > 0, X [PC]
	MOV R_0, SUM

The value of X, if target address of branch is loop, when instruction is uses PC relative addressing mode is _____. (Assume memory is byte addressable)

(a) –10 (b) +12

(c) +10 (d) (–12)

■■■■

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Date of Test : 08/09/2025

ANSWER KEY ➤

1.	(d)	7.	(b)	13.	(a)	19.	(a)	25.	(d)
2.	(c)	8.	(c)	14.	(c)	20.	(a)	26.	(b)
3.	(c)	9.	(b)	15.	(b)	21.	(b)	27.	(c)
4.	(a)	10.	(b)	16.	(d)	22.	(b)	28.	(c)
5.	(a)	11.	(b)	17.	(b)	23.	(c)	29.	(a)
6.	(c)	12.	(d)	18.	(a)	24.	(b)	30.	(d)

DETAILED EXPLANATIONS

1. (d)

Since, it uses horizontal micro-programmed that requires 1 bit control / signal.
For 125 control signal, we need 125 bits.
Total number of micro-operation instruction = 215 × 6 = 1290
It requires 11 bit.

2. (c)

Stack	
Push (A)	8 + 64
Push (B)	8 + 64
Add	8
Pop (C)	8 + 64
= 224 bits	

Accumulator	
Load A	8 + 64
Add B	8 + 64
Store C	8 + 64
= 216 bits	

Register-Memory	
Load R_1, A	8 + 6 + 64
Add R_3, R_1, B	8 + 6 + 6 + 64
Store R_3, C	8 + 6 + 64
= 240 bits	

Load-store	
Load R_1, A	8 + 6 + 64
Load R_2, B	8 + 6 + 64
Add R_3, R_1, R_2	8 + 6 + 6 + 6
Store R_3, C	8 + 6 + 64
= 260 bits	

Total size = 224 + 216 + 240 + 260 = 940 bits

3. (c)

- In pipelined CPU, there will be buffer delays. So, for single instruction non-pipelined CPU takes less time compared to pipelined CPU.
- Structural dependencies cause hazards during pipelining.

4. (a)

	A_{31}	A_{30}	A_{29}	A_{28}	$A_3 A_2 A_1 A_0$
Memory	0	0	0	0	
	0	0	0	1	
	0	0	1	0	
	0	0	1	1	
	0	1	0	0	
	M	M	M	M	
	1	1	0	1	
	1	1	1	0	
I/O →	1	1	1	1	

∴ Memory address space: 15×2^{28}
I/O address space = 1×2^{28}

5. (a)

A vectored interrupt is the one, where CPU actually knows the address of the ISR in advance, with the help of an interrupt vector, the interrupting device supplies the branch information to the processor.

6. (c)

Rate of transfer to or from any one disk = 30 MBps.

$$\text{Maximum memory transfer rate} = \frac{4\,B}{10 \times 10^{-9}} = 400 \times 10^6 \text{Bps} = 400 \text{ MBps}$$

Since rate of data transfer = 30 MBps

$$\text{Here number of disk transfer} = \left\lceil \frac{400}{30} \right\rceil = 13$$

Therefore, 13 disks can simultaneously transfer data to or from the main memory.

7. (b)

DMA transfer character at rate of 19200 bpsec

$$8 \text{ bit} = 1 \text{ character}$$

So, $192000 \text{ b} = 2400 \text{ character}$

So, $1 \text{ sec} = 2400 \text{ character}$

$$1 \text{ character} = \frac{1}{2400} = 416.7 \times 10^{-6} \text{ sec}$$

Processor fetch rate is 2 MIPS

$$1 \text{ MIPS} = 1 \text{ sec}$$

$$1 \text{ Instruction} = \frac{1}{2 \times 10^6} = 0.5 \text{ micro-sec}$$

$$\% \text{ slow down using DMA} = \frac{0.5 \times 10^{-6}}{416.7 \times 10^{-6}} \times 100$$

$$= \frac{0.5}{416.7} = 0.11\%$$

8. (c)

$$\text{CPI} = \text{CPI}_{\text{execution}} + \text{Memory stall per instruction} \quad ...(1)$$

$$\text{Memory stall per instruction} = \text{Memory access / Instruction} * \text{Miss rate} * \text{Miss penalty} \quad ...(2)$$

$$\text{Memory access / Instruction} = \text{Instruction fetch + Load / store} = 1 + 0.3 = 1.3 \quad ...(3)$$

from (2) and (3)

$$\text{Memory stall / Instruction} = 1.3 \times 0.15 \times 5 = 0.975$$

...(4)

from (1) and (4)

$$\text{CPI} = 1.1 + 0.975 = 2.075$$

The ideal memory CPU with no misses $= \frac{2.075}{1.1} = 1.88$ time faster

9. (b)

Memory mapped I/O uses the same address bus to address both memory and I/O devices the memory and registers of the I/O devices are mapped to address values.

So, when an address is accessed by the CPU, it may refer to a portion of physical RAM, but it can also refer to memory of I/O device.

10. (b)

11. (b)

$$\text{Number of cache lines} = \frac{64\,kB}{64\,B} = 1 \text{ k} = 2^{10}$$

$$\text{Number of sets} = \frac{2^{10}}{2^2} = 2^8$$

Tag	Set	Block
18	8	6

$$H_1 = 18/5 + 0.8 \text{ ns}$$

$$= 3.6 + 0.8 \text{ ns} = 4.4 \text{ ns}$$

Direct mapped cache:

Tag	Set	Block
16	10	6

This is no need of multiplexer in direct mapped cache.

So $H_2 = 16 / 5$ nsec
$= 3.2$ nsec
Difference $= H_1 - H_2$
$= 4.4 - 3.2 = 1.2$ nsec

12. (d)

2 memory references $\rightarrow$ 1 Instruction
500 memory references $\rightarrow$? instructions.

$$\text{Number of instructions} = \frac{500}{2} = 250$$

$$\left[\frac{\#\text{ memory stalls}}{\#\text{ Instructions}}\right] = \left[\frac{\#\text{ misses } L_1}{\#\text{ Instructions}} \times \text{hit } L_2\right] + \left[\frac{\#\text{ misses } L_2}{\#\text{ Instructions}} \times \text{miss panality } L_2\right]$$

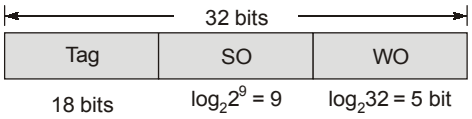
$$= \left[\frac{100}{250} \times 20\right] + \left[\frac{50}{250} \times 100\right]$$

$$= [20 + 8] = 28 \text{ cycles}$$

13. (a)

$$\text{Number of lines} = \frac{64K}{32} = 2^{11}$$

$$\text{Number of sets} = \frac{2^{11}}{4} = \frac{2^{11}}{2^2} = 2^9$$



Tag memory size $= S \times P \times \#$ tag bits
$= 2^9 \times 4 \times (18 + 1 + 1 + 2)$
$= 2^9 \times 2^2 \times 22$ bits
$= 2^{10} \times 2 \times 22$ bits
$= 44$ K bits

14. (c)

f cycles/instruction = 4
Total # *f* μ-instruction = $400 \times 4 = 1600$
f bit for CAR = $[\log_2(1600)] = 11$ bit

Branch Conditions	Flag	Control Signal	CM Address
5-bit	6-bit	8-bit	11-bit

f bit for CDR = $5 + 6 + 8 + 11 = 30$ bit

15. (b)

Given, Decimal = –12

Number is negative, so

Sign bit = 1

Sign	Exponent	Significant
1-bit	3-bit	4-bit

- Now express 12 in binary form : 1100
  Normalized form = 1.100×2^3
- For 3-bit exponent field, a bias of $(2^{3-1} - 1 = 3)$ is used.
- Add the bias to the exponent = 3 + 3 = 6 = $(110)_2$.

Hence result will be

1	110	1000
Sign	Exponent	Significant

Hence, option (b) is correct.

16. (d)

	c_1	c_2	c_3	c_4	c_5	c_6	c_7	c_8	c_9	c_{10}	c_{11}
S_4						I_1		I_2	I_3	I_3	I_4
S_3					I_1	I_2	I_2	I_3	I_4	I_4	
S_2		I_1	I_1	I_1	I_2	I_3	I_3	I_4			
S_1	I_1	I_2	I_2		I_3	I_4	I_4				

$$\text{Throughput} = \frac{\text{Number of task completed}}{\text{Total time taken to process the tasks}}$$

$$= \frac{4}{11} \text{ cycles}$$

17. (b)

Given that 256 kW of memory used.

$$256 \text{ kW} = 2^8 \times 2^{10} \text{ W}$$
$$= 2^{18} \text{ W}$$

Whenever 3 MSB bit is high, that is used for I/O port.

$$\underbrace{A_{17}A_{16}A_{15}}_{\text{3 MSB bit}} \quad \underbrace{A_{14}.....A_3A_2A_1A_0}_{\text{15 LSB bit}}$$
$$\underbrace{1\ 1\ 1}$$
$$\downarrow$$
$$2^{15}$$

When $A_{17}A_{16}A_{15}$ is high then remaining 2^{15} combinations of memory reserved for I/O Port.

So, $2^{15} = 32768$

18. (a)

Anti data dependency → Write After Read Hazard (WAR)

True data dependency → Read After Write Hazard (RAW)

	WAR hazards		RAW hazards (Adjacent)
1.	$I_3 - I_1(R_1)$	1.	$I_3 - I_2(R_2)$
2.	$I_4 - I_3(R_2)$	2.	$I_4 - I_3(R_1)$
		3.	$I_5 - I_4(R_2)$

19. (a)

$$\text{WAW} = I_0(R_2) \rightarrow I_2(R_2),\ I_1(R_5) \rightarrow I_3(R_5)$$
$$\text{WAR} = I_0(R_5) \rightarrow I_1(R_5),\ I_0(R_5) \rightarrow I_3(R_5),\ I_2(R_5) \rightarrow I_3(R_5)$$

20. (a)

I_1 : 5000 – 5005
I_2 : 5006 – 5010
I_3 : 5011 – 5015
I_4 : 5016 – 5021
I_5 : 5022 – 5026
I_6 : 5027 – 5031
I_7 : 5032 – 5034
I_8 : 5035 – 5039
I_9 : 5040 – 5045

Return address (5032) is pushed onto the stack.

21. (b)

Execution time of programmed IO mode :

$$1 \text{ sec} \rightarrow 40 \text{ KB}$$
$$1\text{B} \rightarrow \frac{1}{40\text{K}} = 25\ \mu \text{ sec}$$
$$\Rightarrow \quad S = \frac{25}{2} = 12.5$$

22. (b)

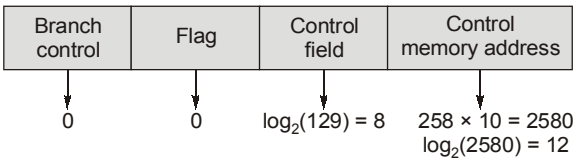
$$T_{\text{average read}} = 0.90 \times 45 + 0.10 \times 750$$
$$= 40.5 + 75 = 115.5 \text{ nsec}$$

In write-through technique, CPU performs simultaneous WRITE operation in both cache memory and main memory. So,

$$T_{\text{average write}} = \text{Max}[T_{\text{updation}}(\text{cache}), T_{\text{updation}}(\text{main memory})]$$
$$= \text{Max}[45, 750]$$
$$= 750 \text{ nsec}$$

So
$$T_{\text{average}} = 0.75\,(115.5) + 0.25\,(750)$$
$$= 86.625 + 187.5$$
$$= 274.125 \text{ nsec}$$

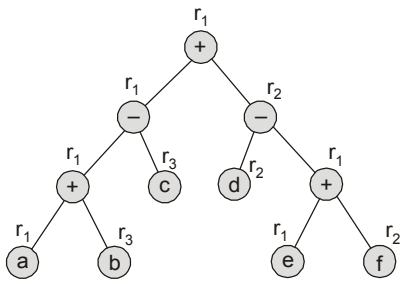
23. (c)



$$\text{So, control memory size} = 2580 \text{ Control words}$$
$$= 2580 = 20 \text{ bits}$$
$$\text{Size in bytes} = \frac{2580 \times 20 \text{ bits}}{8} = 6450$$

24. (b)

Load	r_1, e
Load	r_2, f
Add	r_1, r_2
Load	r_2, d
Sub	r_2, r_1
Load	r_1, a
Load	r_3, b
Add	r_1, r_3
Load	r_3, c
Sub	r_1, r_3
Add	r_1, r_2



25. (d)

$$\text{Number of sets} = \frac{\text{Number of blocks}}{2}$$

$$= \frac{8}{2} = 4$$

0	~~0~~ ~~8~~ ~~0~~ 8	4
1		
2		
3	~~3~~ ~~19~~ ~~3~~ 19	15

1st access
[Initially all sets are empty]
Number of miss = 10

0	~~8~~ ~~0~~ ~~8~~ ~~0~~ 8	4
1		
2		
3	~~19~~ ~~3~~ ~~19~~ ~~3~~ 19	15

2nd access
[Initially set 1 contains 8, 4 and set 3 contains 19, 15]
Number of miss = 8

So, total number of misses are = 10 + 8 = 18

26. (b)

Clock cycles	Instruction (operation)
1	SUB
1	ADD
3	MUL

	c_1	c_2	c_3	c_4	c_5	c_6	c_7	c_8	c_9	c_{10}	c_{11}
I_0	IF	ID	OP	MA	WB						
I_1		IF	ID	OP	MA	WB					
I_2			IF	ID	OP	OP	OP	MA	WB		
I_3				IF	ID			OP	MA	WB	
I_4					IF			ID	OP	MA	WB

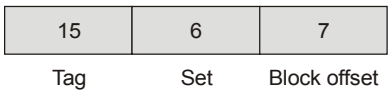
Total number of clock cycles needed for given program is 11.

27. (c)

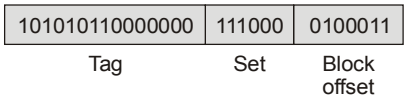
28. (c)

29. (a)

$$\text{Cache size} = 64\text{ kB} = 2^{16}$$
$$\text{Block size} = \text{Cache line size} = 128\text{ bytes} = 2^7$$
$$\text{Number of cache lines} = \frac{2^{16}}{2^7} = 2^9$$
$$\text{Number of sets} = \frac{2^9}{2^3} = 2^6 = 64$$



Memory location : A B 0 1 C 2 3



30. (d)

$$\text{Each instruction of 24 bits} = \frac{24}{8} = 3\text{ B}$$

So, loop: $\leftarrow [R_0] + R_2\,[\text{PC}]\ i$
Dec R_1 $i + 3\text{B}$
$R_2 \leftarrow [R_2] + 1$ $i + 6\text{B}$
Branch > 0, offset $i + 9\text{B}$

$$\text{PC} = [i + 12\text{B}]$$
$$\text{So value of } X = [i + 12] - 12 = i$$
$$\text{So value of } X = [-12]$$

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