Sl. : 01SKEC_ABCDEFG_220425

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COMPUTER ORGANISATION

ELECTRONICS ENGINEERING

Date of Test : 22/04/2025

ANSWER KEY ➤

1.	(d)	7.	(c)	13.	(b)	19.	(a)	25.	(b)
2.	(b)	8.	(c)	14.	(b)	20.	(d)	26.	(d)
3.	(a)	9.	(d)	15.	(c)	21.	(a)	27.	(a)
4.	(b)	10.	(a)	16.	(d)	22.	(d)	28.	(d)
5.	(b)	11.	(b)	17.	(d)	23.	(d)	29.	(a)
6.	(a)	12.	(c)	18.	(c)	24.	(c)	30.	(b)

Detailed Explanations

1. (d)
Cache memory (SRAM) access time is less compared to main memory (DRAM). Further, Register is the part of CPU and more closer than Cache so it is much faster to access from register.

2. (b)
The word length of processor is defined as the width of a CPU register, which determines the maximum size of data that can be processed by the CPU in one clock cycle.

3. (a)
Control unit is a component of a computer's central processing unit that directs the operations of the processor. Control unit accesses program instruction, decodes them, and coordinates the flow of data in and out of the ALU, the registers, the primary storage and various output devices.

4. (b)
Instruction prefetch i.e. fetching instructions before they need to be executed is often combined with pipelining in an attempt to keep the pipeline busy.

5. (b)
Instruction received by the CPU is decoded by control unit, not by arithmetic unit.

6. (a)
PC holds the address of next instruction.
Size of instruction is 24 bits i.e., 3 bytes.
Starting address of the program is 300. So, the address is always the multiple of 3 bytes i.e., 24 bits. Hence, the valid counter value will be the one which is the multiple of 3 i.e. 315.

7. (c)
Pipelining allows for efficient utilization of computational resources. The processor remains busy most of the time as idle stages are filled with new instructions, maximizing the utilization of hardware resources.

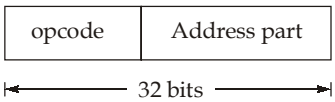
8. (c)
Von Neumann computers belong to single instruction stream and single data stream.

9. (d)
If X is the value contained in instruction,
(i) In Absolute Addressing Mode, effective address of the operand, $EA = X$.
(ii) In Indirect addressing mode, $EA = [X]$ i.e. the address of the operand is stored at memory location X.
(iii) Immediate addressing mode, the value of the operand is specified in the instruction itself.
(iv) In index addressing mode, $EA = X + [R_i]$ i.e. the effective address of the operand is generated by adding an index value to the contents of a register.

10. (a)
The control data register holds the present microinstruction while next address is computed and read from memory. The data register is sometimes called a pipeline register. It allows the execution of the microoperations specified by the control word simultaneously with the generation of the next microinstruction.

11. (b)

The instruction format of the given computer:



Each memory word has 32 bits and each instruction is stored in one memory word.

$\therefore$ The number of bits needed to represent opcode = $\lceil \log_2(260) \rceil$

$= \lceil 8.022 \rceil$

$= 9$ bits

The number of bits needed for address part = 32 – 9

$= 23$ bits

$\Rightarrow$ The maximum allowable size of the memory = 2^{23} words

1 word = 32 bits

$\therefore$ Maximum size of the memory = $2^{23} \times 32$

$= 256 \times 2^{20}$ bits

= 32 MB (Mega Bytes)

12. (c)

K stage pipeline can process n tasks in T time given by

$$T = [K + (n - 1)]T_{clk}$$

T_{clk} = maximum stage delay + Register delay

= Max(25, 45, 65, 35) + 1

= 65 + 1

T_{clk} = 66 nsec

$\therefore$ T = (4 + 100 – 1) 66 nsec

T = 6.798 μsec

13. (b)

$$\text{speedup} = \frac{\text{Original time taken}}{\text{New time taken}}$$

Let x be time for a fixed point operation.

$\therefore$ Original time taken = $\dfrac{3x + 2 \times 2x}{5} = \dfrac{7x}{5}$

$\because$ $\text{speed} \propto \dfrac{1}{\text{time}}$

$\therefore$ Time taken by the enhanced CPU design = $\dfrac{\frac{3x}{1.1} + \frac{4x}{1.2}}{5} = \dfrac{8x}{1.32 \times 5}$

Hence, $\text{speedup} = \dfrac{7x/5}{8x/1.32 \times 5} = \dfrac{7 \times 1.32}{8} = 1.155$

14. (b)

- Memory Data Register (MDR) contains data to be written into or read out from the addressed location.
- Memory Address Register (MAR) holds the address of the location to be addressed from memory.

- Program Counter holds the memory address of the next instruction that would be executed.
- Index register is used for pointing to operand addresses during the run of a program.

15. (c)

RISC processor has CPI = 1.

The RISC processors are used in real time applications.

RISC systems commonly uses Expanding opcode technique to have fixed size instructions. RISC processor uses hardwired control unit while the CISC processors use microprogrammed control unit.

16. (d)

$$\text{RAM chip capacity} = 512 \times 128$$
$$= 2^9 \times 2^6$$
$$= 2^{12} \times 8$$
$$= 2^2 \times 2^{10} \times 8$$
$$= 4 \text{ kB}$$

$\therefore$ Address lines = 12 i.e. $A_0 - A_{11}$

$A_{15}A_{14}A_{13}A_{12}$ is selected such that $\overline{CS} = 0$ i.e. $A_{15}A_{14}A_{13}A_{12} = 1100$

	A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0
Starting	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Ending	1	1	0	0	1	1	1	1	1	1	1	1	1	1	1	1

Starting address = C000 H

Ending address = CFFF H

$\therefore$ Memory address range $\Rightarrow$ C000 H – CFFF H

17. (d)

Time taken by nonpipelined processor,

$$T_{WP} = nKT_{clk}$$

Here, $K = 45$

$\therefore$ $T_{WP} = 45\ n\ T_{CLK}$

Time taken by pipelined processor $T_P = (n + K - 1)T_{CLK}$

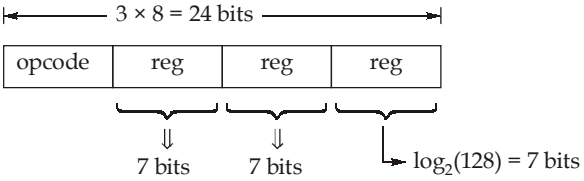
$$T_P = (n + 44)T_{CLK}$$

$$\text{Speedup} = 9 = \frac{T_{WP}}{T_P}$$

$$9 = \frac{45\,nT_{clk}}{(n+44)T_{clk}}$$

$$n + 44 = 5n$$
$$4n = 44$$
$$n = 11$$

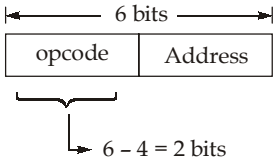
18. (c)



Bits assigned to opcode = 24 – 7 – 7 – 7 = 3 bits

∴ Number of instructions in CPU = 2^3 = 8 instructions

19. (a)



Number of bits required for opcode = 6 – 4 = 2 bits

Total number of possible operations = 2^2 = 4

Number of free opcodes = 4 – 2 (as '2' are 1-address instructions)

Number of free opcodes = 2

∴ Number of possible zero address instructions

= Number of free opcode $*$ $2^{\text{address size}}$

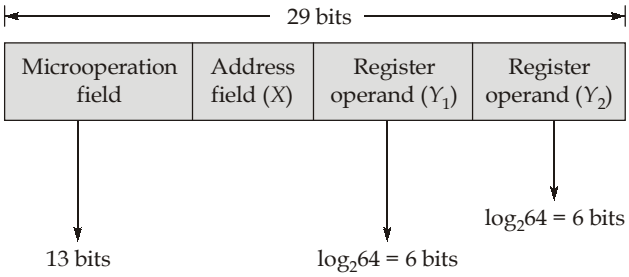
= 2×2^4

= 32

20. (d)

$$\text{No. of chips needed} = \frac{2048 \times 8}{128 \times 8} = 16$$

21. (a)



Address field (X) = 29 – 13 – 6 – 6

= 4 bits

Register operand $Y_1 = Y_2$ = 6 bits

No. of possible microinstructions = 2^{13} = 8192 microinstructions.

22. (d)

Overlapped register window is a characteristic of RISC processor used to speed up procedure call and return. Each procedure call results in the allocation of a new window consisting of a set of registers from the register file for use by the new procedure. Each procedure call activates a new register window by incrementing a pointer, while the return statement decrements the pointer and causes the activation of the previous window. Windows for adjacent procedures have overlapping registers that are shared to provide the passing of parameters and results.

23. (d)

Time taken by six stage pipeline processor for single instruction

$$T = \text{Max}[152, 121, 111, 169, 147, 132]$$
$$T = 169 \text{ nsec}$$

Time required to execute 150 independent instructions

$$= [6 + (150 - 1)] \times 169 \text{ nsec}$$
$$= 26.195 \ \mu\text{sec}$$

24. (c)

Time taken by five stage pipeline processor for single instruction,

$$T = \text{Max (3 nsec, 2 nsec, 5 nsec, 4 nsec, 6 nsec)}$$
$$T = 6 \text{ nsec}$$

$\therefore$ Time required to execute 96 instructions on this processor

$$= (n + K - 1)[T + T_l]$$

where $T_l \rightarrow$ Latch delay

$$= (5 + 96 - 1)[6 + 0.2] \text{ nsec}$$
$$= 620 \text{ nsec}$$
$$= 0.62 \ \mu\text{sec}$$

25. (b)

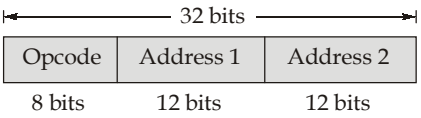
When addressing mode is index with R_1 as the index register.

$$\text{effective address} = \text{Address field value} + \text{index register value}$$
$$= 400 + 200$$
$$= 600$$

26. (d)

$$\text{Instruction size} = 32 \text{ bits}$$

Two address instruction format:



No. of possible instructions opcode = $2^8 = 256$

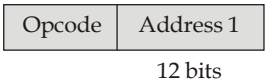
Given: Two address instructions opcode = 250

$\therefore$ Remaining instruction opcode = 256 – 250

$$= 6$$

These 6 opcode combinations can be used for one address instructions.

One address instruction format:



$\therefore$ Maximum number of one address instructions

$$= 6 \times 2^{12}$$
$$= 24576$$

27. **(a)**

MIPS rating of a processor is dependent on the program being executed.

i.e., MIPS rating of the same processor would vary depending on which program is selected for running on the computer to determine the MIPS rating.

28. **(d)**

Enhanced portion/fraction is 75% i.e., 0.75 performance enhanced/speedup obtained due to enhancement is '5'.

Amdahl's law states that, "The performance improvement to be gained by using a faster mode of execution is limited by the fraction of time the faster mode can be used.

By this, speedup overall is,

$$S_{\text{overall}} = \left[(1-F)+\frac{F}{S}\right]^{-1}$$

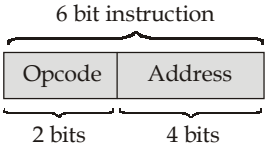
$$= \left[(1-0.75)+\frac{0.75}{5}\right]^{-1}$$

$$= [0.25 + 0.15]^{-1}$$

$$= (0.4)^{-1}$$

$$S_{\text{overall}} = 2.5$$

29. **(a)**



$\therefore$ No. of possible single address instruction (operation)

$$= 2^{\text{opcode}} = 2^2$$

$$= 4$$

30. **(b)**

$$\text{No. of lines in CM } (N) = \frac{16B}{2B} = 8$$

$$\text{No. of sets } [S] = \frac{\text{No. of lines in CM } [N]}{\text{P-way set}}$$

$$= \frac{8}{2} = 4$$

$$S = 4$$

■■■■