CLASS TEST

S.No. : 01SK_CS_BCDF_310325

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Date of Test : 31/03/2025

ANSWER KEY ➤

1.	(d)	7.	(b)	13.	(a)	19.	(a)	25.	(d)
2.	(c)	8.	(c)	14.	(c)	20.	(a)	26.	(b)
3.	(c)	9.	(b)	15.	(b)	21.	(b)	27.	(c)
4.	(a)	10.	(b)	16.	(d)	22.	(b)	28.	(c)
5.	(a)	11.	(b)	17.	(b)	23.	(c)	29.	(a)
6.	(c)	12.	(d)	18.	(a)	24.	(b)	30.	(d)

DETAILED EXPLANATIONS

1. (d)

Since, it uses horizontal micro-programmed that requires 1 bit control / signal.
For 125 control signal, we need 125 bits.
Total number of micro-operation instruction = 215 × 6 = 1290
It requires 11 bit.

2. (c)

Stack	
Push (A)	8 + 64
Push (B)	8 + 64
Add	8
Pop (C)	8 + 64
= 224 bits	

Accumulator	
Load A	8 + 64
Add B	8 + 64
Store C	8 + 64
= 216 bits	

Register-Memory	
Load R_1, A	8 + 6 + 64
Add R_3, R_1, B	8 + 6 + 6 + 64
Store R_3, C	8 + 6 + 64
= 240 bits	

Load-store	
Load R_1, A	8 + 6 + 64
Load R_2, B	8 + 6 + 64
Add R_3, R_1, R_2	8 + 6 + 6 + 6
Store R_3, C	8 + 6 + 64
= 260 bits	

Total size = 224 + 216 + 240 + 260 = 940 bits

3. (c)

- In pipelined CPU, there will be buffer delays. So, for single instruction non-pipelined CPU takes less time compared to pipelined CPU.
- Structural dependencies cause hazards during pipelining.

4. (a)

	A_{31}	A_{30}	A_{29}	A_{28}	$A_3 A_2 A_1 A_0$
Memory	0	0	0	0	
	0	0	0	1	
	0	0	1	0	
	0	0	1	1	
	0	1	0	0	
	M	M	M	M	
	1	1	0	1	
	1	1	1	0	
I/O →	1	1	1	1	

∴ Memory address space: 15×2^{28}
I/O address space = 1×2^{28}

5. (a)

A vectored interrupt is the one, where CPU actually knows the address of the ISR in advance, with the help of an interrupt vector, the interrupting device supplies the branch information to the processor.

6. (c)

Rate of transfer to or from any one disk = 30 MBps.

$$\text{Maximum memory transfer rate} = \frac{4\,B}{10 \times 10^{-9}} = 400 \times 10^6 \text{Bps} = 400 \text{ MBps}$$

Since rate of data transfer = 30 MBps

$$\text{Here number of disk transfer} = \left\lceil \frac{400}{30} \right\rceil = 13$$

Therefore, 13 disks can simultaneously transfer data to or from the main memory.

7. (b)

DMA transfer character at rate of 19200 bpsec

$$8 \text{ bit} = 1 \text{ character}$$

So, $192000 \text{ b} = 2400 \text{ character}$

So, $1 \text{ sec} = 2400 \text{ character}$

$$1 \text{ character} = \frac{1}{2400} = 416.7 \times 10^{-6} \text{ sec}$$

Processor fetch rate is 2 MIPS

$$1 \text{ MIPS} = 1 \text{ sec}$$

$$1 \text{ Instruction} = \frac{1}{2 \times 10^6} = 0.5 \text{ micro-sec}$$

$$\% \text{ slow down using DMA} = \frac{0.5 \times 10^{-6}}{416.7 \times 10^{-6}} \times 100$$

$$= \frac{0.5}{416.7} = 0.11\%$$

8. (c)

$$\text{CPI} = \text{CPI}_{\text{execution}} + \text{Memory stall per instruction} \quad ...(1)$$

$$\text{Memory stall per instruction} = \text{Memory access / Instruction} * \text{Miss rate} * \text{Miss penalty} \quad ...(2)$$

$$\text{Memory access / Instruction} = \text{Instruction fetch + Load / store} = 1 + 0.3 = 1.3 \quad ...(3)$$

from (2) and (3)

$$\text{Memory stall / Instruction} = 1.3 \times 0.15 \times 5 = 0.975$$

...(4)

from (1) and (4)

$$\text{CPI} = 1.1 + 0.975 = 2.075$$

The ideal memory CPU with no misses $= \frac{2.075}{1.1} = 1.88$ time faster

9. (b)

Memory mapped I/O uses the same address bus to address both memory and I/O devices the memory and registers of the I/O devices are mapped to address values.

So, when an address is accessed by the CPU, it may refer to a portion of physical RAM, but it can also refer to memory of I/O device.

10. (b)

11. (b)

$$\text{Number of cache lines} = \frac{64\,kB}{64\,B} = 1 \text{ k} = 2^{10}$$

$$\text{Number of sets} = \frac{2^{10}}{2^2} = 2^8$$

Tag	Set	Block
18	8	6

$$H_1 = 18/5 + 0.8 \text{ ns}$$

$$= 3.6 + 0.8 \text{ ns} = 4.4 \text{ ns}$$

Direct mapped cache:

Tag	Set	Block
16	10	6

This is no need of multiplexer in direct mapped cache.

So $H_2 = 16 / 5$ nsec
$= 3.2$ nsec
Difference $= H_1 - H_2$
$= 4.4 - 3.2 = 1.2$ nsec

12. (d)

2 memory references $\rightarrow$ 1 Instruction
500 memory references $\rightarrow$? instructions.

$$\text{Number of instructions} = \frac{500}{2} = 250$$

$$\left[\frac{\#\text{ memory stalls}}{\#\text{ Instructions}}\right] = \left[\frac{\#\text{ misses } L_1}{\#\text{ Instructions}} \times \text{hit } L_2\right] + \left[\frac{\#\text{ misses } L_2}{\#\text{ Instructions}} \times \text{miss panality } L_2\right]$$

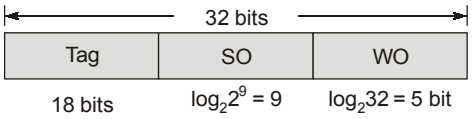
$$= \left[\frac{100}{250} \times 20\right] + \left[\frac{50}{250} \times 100\right]$$

$$= [20 + 8] = 28 \text{ cycles}$$

13. (a)

$$\text{Number of lines} = \frac{64K}{32} = 2^{11}$$

$$\text{Number of sets} = \frac{2^{11}}{4} = \frac{2^{11}}{2^2} = 2^9$$



Tag memory size $= S \times P \times \#$ tag bits
$= 2^9 \times 4 \times (18 + 1 + 1 + 2)$
$= 2^9 \times 2^2 \times 22$ bits
$= 2^{10} \times 2 \times 22$ bits
$= 44$ K bits

14. (c)

f cycles/instruction = 4
Total # *f* μ-instruction = $400 \times 4 = 1600$
f bit for CAR = $[\log_2(1600)] = 11$ bit

Branch Conditions	Flag	Control Signal	CM Address
5-bit	6-bit	8-bit	11-bit

f bit for CDR = $5 + 6 + 8 + 11 = 30$ bit

15. (b)

Given, Decimal = –12

Number is negative, so

Sign bit = 1

Sign	Exponent	Significant
1-bit	3-bit	4-bit

- Now express 12 in binary form : 1100
  Normalized form = 1.100×2^3
- For 3-bit exponent field, a bias of $(2^{3-1} - 1 = 3)$ is used.
- Add the bias to the exponent = 3 + 3 = 6 = $(110)_2$.

Hence result will be

1	110	1000
Sign	Exponent	Significant

Hence, option (b) is correct.

16. (d)

	c_1	c_2	c_3	c_4	c_5	c_6	c_7	c_8	c_9	c_{10}	c_{11}
S_4						I_1		I_2	I_3	I_3	I_4
S_3					I_1	I_2	I_2	I_3	I_4	I_4	
S_2		I_1	I_1	I_1	I_2	I_3	I_3	I_4			
S_1	I_1	I_2	I_2		I_3	I_4	I_4				

$$\text{Throughput} = \frac{\text{Number of task completed}}{\text{Total time taken to process the tasks}}$$

$$= \frac{4}{11} \text{ cycles}$$

17. (b)

Given that 256 kW of memory used.

$$256 \text{ kW} = 2^8 \times 2^{10} \text{ W}$$
$$= 2^{18} \text{ W}$$

Whenever 3 MSB bit is high, that is used for I/O port.

$$\underbrace{A_{17}A_{16}A_{15}}_{\text{3 MSB bit}} \quad \underbrace{A_{14}.....A_3A_2A_1A_0}_{\text{15 LSB bit}}$$
$$\underbrace{1\ 1\ 1}$$
$$\downarrow$$
$$2^{15}$$

When $A_{17}A_{16}A_{15}$ is high then remaining 2^{15} combinations of memory reserved for I/O Port.

So, $2^{15} = 32768$

18. (a)

Anti data dependency → Write After Read Hazard (WAR)

True data dependency → Read After Write Hazard (RAW)

	WAR hazards		RAW hazards (Adjacent)
1.	$I_3 - I_1(R_1)$	1.	$I_3 - I_2(R_2)$
2.	$I_4 - I_3(R_2)$	2.	$I_4 - I_3(R_1)$
		3.	$I_5 - I_4(R_2)$

19. (a)

$$\text{WAW} = I_0(R_2) \rightarrow I_2(R_2),\ I_1(R_5) \rightarrow I_3(R_5)$$
$$\text{WAR} = I_0(R_5) \rightarrow I_1(R_5),\ I_0(R_5) \rightarrow I_3(R_5),\ I_2(R_5) \rightarrow I_3(R_5)$$

20. (a)

I_1 : 5000 – 5005
I_2 : 5006 – 5010
I_3 : 5011 – 5015
I_4 : 5016 – 5021
I_5 : 5022 – 5026
I_6 : 5027 – 5031
I_7 : 5032 – 5034
I_8 : 5035 – 5039
I_9 : 5040 – 5045

Return address (5032) is pushed onto the stack.

21. (b)

Execution time of programmed IO mode :

$$1 \text{ sec} \rightarrow 40 \text{ KB}$$
$$1\text{B} \rightarrow \frac{1}{40\text{K}} = 25\ \mu \text{ sec}$$
$$\Rightarrow \quad S = \frac{25}{2} = 12.5$$

22. (b)

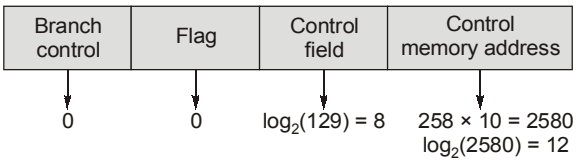
$$T_{\text{average read}} = 0.90 \times 45 + 0.10 \times 750$$
$$= 40.5 + 75 = 115.5 \text{ nsec}$$

In write-through technique, CPU performs simultaneous WRITE operation in both cache memory and main memory. So,

$$T_{\text{average write}} = \text{Max}[T_{\text{updation}}(\text{cache}), T_{\text{updation}}(\text{main memory})]$$
$$= \text{Max}[45, 750]$$
$$= 750 \text{ nsec}$$

So
$$T_{\text{average}} = 0.75\,(115.5) + 0.25\,(750)$$
$$= 86.625 + 187.5$$
$$= 274.125 \text{ nsec}$$

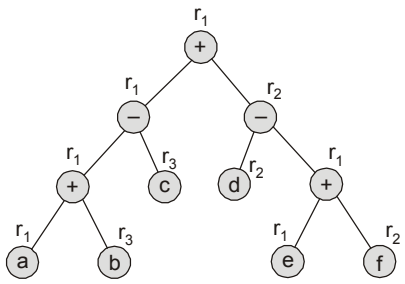
23. (c)



$$\text{So, control memory size} = 2580 \text{ Control words}$$
$$= 2580 = 20 \text{ bits}$$
$$\text{Size in bytes} = \frac{2580 \times 20 \text{ bits}}{8} = 6450$$

24. (b)

Load	r_1, e
Load	r_2, f
Add	r_1, r_2
Load	r_2, d
Sub	r_2, r_1
Load	r_1, a
Load	r_3, b
Add	r_1, r_3
Load	r_3, c
Sub	r_1, r_3
Add	r_1, r_2



25. (d)

$$\text{Number of sets} = \frac{\text{Number of blocks}}{2}$$

$$= \frac{8}{2} = 4$$

0	~~0~~ ~~8~~ ~~0~~ 8	4
1		
2		
3	~~3~~ ~~19~~ ~~3~~ 19	15

1st access
[Initially all sets are empty]
Number of miss = 10

0	~~8~~ ~~0~~ ~~8~~ ~~0~~ 8	4
1		
2		
3	~~19~~ ~~3~~ ~~19~~ ~~3~~ 19	15

2nd access
[Initially set 1 contains 8, 4 and set 3 contains 19, 15]
Number of miss = 8

So, total number of misses are = 10 + 8 = 18

26. (b)

Clock cycles	Instruction (operation)
1	SUB
1	ADD
3	MUL

	c_1	c_2	c_3	c_4	c_5	c_6	c_7	c_8	c_9	c_{10}	c_{11}
I_0	IF	ID	OP	MA	WB						
I_1		IF	ID	OP	MA	WB					
I_2			IF	ID	OP	OP	OP	MA	WB		
I_3				IF	ID			OP	MA	WB	
I_4					IF			ID	OP	MA	WB

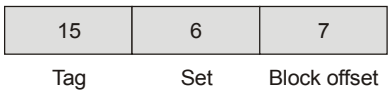
Total number of clock cycles needed for given program is 11.

27. (c)

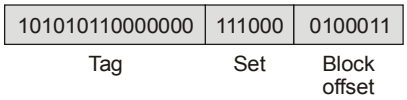
28. (c)

29. (a)

$$\text{Cache size} = 64\text{ kB} = 2^{16}$$
$$\text{Block size} = \text{Cache line size} = 128\text{ bytes} = 2^7$$
$$\text{Number of cache lines} = \frac{2^{16}}{2^7} = 2^9$$
$$\text{Number of sets} = \frac{2^9}{2^3} = 2^6 = 64$$



Memory location : A B 0 1 C 2 3



30. (d)

$$\text{Each instruction of 24 bits} = \frac{24}{8} = 3\text{ B}$$

So, loop: $\leftarrow [R_0] + R_2\,[\text{PC}]\ i$
Dec R_1 $i + 3\text{B}$
$R_2 \leftarrow [R_2] + 1$ $i + 6\text{B}$
Branch > 0, offset $i + 9\text{B}$

$$\text{PC} = [i + 12\text{B}]$$
$$\text{So value of } X = [i + 12] - 12 = i$$
$$\text{So value of } X = [-12]$$

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