Electronics Engineering

Advanced Electronics

Comprehensive Theory

with Solved Examples and Practice Questions

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CHAPTER 1

Introduction to VLSI Technology

1.1 Historical Perspective

In the beginning of the twenty-first century, we find ourselves surrounded by different machines and applications that are impossible to build without applying the principles of electronics onto them. Moreover, the communication boom that we see now would not have been possible without the advancement in the electronics industry and without using integrated circuits (ICs). Integrated circuits can simply be described as a large circuit manufactured on a very small semiconductor chip. Starting with a few transistors on a single chip in the early 1970's, it has increased to a billion transistors within a span of 40 years. The ever-increasing demand of humans has pushed the technology to integrate more and more components into a single chip. And it is expected that the trend will continue.

The journey started when the first transistor was invented in 1947 by Bardeen, Brattain and Schockley at the Bell Telephone Laboratory. It was followed by the introduction of the bipolar junction transistor (BJT) in 1949 by Schockley. Then it took seven years to build a digital logic gate. In 1958, Jack Kilby at Texas Instruments first made the monolithic integrated circuit. This was a significant breakthrough in the semiconductor technology by Kilby, for which he was awarded Noble Prize in 2000. the first commercial IC was introduced by Fairchild Corporation in 1960 followed by TTL IC in 1962. The ECL logic family has come up in 1974. Another breakthrough in the IC technology is the introduction of the first microprocessor 4004 by Intel in 1972. Since then, there has been a steady progress in the IC industry resulting in high density chips such as Pentium processors.

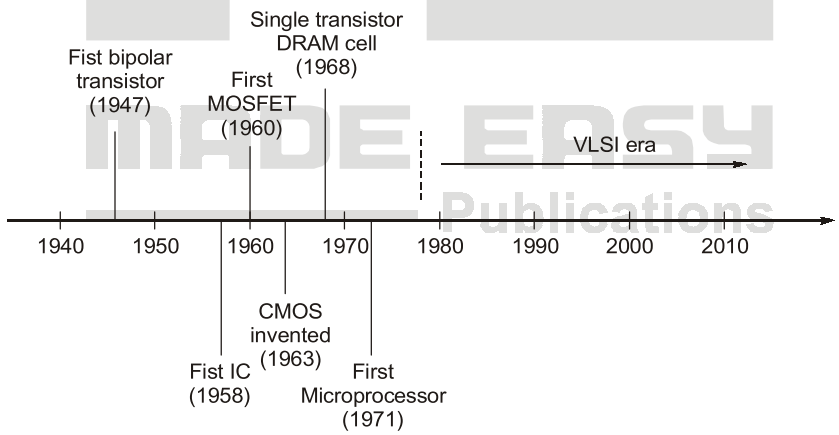


Figure-1.1 *Evolution of VLSI (major milestones)*

The evolution of very large scale integration (VLSI) in the last half century is illustrated in Figure (1.1), indicating major milestones.

Depending on the level of integration of components into a single chip, the IC technology is classified into several categories, among which VLSI is an advanced integration level. The acronym VLSI is used in the context of integrated circuit (IC) design and manufacturing. Table 1.1 lists the difference IC technologies that have evolved over the last 50 years.

Year	Era	Level of integration
1958	Single transistor	–
1960	Monolithic IC	1
1962	Multi-function	2-4
1964	Complex function	5-20
1967	Medium scale integration (MSI)	20-200
1972	Large scale integration (LSI)	200-2000
1978	Very large scale integration (VLSI)	2000-20,000
1989	Ultra large scale integration (ULSI)	Above 20,000

Table-1.1 *Evolution of integration level in integrated circuits*

1.2 Introduction to IC Technology

VLSI technology has been the enabler for advancement of the present electronics and communication age. Silicon has been a natural choice of material for IC manufacturing because of its abundance in nature, and more importantly its native oxide which is most suitable for IC fabrication. Almost 90% of the electronic circuits fabricated worldwide are made of silicon using CMOS technology. CMOS technology is the most popular technology because of its low power and less area requirement.

Figure 1.2 describes the IC manufacturing process in a pictorial format. First, the single crystal silicon ingot is grown, which is sliced to obtain wafers. The wafers are the substrate of the IC chip. Now on the wafer, the devices and their interconnections are patterned using the lithography technique. A processed wafer contains several identical ICs called a die. The processed wafer is then tested to identify faulty circuits.

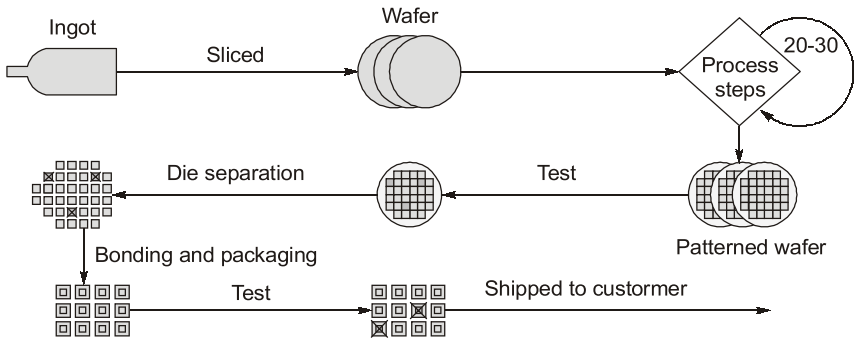


Figure-1.2 *Schematic view of IC technology*

The dies are separated from the wafer and each die is bonded and packaged to form IC chips. These chips are tested to sort out the faulty ones from the manufactured chips, and then the good chips are shipped to the customer site.

The IC is patterned on the wafer using the photolithography technique which is a combination of several process steps, namely, oxidation, coating of photoresist, exposure to UV light, etching, diffusion, ion implantation, film deposition, and metallization.

CHAPTER 2

Crystal Growth, Wafer Fabrication and Basic Properties of Silicon Wafers

2.1 Introduction

Almost from the very beginning, it was clear that silicon was the best choice for the material on which to base this industry. The abundance of silicon, the availability of simple techniques for refining it and growing single crystals, the essentially ideal properties of the Si/SiO_2 interface, and the invention of manufacturing techniques based on the planar process all led to the dominance of silicon based devices by the early 1960s.

The silicon industry depends on a ready supply of inexpensive, high-quality single-crystal wafers. In this chapter we will discuss the methods by which such wafers are prepared and some of the basic properties of these wafers. Integrated circuit manufacturers typically specify physical parameters (diameter, thickness, flatness, mechanical defects like scratches, crystallographic defects like dislocation density, etc.), electrical parameters (N or P type, dopant, resistivity, etc.), and finally, impurity levels (oxygen and carbon in particular) when purchasing wafers. All these parameters must be tightly controlled in order to use the wafers in the high-volume manufacturing of complex chips.

Need of Silicon for VLSI Fabrication

- The fabrication of semiconductor devices has been based on the use of silicon as the premier semiconductor. Two other semiconductors, germanium (Ge) and gallium arsenide (GaAs), present special problems while silicon has certain specific advantages not available with the others.
- At 300°K silicon has a band gap of 1.12 eV, while germanium's band gap is 0.66 eV. Because of this small band gap, the intrinsic carrier density of germanium at $T = 300°K$ is about 2.5×10^{13} cm^{-3}. At temperature of about 400°K, this density becomes 10^{15} cm^{-3} which is comparable to the lower range of doping densities used. This property limits its use to low temperature applications at less than 350°K.
- The other semiconductor of major interest is gallium arsenide. In spite of its attractive electrical properties, gallium arsenide crystals have a high density of crystal defects, which limit the performance of devices made from it.
- Silicon is an abundant element and occurs naturally in the form of sand. It can be refined using simple purification and crystal growth techniques. It also exhibits suitable physical properties for fabricating active devices with good electrical characteristics. In addition silicon can be easily oxidized to form an excellent insulator, (SiO_2) or glass.

- This native oxide is useful, for constructing capacitors and MOSFETs. It also serves as a diffusion barrier that masks against unwanted impurities from diffusing into the high purity silicon material. This masking property allows selective alternation of electrical properties in the silicon.
- Thus active and passive elements can be built on the same piece of material. The components can be interconnected to form a monolithic IC.

2.2 Crystal Structure

In crystalline materials, the atoms are arranged spatially in a periodic fashion. A basic unit cell can be defined as a cell which repeats in all three dimensions. Figure (2.1) illustrates three simple crystal unit cells. All are based on a cubic structure. The body-Centered Cubic or BCC cell has an extra atom in the center of the cube the Face-Centered Cubic or FCC cell has as extra atom in the center of each face of the cube. The dimension *a* is called the lattice constant and is the basic distance over crystal.

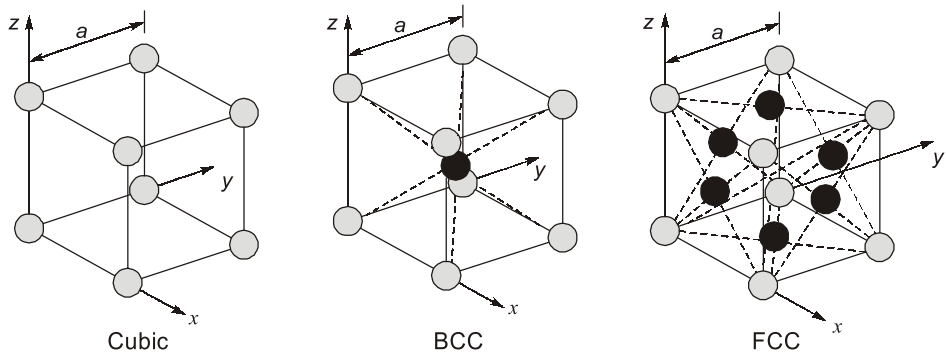


Figure-2.1 : *Unit cells in simple cubic crystals*

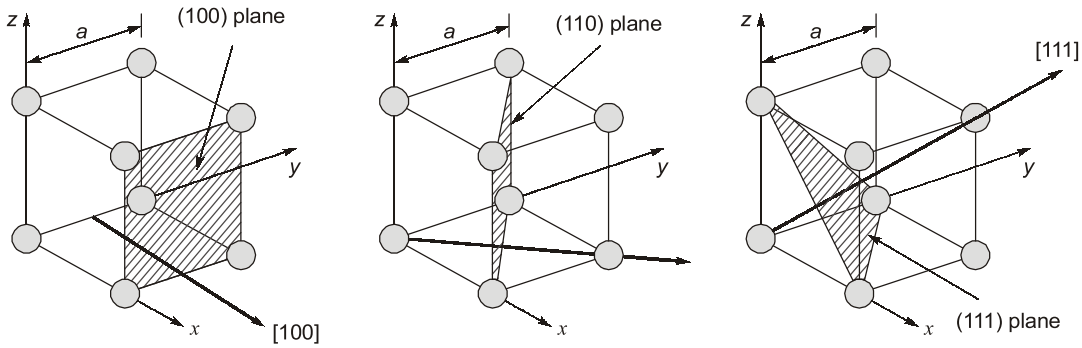


Figure-2.2 : *Crystal planes and major directions for a cubic lattice. The heavy arrows in each case illustrate crystal directions, designated [hkl]. The cross-hatched areas are the corresponding crystal planes ; designated (hkl)*

It is also useful to describe planes in a crystal and convention has been adopted for doing this, Figure (2.2) illustrates three simple planes in a cubic crystal. Such planes are described by Miller indices which are a set of three integers calculated as follows. For a particular plane, the intercepts of that plane with the three crystal axes are determined. In the middle example in Figure (2.2), the intercepts of the (110) plane with the x, y and z-axes are 1, 1 and ∞, respectively. The reciprocals of these three intercepts are then taken, which gives 1/1, 1/1, and 1/∞ simply the (110) plane. (The reciprocals eliminate infinities in the notation.) A minor complication can arise in this procedure if we pick a plane with intercepts outside the basic cell. For examples, if we picked a plane with xyz in intercepts outside the basic unit cell. For example, if we picked a plane with xyz intercepts of 3, 4 and 2

respectively, the reciprocals would be 1/3, 1/4 and 1/2. In this case the smallest set of integers that have the same relative values are chosen for the Miller indices, which would result in the (436) plane in this case. There is also no reason why we could not pick a plane with a negative intercept, for example 1, –1, 2. In this case the reciprocals are 1/1, 1/–1 and 1/2, respectively. The nomenclature in this case places a bar over the corresponding Miller indices, so that this plane becomes the $(2\bar{2}1)$ plane. Finally, as was the case for crystal directions, many crystal planes are also equivalent. The (100), (010) and $(0\bar{1}0)$ planes are all equivalent and are designated as {100} planes. Note that there are conventions which are used here for the style of bracket used to describe crystal directions and planes.

Silicon has a diamond cubic lattice structure, shown in Figure (2.3). This is structure is most easily visualized as two merged FCC lattices with the origin of the second lattice offset from the first by *a*/4 in all three directions. Equivalently, one could think of the structure as an FCC lattice with two atoms at each lattice point, with the two offset from each other by *a*/4 in all three directions. Each atom is individually covalently bonded to four nearest neighbours.

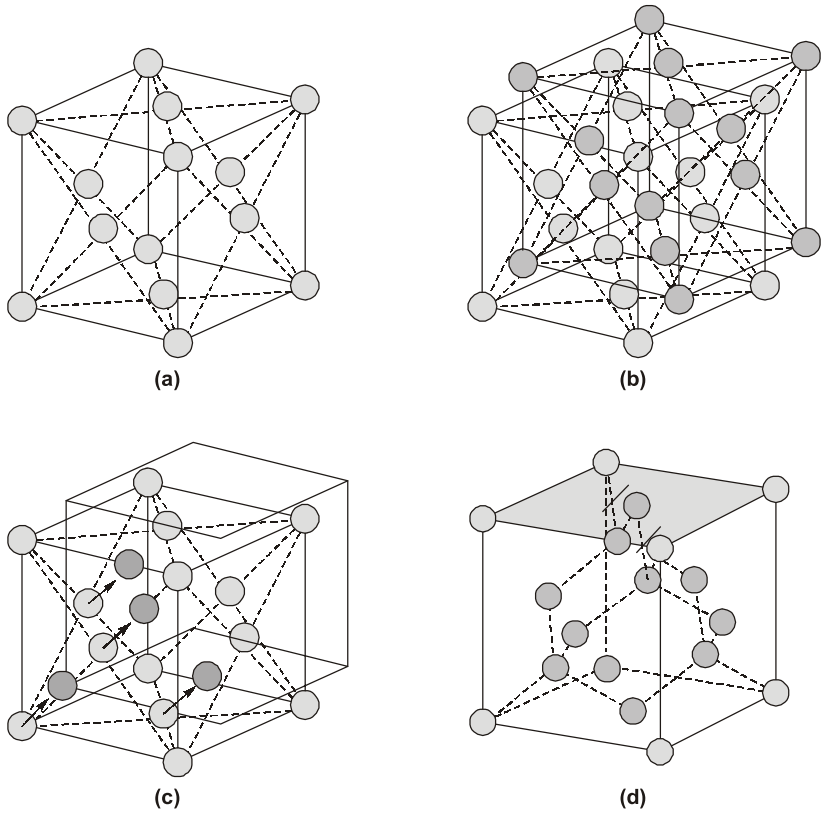


Figure-2.3 : *Diamond crystal structure of silicon. The unit cell may be visualized as two merged FCC cells, offset from each other by a/4 in all three directions. (a) shows the basic FCC unit cell (b) shows two merged cells, offset by a/4*

Figure (2.3) illustrates the construction of the diamond lattice from the two merged FCC lattices.

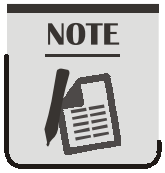
There are two principal silicon crystal orientations that are used in manufacturing integrated circuits, (111) and (100) (meaning that the crystal terminates at the wafer surface on {111} or {100} planes respectively).

Planes in silicon have the largest number of silicon atoms per cm^2, {100} planes the lowest. This results in a number of differences in properties. {111} planes oxidize faster than {100} because the oxidation rate is proportional to the number of silicon atoms available for reaction (Chapter 6).

{111} surfaces have higher densities of electrical defects (interface states) because at least some of these defects are believed to be associated with dangling silicon bonds.

Historically many bipolar technologies used (111) crystals because this orientation is somewhat easier to grow by the Czochralski method described later in this chapter: however as bipolar devices have shrunk in size in recent years, they have become more sensitive to surface properties and increasingly also use (100) wafers.

A final point should be made regarding surface effects on device and process parameters. The CMOS process flow described in Chapter-2 illustrated the fact that many etching, oxidation, and deposition steps are used in modern processes. Such steps can end up producing a very non-planar surface. In other words, the shaping and patterning of the silicon inherent to device fabrication will produce a device surface, which contains {100} surface regions along with almost every other possible crystal orientation. Physical or electrical parameters, which vary with surface orientation, will therefore vary with position in modern ICs. Modelling such effects is only possible with modern computer simulation tools which need to first predict the structure accurately enough to know the surface orientation as a function of position, and then predict the resulting orientation effects on device parameters.



- Angle θ between two planes
  $(U_1\ V_1\ W_1)$ and $(U_2\ V_2\ W_2)$ is $\cos\theta = \dfrac{U_1U_2 + V_1V_2 + W_1W_2}{\sqrt{(U_1^2 + V_1^2 + W_1^2)(U_2^2 + V_2^2 + W_2^2)}}$
- Separation between two adjacent parallel planes (h, k, l) ; $d = \dfrac{a}{\sqrt{h^2 + k^2 + l^2}}$
- Line of intersection between two planes $[U\ V\ W]$
  $U = V_1W_2 - V_2W_1$; $V = W_1U_2 - W_2U_1$; $W = U_1V_2 - U_2V_1$

2.3 Density of Atoms in Plane of Silicon

The lattice constant of Si, a, is 5.43 Å. We have to calculate the number of atoms per unit area (cm^2) on the (100), (110) and (111) planes:

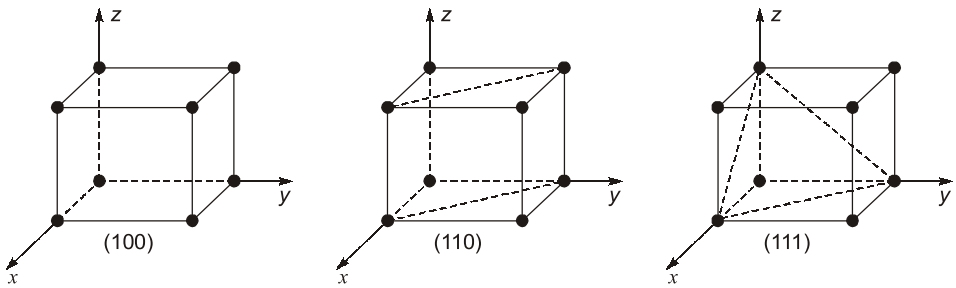


Figure-2.4: *(100), (110) and (111) planes in silicon crystal*

The area of the square of the (100) plane within the unit cell is $A_{100} = a \times a = a^2$

The area of the rectangular region of the (110) plane within the unit cell is $A_{110} = a \times \sqrt{2}a = \sqrt{2}a^2$

The area of the triangular region of the (111) plane within the unit cell is

$$A_{111} = \frac{1}{2} \times \sqrt{2}a \times \frac{\sqrt{3}}{\sqrt{2}}a = \frac{\sqrt{3}}{2}a^2$$

Next, let's determine how many atoms lie on each of these planes within the unit cell.

Characteristic	CZ	FZ
Growth Speed (mm/min)	1 to 2	3 to 5
Crucible	Yes	No
Consumable Material Cost	High	Low
Heat-Up/Cool-Down Times	Long	Short
Axial Resistivity Uniformity	Poor	Good
Oxygen Content (atoms/cm^3)	$> 1 \times 10^{18}$	$< 1 \times 10^{16}$
Carbon Content (atoms/cm^3)	$> 1 \times 10^{17}$	$< 1 \times 10^{16}$
Metallic Impurity Content	Higher	Lower
Bulk Minority Charge Carrier Lifetime (s)	5 – 100	1,000 – 20,000
Production Diameter (mm)	150 – 200	100 – 150

NOTE

For measurement of resistivity of the grown crystal we use Four-point probe method. The resistivity measured is given by

$$\rho = (V/I)2\pi D$$

Where V is applied voltage, I measured current and D is probe spacing.

***Example* - 2.1** A Si ingot with 0.5×10^{16} boron atoms/cm^3 is to be grown by CZ method what should be the concentration of Boron in the melt to obtain the required doping concentration. The segregation coefficient of boron is 0.8.

Solution:

$\because$ $$K_0 = \frac{C_s}{C_l}$$

$\therefore$ $$C_l = \frac{C_s}{K_0} = \frac{0.5 \times 10^{16}}{0.8} \Rightarrow 0.625 \times 10^{16} \text{ atoms/cm}^3$$

Student's Assignments 1

Q.1 A Si ingot with 0.5×10^{16} boron atoms/cm^3 is to be grown by CZ method what should be the concentration of Boron in the melt to obtain the required doping concentration. The segregation coefficient of boron is 0.8.

(a) 0.625×10^{16} (b) 2.4×10^{16}

(c) 1.6×10^{16} (d) 0.5×10^{16}

Q.2 What is the crystal structure of silicon?

(a) Face Centred Cubic

(b) Body Centred Cubic

(c) Diamond

(d) Hexagonal

Q.3 The packing density in an FCC lattice is

(a) 50% (b) 34%

(c) 60% (d) 27%

Q.4 The cleavage plane for silicon is

(a) (100) (b) (110)

(c) (111) (d) (211)