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Microprocessors

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CLASS TEST 2020-2021

ELECTRICAL ENGINEERING

Date of Test : 12/02/2020

ANSWER KEY ➤ Microprocessors

1. (a)	7. (a)	13. (c)	19. (a)	25. (a)
2. (c)	8. (b)	14. (b)	20. (c)	26. (d)
3. (c)	9. (d)	15. (b)	21. (d)	27. (d)
4. (b)	10. (b)	16. (c)	22. (a)	28. (d)
5. (d)	11. (b)	17. (c)	23. (b)	29. (a)
6. (b)	12. (d)	18. (b)	24. (b)	30. (c)

DETAILED EXPLANATIONS

1. (a)

```
MOV H, B      ; H ← B
MOV L, C      ; L ← C
XCHG          ; DE ↔ HL, exchange HL and DE register pair contents
MOV B, H      ; B ← H
MOV C, L      ; C ← L
```

2. (c)

RM is conditional return instruction. When sign flag is set RM is executed with three machine cycles and 12 T-states.

3. (c)

Here register C acts as counter and is loaded with 7. Loop is executed 7-times.
Total T-states = 7 T + 7(4 T) + 6(10 T) + 7 T = 102 T-states

4. (b)

When XRA instruction is executed Sign, Zero, Parity flags are modified to reflect the result of operation with Carry and Auxiliary flags being reset.

5. (d)

LDA 7500 H // Load the contents in location 7500 H to accumulator

CMA //Complement accumulator ($\overline{A}$)

INR A // Increment A by one ($\overline{A}$ + 1)

STA 7500 H // Store contents of accumulator to memory locaton 7500 H

HLT // Halt the program

Contents in location 7500 H are two's complemented.

6. (b)

```
[A] =  0 1 0 1  0 1 1 0
[B] =  1 0 1 0  1 0 0 1          S Z × AC × P × CY
ADD B ⇒ 1 1 1 1  1 1 1 1  ⇒  1 0    0    1    0
        1                1
INR A    0 0 0 0  0 0 0 0  ⇒  0 1    1    1    0
```

INR doesn't effect carry flag.

7. (a)

If the register hold minus five in two's compliment from then in arithmetic shift left the contents of the register shall be

Initial Register content

1	1	0	1	1

= (– 5) in 2's compliment form

After shift left

1	0	1	0	1

= (–10) in 2's comliment form

It is found that the register contents is multiplied by two after logical shift left, left operation. Hence, arithmetic shift left operation is same as logical shift operation.

8. (b)

An instruction cycle consists of several machine cycles.

Hence, option (b) is correct.

9. (d)

$$\begin{array}{r} 8C\ H \\ +\ 7E\ H \\ \hline 1\ 0A\ H \end{array}$$

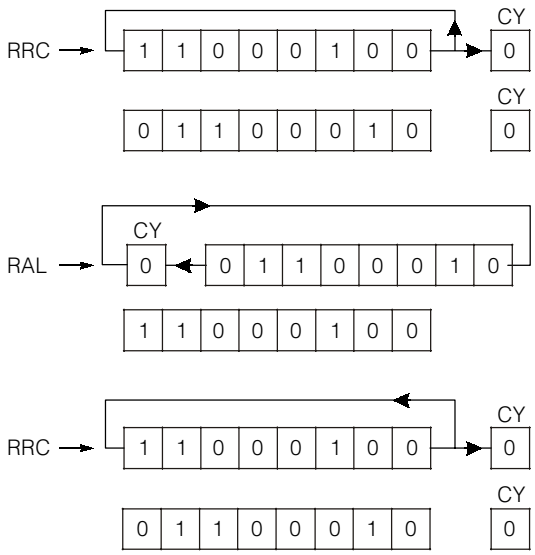
CY = 1

(A) = 0A H

10. (b)

11. (b)

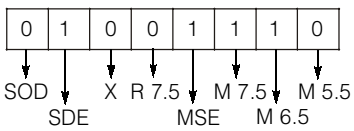
Accumulator is initially loaded with C4 H. Instruction ORA A resets the carry flag



Contents of accumulator are 62 H.

12. (d)

After executing SIM instruction, accumulator set-up for the SIM instruction is shown as



As MSE is enabled, M 7.5 and M 6.5 are masked.

13. (c)

Analysis of code:

```
LXI H, 2200 H     ; Initialize pointer
MOV A, M          ; Get the number 45 H
INX H             ; Increment the pointer
ADD M             ; Add 45 H and 46 H
DAA               ; Convent HEX to valid BCD ; A ← 91 H
STA 2300 H        ; Store the result
HLT               ; Terminate program execution
```

14. (b)

SPHL ; Load contents of HL into stack pointer. This is a one Byte instruction that needs 6 T-states to execute fully.

15. (b)

```
0300 H  :  LXI B, 11FF H
0303 H  :  LXI H, 0307 H
0306 H  :  MVI A, 32 H
0308 H  :  ANA M
```

[AND operation of A with M]

M contains the data of memory location whose address is in HL pair,

Contents of HL pair = 0307 H

Contents of location 0306 H = 0306 H = opcode of MVI A, Data

Contents of location 0307 H = 32 H

∴ A AND with 32 H

```
  00110010
  00110010
  --------
  00110010  =  32 H
         A  =  32 H
```

After the AND operation, CY = 0 and AC = 1

16. (c)

```
        LXI H, 2270 H    ⇒  HL is loaded with 2270 H
        MVI B, 05 H      ⇒  B is loaded with 05 H
        MVI A, 01 H      ⇒  A is loaded with 01 H
STORE : MOV M, A         ⇒  Content of A is moved into location provided by HL pair
        INR A            ⇒  Content of A is incremented by '1'
        INX H            ⇒  Content of HL is incremented by '1'
        DCR B            ⇒  Content of B is decremented by '1'
        JNZ STORE        ⇒  Jump to STORE if Z ≠ 1
        HLT
```

Loop STORE is executed 5 times.

2270 H	01 H
2271 H	02 H
2272 H	03 H
2273 H	04 H
2274 H	05 H
	⋮

∴ The content of 2274 H is 05 H.

17. (c)

LXI D, 0020 H	←	D = 00 H
		E = 20 H = $(32)_{10}$
LOOP : DCX D	←	Decrement content of DE pair by 1
MOV A, D	←	A = 00 always
ORA E	←	logical OR of content E with A
JNZ LOOP		

So, this loop continues till ORA E result is zero i.e. zero flag set so this will happen when content of *E* become zero,

Since initial content of *E* is $(32)_{10}$ so after 32 times execution of DCX it will become zero. So loop will be executed 32 times.

18. (b)

Starting address of RAM is F400H

$$\text{F400H} = \underset{A_{15}}{1}\ \underset{A_{14}}{1}\ \underset{A_{13}}{1}\ \underset{A_{12}}{1}\ \ \underset{A_{11}}{0}\ \underset{A_{10}}{1}\ \underset{A_9}{0}\ \underset{A_8}{0}\ \ \underset{A_7}{0}\ \underset{A_6}{0}\ \underset{A_5}{0}\ \underset{A_4}{0}\ \ \underset{A_3}{0}\ \underset{A_2}{0}\ \underset{A_1}{0}\ \underset{A_0}{0}$$

$A_{12}\,A_{11}\,A_{10}$ are connected to decoder

$\therefore \quad A_{12}\,A_{11}\,A_{10} = 101 = (5)_{10}$

$\therefore$ Y_5 is connected to chip select

$\therefore$ value of *X* is '5'

19. (a)

LXI SP, 9000 ; SP ← 9000

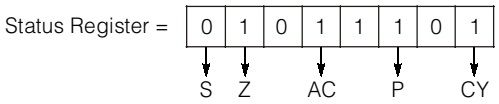
LXI H, 005D ; HL ← 005D

PUSH H ; SP = SP – 2 = 8FFE

POP PSW ; Pop the contents 005D onto PSW register.

PSW = accumulator + status register

PSW = | 00 | 5D |



20. (c)

IO/$\overline{M}$	$\overline{RD}$	$\overline{WR}$		
0	0	0	D_0	
0	0	1	D_1	MEM RD
0	1	0	D_2	MEM WR
0	1	1	D_3	
1	0	0	D_4	
1	0	1	D_5	I/O RD
1	1	0	D_6	I/O WR
1	1	1	D_7	

21. (d)

CY
1

A: | *x* | *x* | *x* | *x* | 0 | 0 | 0 | 0 |

After execution of RRC 4 time

A: | 0 | 0 | 0 | 0 | *x* | *x* | *x* | *x* |

Which is equivalent to dividing by $(10000)_2$ or 16.

22. (a)

The chip select lines A_{14} to A_8 will be set to 1 for chip select.
A_{15} is do not care since it is not connected to chip select so it can be either '0' or '1'.
So, address range will be

	A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0
Initial address	0 or 1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
Final address	0 or 1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

So, address range can be $(7F00)_H$ to $(7FFF)_H$ or $(FF00)_H$ to $(FFFF)_H$ but checking from the option $(7F00)_H$ to $(7FFF)_H$.

23. (b)

$IO/\overline{M}$ is high so its IO operation. $\overline{WR}$ goes low so its a write operation. Hence (b).

24. (b)

Machine cycles of OUT 20 H are
Opcode fetch, memory read (For stored address) and I/O write.

Hence, $\overline{RD}$ = 2 ; $\overline{WR}$ = 1 ; ALE = 3.

25. (a)

	A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0
CC00 :	1	1	0	0	1	1	0	0	0	0	0	0	0	0	0	0
CFFF :	1	1	0	0	1	1	1	1	1	1	1	1	1	1	1	1

chip select

For active low chip select signal, the output of NAND gate should be low. Now, the output of NAND gate becomes low only when all inputs are high. Hence, for the given address range all the inputs of NAND should be $A_{10}\,A_{11}\,\overline{A}_{12}\,\overline{A}_{13}\,A_{14}\,A_{15}$.

26. (d)

LXI B, 2070 H ; loads BC pair with 2070 H with 20 H → B; 70 H → C
MVI A, 8F H ; moves 8 FH to A
MVI C, 68 H ; moves 68 H to C
SUB C ; subtract contents of C from A and store result in A.

$\Rightarrow$ 8 FH

-68 H

27 H

ANI OFH ; OFH is ANDed with contents of A(ie. 27 H) and result is stored in A.

A(27 H) : 00100111

OFH : 00001111

00000111

$\Rightarrow$ A = 07H

STAX B ; stores the contents of 'A' (ie. 07H) at address stored in BC pair (ie. 2070 H)

HLT ; Halts the execution of program.

So, content of memory location 2070 H after execution of program are 07 H.

27. (d)

starting address= 1001 H

ending address = 2016 H

size of memory = (2016 – 1001) H + 1 H

=1016 H = 4118 bytes

28. (d)

HLT is a 1 Byte instruction with 5 T-states or more.

29. (a)

Given, number of T-states in each machine cycle = 3

No. of T-states required in 4 machine cycles = 12

One '*T*' state is precisely equal to one time period of clock signal.

So, time of one T-state is:

$$T = \frac{1}{3}\mu s$$

$\therefore$ Time of 12 T-state

$$= 12\,T = 12 \times \frac{1}{3} = 4\,\mu s$$

30. (c)

The instruction Push B store the contents of BC at stack. The POP PSW instruction copy the contents of BC in to PSW. The contents of register C will be copied into flag register.

D_0 = 1 = carry flag, D_6 = 0 = zero flag.

■■■■