S.No. : 05 BS1_CS_B_280919

Computer Organization

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# CLASS TEST 2019-2020

## COMPUTER SCIENCE & IT

## Computer Organization

Date of Test : 28/09/2019

### *Answer Key*

| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| **1.** | **(a)** | **8.** | **(b)** | **13.** | **(b)** | **19.** | **(d)** | **25.** | **(b)** |
| **2.** | **(c)** | **8.** | **(d)** | **14.** | **(a)** | **20.** | **(d)** | **26.** | **(d)** |
| **3.** | **(c)** | **9.** | **(c)** | **15.** | **(b)** | **21.** | **(b)** | **27.** | **(b)** |
| **4.** | **(d)** | **10.** | **(b)** | **16.** | **(d)** | **22.** | **(a)** | **28.** | **(b)** |
| **5.** | **(c)** | **11.** | **(c)** | **17.** | **(c)** | **23.** | **(b)** | **29.** | **(a)** |
| **6.** | **(b)** | **12.** | **(b)** | **18.** | **(b)** | **24.** | **(b)** | **30.** | **(c)** |

## DETAILED EXPLANATIONS

1. (a)
Since, it uses horizontal micro-programmed that requires 1 bit control / signal.
For 125 control signal, we need 125 bits.
Total number of micro-operation instruction = 215 × 6 = 1290
It requires 11 bit.

2. (c)

| Multiplier | Pair with ($q$ – 1) | Recorder |
|---|---|---|
| 0 | 0 | 0 |
| 1 | 0 | –1 |
| 1 | 1 | 0 |
| 0 | 1 | +1 |
| 1 | 0 | –1 |
| 0 | 1 | +1 |
| 0 | 0 | 0 |
| 1 | 0 | –1 |
| 0 | 1 | +1 |
| 1 | 0 | –1 |
| 1 | 1 | 0 |
| 0 | 1 | +1 |

3. (c)
**When instruction is a computation:**
Memory reference : Fetch instruction
Fetch reference of the operand
Fetch operand
Total 3 memory references.
**When instruction is a branch:**
Memory reference : Fetch instruction
Fetch operand reference and loading program counter
Total 2 memory references.

4. (d)
**RAW hazards:** $I_1 - I_2$, $I_1 - I_4$, $I_2 - I_3$, $I_2 - I_4$, $I_2 - I_5$
**WAW hazards:** $I_2 - I_4$
**WAR hazards:** $I_3 - I_4$ and $I_2 - I_4$

5. (c)
- In pipelined CPU, there will be buffer delays. So, for single instruction non-pipelined CPU takes less time compared to pipelined CPU.
- Structural dependencies cause hazards during pipelining.

6. (b)
**Programmed I/O:** Processor issues an I/O command, on behalf of a processor, to an IO module; that process then busy-waits for the operation to be completed before proceeding.
**Interrupt driven I/O:** The processor isues an IO command on behalf of a process, continues to execute subsequent instruction, and is interrupted by the IO module when the latter has completed its work.
**Direct memory access:** A DMA module controls the exchange of data between main memory and IO module.

8. (b)

For 1 second it take $10^9$ byte

$$\text{So for 64 kbyte it takes} = \frac{64k}{10^9} = 64\ \mu\text{sec}$$

$$\text{Main memory latency} = 64\ \mu\text{sec}$$

$$\text{Total time required to fetch} = 64\ \mu\text{sec} + 64\ \mu\text{sec} = 128\ \mu\text{sec}$$

8. (d)

$$\text{Main memory size} = 32768\ \text{blocks}$$

$$1\ \text{block} = 512\ \text{words}$$

$$= 32768 \times 512\ \text{words} = 2^{15} \times 2^9 = 2^{24}\ \text{words}$$

Main memory takes 24 bits.

Block size = 512 words = $2^9$ words

Number of bits for block size = 9 bits.

Number of blocks in set associative = 128

Number of blocks in one set = 4

$$\text{Number of sets in cache} = \frac{128}{4} = 32 = 2^5$$

Number of bits in set offset = 5 bits

← 24 →

| TAG | SET OFFSET | WORD OFFSET |
|---|---|---|
| 10 | 5 | 9 |

Number of TAG bits = 24 – (9 + 5) = 10 bits.

9. (c)

Consider each statement :

$S_1$ : Microprogrammed control unit uses variable logic to interrupt instruction since its uses encoded scheme for the instruction.

$S_2$ : Horizontal microprogramming control unit does not requires an additional hardware (like a decoder) because a fixed logic is associated with the instructions.

$S_3$ : The performance of a system depends on the direct proportion of memory accesses satisfied by cache.

10. (b)

| 1 bit | 8 bits | 23 bits |
|---|---|---|
| 1 | 10000101 | 11000 ... 0 |
| Sign | Exponent | Mantissa |

$$\text{Bias exponent value} = 10000101$$

$$\text{Actual exponent} = 10000101 - 127 \qquad [\because\ 127 \text{ is bias}]$$

$$= 133 - 127 = 6$$

$$\text{Normalized mantissa bits} = 11000000000000000000000$$

$$\text{Actual value} = 1.11000000000000000000000$$

$$\text{Decimal number} = 1.11000 \times 2^6$$

$$= -(1110000)_2$$

$$= -(112)_{10}$$

11. (c)

Rate of transfer to or from any one disk = 30 MBps.

$$\text{Maximum memory transfer rate} = \frac{4\text{ B}}{10 \times 10^{-9}} = 400 \times 10^{6}\text{Bps} = 400\text{ MBps}$$

Since rate of data transfer = 30 MBps

$$\text{Here number of disk transfer} = \left\lceil \frac{400}{30} \right\rceil = 13$$

Therefore, 13 disks can simultaneously transfer data to or from the main memory.

12. (b)

Biased exponent = 18 + 64 = 82

Representing 82 in binary

$(82)_2 = (1010010)_2$

Representing mantissa in binary

$(0.625)_{10} = (0.10100000)$

Floating point representation is as follows:

| Sign bit | Exponent | Mantissa |
|---|---|---|
| 0 | 1010010 | 10100000 |

5 2 A 0

13. (b)

Memory mapped I/O uses the same address bus to address both memory and I/O devices the memory and registers of the I/O devices are mapped to address values.

So, when an address is accessed by the CPU, it may refer to a portion of physical RAM, but it can also refer to memory of I/O device.

14. (a)

$$\text{Number of lines} = \frac{64K}{32} = 2^{11}$$

$$\text{Number of sets} = \frac{2^{11}}{4} = \frac{2^{11}}{2^{2}} = 2^{9}$$

32 bits

| Tag | SO | WO |
|---|---|---|
| 18 bits | $\log_2 2^9 = 9$ | $\log_2 32 = 5$ bit |

$$\begin{aligned}
\text{Tag memory size} &= S \times P \times \#\text{ tag bits} \\
&= 2^9 \times 4 \times (18 + 1 + 1 + 2) \\
&= 2^9 \times 2^2 \times 22 \text{ bits} \\
&= 2^{10} \times 2 \times 22 \text{ bits} \\
&= 44 \text{ K bits}
\end{aligned}$$

15. (b)

Considering each statement :

$S_1$ : Delayed control transfer, also known as delayed branching, is an attempt to cope with control hazards.

$S_2$ : The branch target stores the previous target address for the current branch, other algorithms for branch prediction also exist.

$S_3$ : For any given instruction set architecture implemented on a *N*-stage pipelined processor, *N* registers probably is not enough registers to completely prevent structural hazards involving a shortage of register hardware.

16. (d)

| | IF | ID | OF | PD & WB |
|---|---|---|---|---|
| $I_1$ : | 1 m-ref | 3 m-ref | 2 m-ref | — |
| $I_2$ : | 1 m-ref | 1 m-ref | 1 m-ref | — |
| $I_3$ : | 1 m-ref | — | 1 m-ref | 2 cycles |
| $I_4$ : | 1 m-ref | — | — | 2 m-ref |
| $I_5$ : | 1 m-ref | 3 m-ref | — | 2 m-ref |
| $I_6$ : | 1 m-ref | — | — | — |

$$\text{Total time} = 80 \text{ cycles} \times 0.5 \text{ ns} = 40 \text{ ns}$$

17. (c)

2.5 memory reference per instruction $\Rightarrow \dfrac{1000}{2.5}$ instruction per 1000 reference.

$\Rightarrow$ 400 instructions.

Now

$$200 = \left(\frac{260}{400}\right)x + \left(\frac{120}{400}\right)2x$$

$$x = \frac{400 \times 200}{500}$$

$$x = \frac{80000}{500}$$

$$x = 160$$

$$2x = 320$$

18. (b)

$D_1$ : Number of stages, $k = 5$

$\tau_i = 3, 2, 4, 2, 3$ ns

$i = 1$ to $5$

$\tau = \max(\tau_i) + d$ here $d$ is negligible

$\tau = 4$ ns

$D_2$ : Number of stages, $k = 8$

$\tau_i = 2$ ns each

$i = 1$ to $8$

$\tau = \max(\tau_0) = 2$ nsec

Number of instructions, $n = 100$

$D_1$: $T_k = (n + k - 1)\tau$

$= (100 + 5 - 1) \times 4$

$= 104 \times 4 = 416$ ns

$D_2$: $T_k = (n + k - 1)\tau$

$= (100 + 8 - 1) \times 2$

$= 107 \times 2 = 214$ ns

Total time saved $= 416 - 214 = 202$ ns

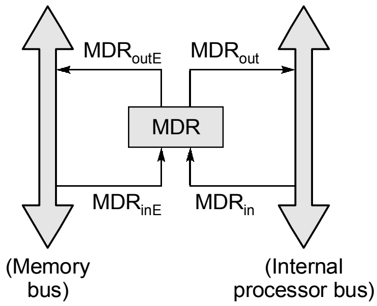
19. (d)

Increasing the cache line size brings in more from memory when a miss occurs. If accessing a certain byte suggests that nearby bytes are likely to be accessed soon (locality), then increasing the cache line essentially prefetches those other bytes. This, in turn, forestalls a later cache miss on those other bytes. If misses occur because the cache is too small, then the designers should increase the size!
Conflict misses occur when multiple memory locations are repeatedly accessed but map to the same cache location. Consequently, when they are accessed, they keep kicking one another out of the cache. Increasing the associativity implies that each chunk of the cache is effectively doubled so that more than one memory item can rest in the same cache chunk.

20. (d)

Considering each statement :

$S_1$ : 4-control signals are needed for each data register.




MDR is directly connected to data lines of the processor. It has 2 input and 2 output. Data may be loaded into MDR either from memory or from internal bus. Data present in MDR may be placed on either bus are memory. It requires total 4 control signals.

$S_2$ : The main disadvantage of direct mapping is that cache hit ratio decreases sharply if two or more frequently used blocks map on the same region.

21. (b)

| Stages of Pipeline | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| WB | | | | | $I_1$ | | | $I_2$ | | | $I_3$ | $I_3$ | $I_4$ |
| EX | | | | $I_1$ | | $I_2$ | $I_2$ | $I_3$ | $I_3$ | $I_3$ | $I_4$ | $I_4$ | |
| ID | | $I_1$ | $I_1$ | $I_2$ | $I_2$ | $I_3$ | – | $I_4$ | $I_4$ | $I_4$ | | | |
| IF | $I_1$ | $I_2$ | – | $I_3$ | $I_3$ | $I_4$ | – | | | | | | |

Number of Clock Cycles

22. (a)

Number of bits for control signals in vertical programming:

$$\log_2(2) + \log_2(1) + \log_2(4) + \log_2(27) + \log_2(17)$$
$$= 1 + 1 + 2 + 5 + 5 = 14 \text{ bits}$$

256 CW = 8 bits

VCW:

| Branch condition | Flag | Control field | Control memory address |
|---|---|---|---|
| | | 14 | 8 |

$$\text{VCW size} = 14 + 8 = 22 \text{ bits}$$

$$\text{Vertical control memory size} = 256 \times 22 \text{ bits}$$
$$= \frac{256 \times 22}{8} \text{ bytes} = 704 \text{ bytes}$$

23. (b)

$$\text{The required probability} = {}^{10}C_3 (0.35)^3 (0.65)^7 = 0.252$$

24. (b)

Time taken by I/O device = $\frac{16\text{ MB}}{128\text{ kB}} = 128\text{ sec}$

Percentage time CPU is busy = $\frac{128}{128+28} \times 100 = 82.05$

25. (b)

I/O ports are placed at addresses on bus and are accessed just like other memory location in computers that uses memory mapped I/O.

26. (d)

$$\begin{array}{r} 10001110 \\ 10000000 \\ \hline \text{Sum} = 100001110 \\ \hline \end{array}$$

Z = 0, C = 1, O =1, S = 0

27. (b)

| | 4 | 3 | 4 | 3 |
|---|---|---|---|---|
| op code | Source data | | Destination | |
| | Mode | R | Mode | R |

Register = 5 = 3 bits

Modes = 14 =4 bits

| Type | Single operand or No operand | Double operand |
|---|---|---|
| Arithmetic (10) | 2 | 8 |
| Logic (15) | 9 | 6 |
| Data moving (20) | 12 | 8 |
| Branch (10) | 5 | 5 |

Total 27 double operands = 5 bits

Size of instruction word = 5 + 7 + 7 = 19

28. (b)

The device generates 8 × 1024 = 8192 bytes/sec

i.e. 1 second 8192 bytes

$$\text{for 1 byte} \Rightarrow \frac{1}{8192}\text{sec}$$

$$\Rightarrow 122\ \mu\text{s}$$

Given that each interrupt consumes 100 μs.

∴ Fraction of processor time consumed in = $\frac{100}{122}$ (for every byte) = 0.82

29. (a)

Average access time for both read and write operations.

$$= 0.4 \times 79.1\text{ ns} + 0.6 \times 84.2\text{ ns} = 61.952\text{ ns}$$

$$\eta_{memory} = \frac{1}{61.952} = 161.4\text{ Mega words/sec.}$$

30. (c)

- Main disadvantage of direct mapping is that cache hit ratio decreases sharply if two or more frequently used blocks map on to same region.
- Because each and every WRITE operation is done simultaneously on both cache and main memory. WRITE THROUGH results in more cache cycles than WRITE BACK.

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