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Microprocessors

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CLASS TEST 2019-2020

ELECTRICAL ENGINEERING

Date of Test : 26/08/2019

ANSWER KEY ➤ Microprocessors

1. (c)	7. (b)	13. (d)	19. (d)	25. (c)
2. (d)	8. (c)	14. (a)	20. (a)	26. (a)
3. (a)	9. (b)	15. (b)	21. (a)	27. (d)
4. (d)	10. (d)	16. (d)	22. (d)	28. (b)
5. (a)	11. (a)	17. (d)	23. (d)	29. (a)
6. (c)	12. (c)	18. (c)	24. (a)	30. (c)

Detailed Explanations

1. **(c)**

TRAP is also called as RST 4.5

Vector address = $(4.5 \times 8)_{10} = (36)_{10}$

= $(24)_H = (0024)_H$.

TRAP is a positive edge triggered and level triggered interrupt.

RST 6.5 is a level triggered interrupt with third highest priority.

INTR is a level triggered interrupt.

2. **(d)**

LDA 7500 H// Load the contents in location 7500 H to accumulator CMA//Complement accumulator ($\overline{A}$)

INR A// Increment A by one ($\overline{A}$ + 1)

STA 7500 H// Store contents of accumulator to memory locaton 7500 H

HLT// Halt the program

Contents in location 7500 H are two's complemented.

3. **(a)**

If the register hold minus five in two's compliment from then in arithmetic shift left the contents of the register shall be

Initial Register content

1	1	0	1	1

= (– 5) in 2's compliment form

After shift left

1	0	1	0	1

= (–10) in 2's comliment form

It is found that the register contents is multiplied by two after logical shift left, left operation.
Hence, arithmetic shift left operation is same as logical shift operation.

4. **(d)**

$$\begin{array}{r} 8C\ H \\ +\ 7E\ H \\ \hline 1\ 0A\ H \end{array}$$

CY = 1

(A) = 0A H

6. **(c)**

RM is conditional return instruction. When sign flag is set RM is executed with three machine cycles and 12 T-states.

7. (b)

Memory chip has 10 address lines and 8 data lines. As control enable is active low and given to NAND gate output. For chip to be enabled A_{15}, A_{14}, A_{13}, A_{12}, A_{11} and A_{10} has to be ones.

A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	Address
1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	$(FC00)_H$
1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	1	
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	$(FFFF)_H$

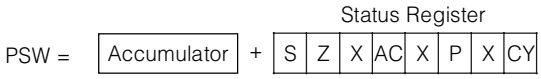
8. (c)

Here register C acts as counter and is loaded with 7. Loop is executed 7-times.

Total T-states = 7 T + 7(4 T) + 6(10 T) + 7 T = 102 T-states

9. (b)

PSW register can be seen as accumulator register with flag register.



contents of register B are added to register A and the result is stored in register A. Here the flags get affected as ADD is an arithmetic instruction.

$\therefore$ PSW = 0000000001X1X1X1

'X' is a don't care bit

PSW = 0000000001110101

10. (d)

Total five memory accesses are involved when the instruction LHLD 2000 is executed by the microprocessor one Op-code fetch cycle and four memory read cycles.

11. (a)

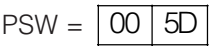
LXI SP, 9000 ; SP ← 9000

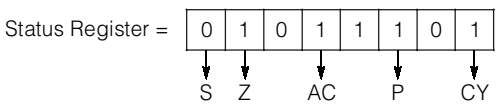
LXI H, 005D ; HL ← 005D

PUSH H ; SP = SP – 2 = 8FFE

POP PSW ; Pop the contents 005D onto PSW register.

PSW = accumulator + status register





12. (c)

IO/$\overline{M}$	$\overline{RD}$	$\overline{WR}$		
0	0	0	D_0	
0	0	1	D_1	MEM RD
0	1	0	D_2	MEM WR
0	1	1	D_3	
1	0	0	D_4	
1	0	1	D_5	I/O RD
1	1	0	D_6	I/O WR
1	1	1	D_7	

13. (d)

CY
1

A:

x	*x*	*x*	*x*	0	0	0	0

After execution of RRC 4 time

A:

0	0	0	0	*x*	*x*	*x*	*x*

Which is equivalent to dividing by $(10000)_2$ or 16.

14. (a)

The chip select lines A_{14} to A_8 will be set to 1 for chip select.
A_{15} is do not care since it is not connected to chip select so it can be either '0' or '1'.
So, address range will be

	A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0
Initial address	0 or 1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
Final address	0 or 1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

So, address range can be $(7F00)_H$ to $(7FFF)_H$ or $(FF00)_H$ to $(FFFF)_H$ but checking from the option $(7F00)_H$ to $(7FFF)_H$.

15. (b)

Machine cycles of OUT 20 H are
Opcode fetch, memory read (For stored address) and I/O write.

Hence, $\overline{RD}$ = 2 ; $\overline{WR}$ = 1 ; ALE = 3.

16. (d)

LXI B, 2070 H ; loads BC pair with 2070 H with 20 H → B; 70 H → C
MVI A, 8F H ; moves 8 FH to A
MVI C, 68 H ; moves 68 H to C
SUB C ; subtract contents of C from A and store result in A.

$$\Rightarrow \quad \begin{array}{r} 8\ FH \\ -68\ H \\ \hline 27\ H \end{array}$$

ANI OFH ; OFH is ANDed with contents of A(ie. 27 H) and result is stored in A.

$$\begin{array}{rl} A(27\ H): & 00100111 \\ OFH: & \underline{00001111} \\ & 00000111 \end{array}$$

$\Rightarrow$ A = 07H
STAX B ; stores the contents of 'A' (ie. 07H) at address stored in BC pair (ie. 2070 H)
HLT ; Halts the execution of program.
So, content of memory location 2070 H after execution of program are 07 H.

17. (d)

XRA M : It is a 1 byte instruction, uses indirect addressing mode and requires two machine cycles (OP + MR). 7T-states are required.

STC : 1-byte instruction, one machine cycle and 4T-states are required.

LHLD 16 bit address
: It is a 3-byte instruction, require 5 machine cycles (OP + MR + MR + MR + MR) & 16 T-states

DAD R_P : It is a 1-byte instruction, require 3 machine cycles and 10 T-states

18. (c)

Program counter (PC) is a 16-bit special purpose register which stores the address of next instruction to be executed or next byte to be fetched from memory. It is incremented automatically after fetching each byte from the memory.

19. (d)

20. (a)

Given, number of T-states in each machine cycle = 3
No. of T-states required in 4 machine cycles = 12
One '*T*' state is precisely equal to one time period of clock signal.
So, time of one T-state is:

$$T = \frac{1}{3}\mu s$$

∴ Time of 12 T-state

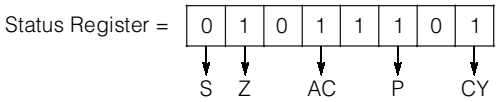
$$= 12\ T = 12 \times \frac{1}{3} = 4\ \mu s$$

21. (a)

```
LXI SP, 9000      ; SP ← 9000
LXI H, 005D       ; HL ← 005D
PUSH H            ; SP = SP – 2 = 8FFE
POP PSW           ; Pop the contents 005D onto PSW register.
```

PSW = accumulator + status register

PSW = | 00 | 5D |



22. (d)

For enabling the decoder, output of NAND should be low and output of NAND gate is low when the address lines A_{13} to A_{15} are high. And for generation of chip select signal the output line Y_5 of decoder should be selected. Line Y_5 is selected when address lines A_{10} = 1.

$A_{11} = 0$

and $A_{12} = 1$

So, for the selection of given RAM,

$A_{10} = 1,$

$A_{11} = 0,$

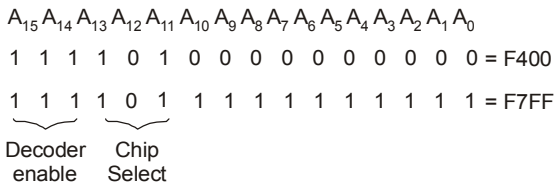
$A_{12} = 1,$

$A_{13} = 1,$

$A_{14} = 1,$

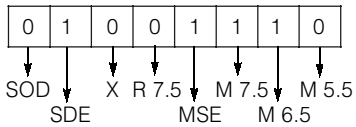
$A_{15} = 1$

Hence, address range will be as follows.



23. (d)

After executing SIM instruction, accumulator set-up for the SIM instruction is shown as



As MSE is enabled, M 7.5 and M 6.5 are masked.

24. (a)

This program multiply Bytel by 10. Hence content of A will be 46H.

$07H = 07_{10}$, $7 \times 10 = 70$, $70_{10} = 46H$.

25. (c)

Analysis of code:

```
LXI H, 2200 H    ; Initialize pointer
MOV A, M         ; Get the number 45 H
INX H            ; Increment the pointer
ADD M            ; Add 45 H and 46 H
DAA              ; Convent HEX to valid BCD ; A ← 91 H
STA 2300 H       ; Store the result
HLT              ; Terminate program execution
```

26. (a)

The code performs 2's complement of an 8-bit number. 87 H is loaded in accumulator and is complemented. Contents are incremented by one. The result [2's complement] is stored in C051 H location.

27. (d)

$A \leftarrow (A7)_H$

$A \rightarrow 10100111$

$A \rightarrow 10100111$

Bitwise or $\rightarrow 10100111$

after ORA A instruction is executed sign flag is set.

sequence jumps to OUTPRT

$\overline{A} \rightarrow 01011000$

$\overline{A} + 1 \rightarrow 01011001$

Finally $(59)_H$ is displayed at Port 01 H.

28. (b)

```
MVI B, 33 H    ; B ← 33 H
MVI C, 40 H    ; C ← 40 H
PUSH B         ; PUSH the contents of BC pair on to stack
POP H          ; POP the contents of stack into HL pair
SHLD C050      ; Contents of HL are stored in locations C050 and C051 respectively
HLT            ; Halt
```

Finally the contents of C050 are 40 H and C051 are 33 H respectively.

29. (a)

Size of one memory chip = 256×1 bits

Required memory size = 1 kB

$$\text{Total chips required} = \frac{1024 \times 8 \text{ bits}}{256 \times 1 \text{ bits}} = 32$$

30. (c)

The loop is executed four times adding the contents of accumulator with decremented contents of register B.

$A = 04 + 04 + 03 + 02 + 01 + 02$

$A = (16)_{10}$

$A = (10)_H$

■■■■