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Digital Electronics

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CLASS TEST 2019-2020

ELECTRICAL ENGINEERING

Digital Electronics

Date of Test : 20/05/2019

Answer Key

1.	(d)	7.	(b)	13.	(d)	19.	(c)	25.	(a)
2.	(b)	8.	(*)	14.	(c)	20.	(b)	26.	(a)
3.	(c)	9.	(d)	15.	(c)	21.	(d)	27.	(a)
4.	(a)	10.	(a)	16.	(a)	22.	(a)	28.	(c)
5.	(d)	11.	(a)	17.	(a)	23.	(a)	29.	(a)
6.	(b)	12.	(a)	18.	(a)	24.	(b)	30.	(d)

DETAILED EXPLANATIONS

1. (d)

Given 12 bit content in excess 3 form

$$1000\ 1001\ 0111 = 897 - 333 = 564$$

3. (c)

Dual of Ex-OR is Ex-NOR. Also, complement of Ex-OR is Ex-NOR whihc is dual of Ex-OR.

4. (a)

CLK	State	Serial in
X	0 0 1 1	0
1	0 0 0 1	1
2	1 0 0 0	

5. (d)

Output of stage 1 X⊕X = 0

Output of 2nd stage 1 ⊕ 0 = 1

Output Y = 1 ⊕ 0 = 1

6. (b)

Minimum number of FF required,

$$2^n \geq \text{Mod no.}$$

$$\therefore \quad 2^n \geq 128$$

$$n = 7$$

8. (*)

$\overline{(A\cdot\bar{B}+\bar{C})D+\bar{E}}$

$\overline{(A\cdot\bar{B}+\bar{C})D}\cdot E$

$\left(\overline{(A\cdot\bar{B}+\bar{C})}+\bar{D}\right)E$

$\left(\left(\overline{A\cdot\bar{B}}\cdot C\right)+\bar{D}\right)E$

$\left((\bar{A}+B)\cdot C+\bar{D}\right)E$

9. (d)

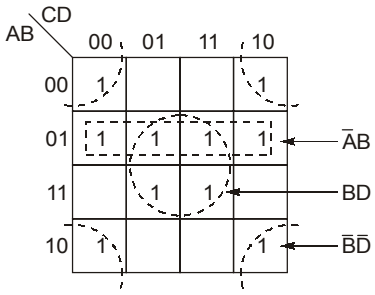
$$(1010) = 10_{10} \text{ gives } 3\text{ V}$$

$$\therefore \quad \text{Step size} = \frac{3V}{10} = 0.3\text{ V}$$

$$\text{Output voltage fof } 0100 = (=4_{10}) \text{ is} = 4 \times 0.3 = 1.2\text{ V}$$

10. (a)

k map

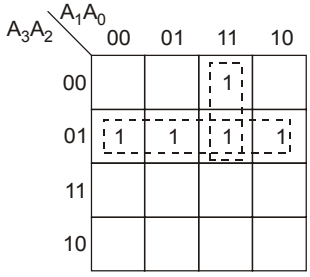


$\therefore \quad f = BD + \bar{A}B + B\bar{D}$

11. (a)

A_3	A_2	A_1	A_0	y
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	1
0	1	0	0	1
0	1	0	1	1
0	1	1	0	1
0	1	1	1	1
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	0
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	0

k-map simiplification



$$y = \bar{A}_3A_2 + \bar{A}_3A_1A_0 = \bar{A}_3(A_2 + A_1A_0)$$

12. (a)

$$x = (M+N)(\bar{M}+P)(\bar{N}+\bar{P})$$

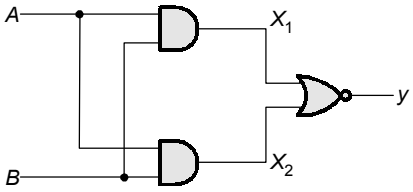
$$= \left(M\bar{M} + MP + N\bar{M} + NP\right)(\bar{N}+\bar{P})$$

$$= \left(MP + N\bar{M} + NP\right)(\bar{N}+\bar{P})$$

$$= MP\bar{N} + MP\bar{P} + N\bar{M}\bar{N} + N\bar{M}\bar{P} + NP\bar{N} + NP\bar{D}$$

$$x = MP\bar{N} + N\bar{M}\bar{P}$$

13. (d)



$X_1 = AB$

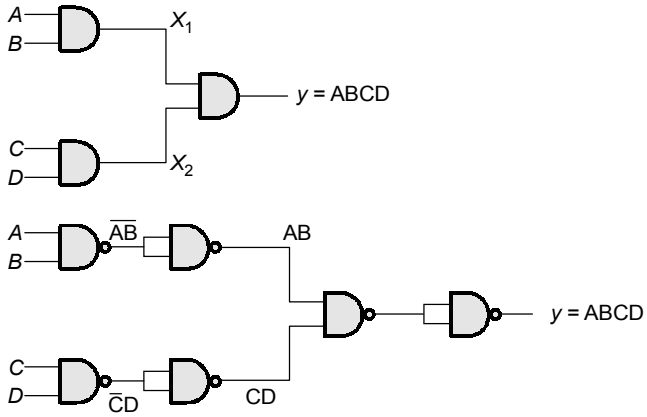
$X_2 = AB$

$y = \overline{AB + AB} = \overline{AB}$

A	B	$y = \overline{AB}$
0	0	1
0	1	1
1	0	1
1	1	0 → LED will be ON

14. (c)

Implementing y suing 2 input AND gates



∴ Hence total 6, 2 input NAND gates are required.

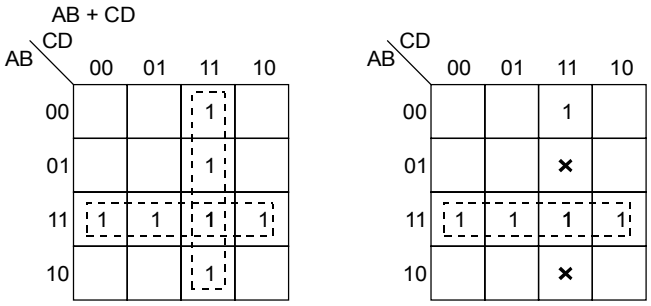
15. (c)

The expression of output is

$$r = (\bar{A} + B)(A + \bar{B}) = A\bar{A} + \bar{A}\bar{B} + AB + B\bar{B} = AB + \bar{A}\bar{B} = A \odot B$$

16. (a)

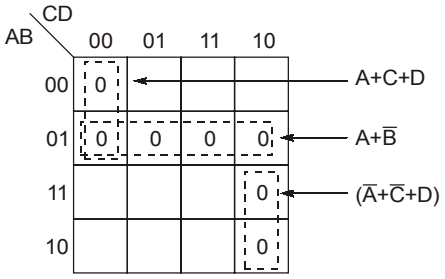
k-map



Comparing both the k-maps, it to clear that there are two don't care enteries. Which are (7, 11).

17. (a)

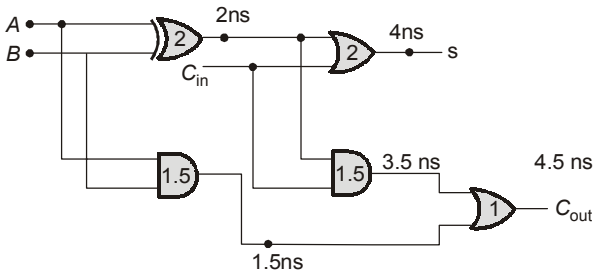
Drawing k-map for x.



$$\therefore \quad x = (A + C + D)(\bar{A} + \bar{C} + D)(A + \bar{B})$$

18. (a)

Full adder implementation



$$s = A \oplus B \oplus C$$

$$C_{out} = (A \oplus B)\, C_{in} + AB$$

From figure, it is clear that delay for sum and carry will be 4ns and 4.5ns respectively.

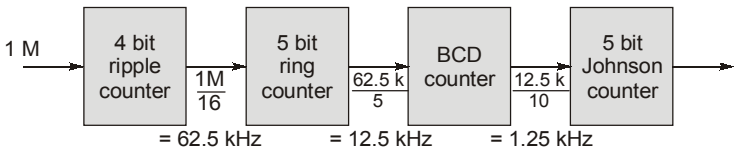
19. (c)

4 bit ripple ripple counter has $2^4 = 16$ states

5 bit ring counter has 5 states

BCD counter has 10 states

5 bit Jhonson counter has $5 \times 2 = 10$ states



$$\text{FOS} = \frac{1250}{10} = 125\ \text{Hz}$$

21. (d)

Propagation delay

$$T_d = (n-1)\, t_{p\,\text{carry}} + \max\,(t_{p\,\text{carry}}.\ t_{p\,\text{sum}})$$
$$= (16-1) \times 5 + \max\,(5.6)$$
$$= 75 + 6 = 81\ \text{ns}$$

22. (a)

For given quadratic equation,

$$(x-3) = 0$$

and $(x-6) = 0$ will be two factors

$\therefore$ $(x-3)(x-6) = x^2 - 11x + 22$ both are equal

$\therefore$ $x^2 - (6+3)x + 6\times 3 = x^2 - 11x + 22$

Let b be the base of number

$$6 + 3 = 1b + 1$$

$$b = 8$$

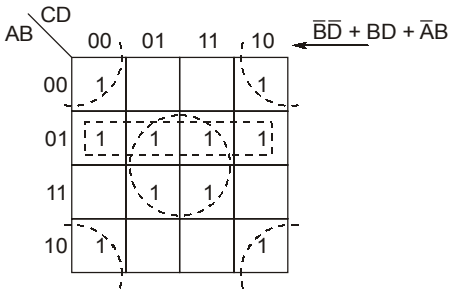
Also, $6\times 3 = 2b + 2$

$$18 = 2b + 2$$

$$b = 8$$

23. (a)

k map



24. (b)

Let n number of flip flop cascaded each having propagation delay of t_{pd}.

Frequency of operation

$$\frac{1}{nt_{pd}} \geq 10\ \text{MHz}$$

$\therefore$ $$n \leq \frac{1}{t_{pd}\times 10\ \text{MHz}} \leq \frac{1}{12\times 10^{-9}\times 10^{7}} \leq \frac{100}{12}$$

$$n = 8$$

For $n = 8$ MOD number of counter $2^8 = 256$

25. (a)

When odd number of NOT gate are arranged with output as a feedback to input it acts as an oscillator with frequency,

$$f = \frac{1}{2nt_{pd}} \quad n = \text{Number of NOT gates}$$

$\therefore$ $$f = \frac{1}{2\times 5\times t_{pd}}$$

$\therefore$ $$t_{pd} = \frac{1}{10\times f_{max}} = \frac{1}{10\times 20}\,\mu s = \frac{1000}{10\times 20}\,\mu s = 5ns$$

$\therefore$ Each NOT gate has a propagation delay of 5 ns.

26. (a)

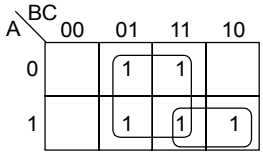
Expression of E.

$$E = \bar{A}O + A \cdot B = AB$$

$$y = \bar{E}C + E.1 = \overline{AB}C + AB$$

$$= (\bar{A} + \bar{B})C + AB = \bar{A}C + \bar{B}C + AB$$

k-map simplification



$$y = C + AB$$

27. (a)

An eight bit binary ripple counter will be RESET i.e. initial condition 00000000 after

= (Mod number - Current state)

= 256 – 127 $(0111 \quad 1111 = 127_{10})$

= 129 clock pulses

∴ i.e. after 129 clock pulses counter will be at $(00)_{10}$.

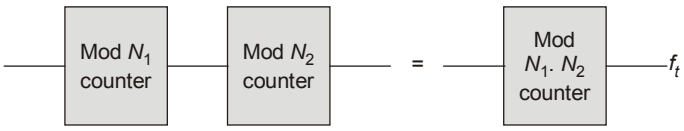
After additional (135 – 129) = 6 pulses counter will be at 0000 0110 state.

28. (c)

(i) n bit Johnson counter will have $2n$ states

∴ 3bit Johnson counter has mod number = 3 × 2 = 6

In 2nd stage, D -Fup flop acts as a T-flip flop and has mod no. 2



Hence given counter arrangement has 6 × 2 = 12 mod number

29. (a)

Full scale voltage = Step size × Maximum count

= Step size × $(2^n - 1)$

= 10 mV × 255

= 2.55 V

$$\% \text{ Resolution} = \frac{1}{2^n - 1} \times 100 = \frac{100}{255} = 0.392\%$$

30. (d)

Number of function using n variables is 2^{2^n}.

Since, here $n = 3$, so number of function is 256.

■■■■