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ESE 2026 : Prelims Exam
CLASSROOM TEST SERIES

E & T ENGINEERING

Test 2

Section A : Network Theory

Section B : Digital Circuits

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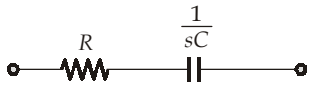
Section A : Network Theory

1. (c)

$$Y(s) = \frac{2s}{s+1}$$

$$Y(s) = \frac{1}{Z(s)} \quad \Rightarrow \quad Z(s) = \frac{s+1}{2s} = \frac{1}{2} + \frac{1}{2s}$$

For a series RC circuit,



$$Z(s) = R + \frac{1}{sC}$$

On comparing, $R = \frac{1}{2}\Omega$

$C = 2F$

Hence, the network consists of a $2F$ capacitor in series with a 0.5 Ω resistor.

2. (b)

Given, $\omega_0 = 10^4$; $Q = 50$; $R = 100\ \Omega$

For a parallel RLC circuit, the quality factor is,

$$Q = \frac{R}{\omega_0 L} = \omega_0 RC$$

$\Rightarrow \quad 50 = 10^4 \times 100 \times C$

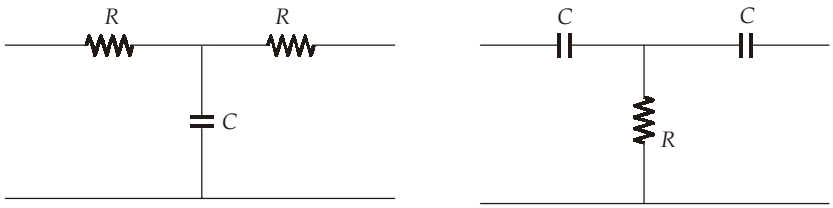
$\Rightarrow \quad C = \frac{50}{10^6}$

$\Rightarrow \quad C = 50\ \mu F$

Hence, the value of the capacitor $C = 50\ \mu F$

3. (b)

The given Twin-T network can split into,

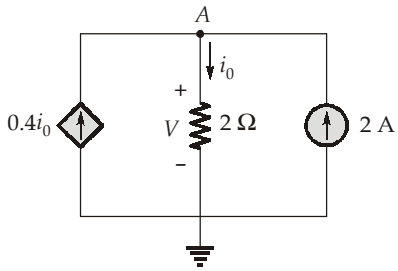


Low-pass network High-pass network

The combination of these two networks forms a notch filters, which exhibits a very high impedance at a specific frequency, thereby attenuating that frequency.

4. (c)

Given circuit,



Applying KCL at node A,

$$-0.4i_0 + i_0 - 2 = 0$$
$$0.6i_0 = 2$$

$$\Rightarrow \quad i_0 = \frac{2}{0.6} = 3.33\text{A}$$

Let 'V' be the voltage across the 2 Ω resistor: $V = i_0 \times 2 = 3.33 \times 2 = 6.66$ V

$\therefore$ The dependent source delivers power,

$$P_d = 0.4i_0 \times V = 0.4 \times 3.33 \times 6.66 = 8.87 \text{ W}$$

5. (b)

From the given pole-zero plot,

$$Z(s) = \frac{k(s+3)}{(s+1-j)(s+1+j)}$$

$$Z(s) = \frac{k(s+3)}{s^2+2s+2}$$

Given, $Z(0) = 3$ i.e., $Z(s)\big|_{\text{at } s=0} = 3$

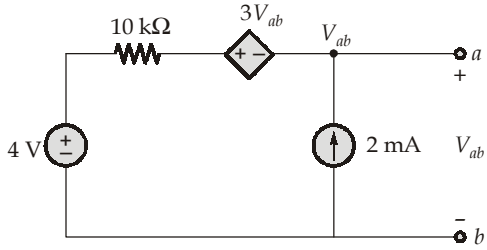
$$3 = \frac{k(3)}{2} \quad \Rightarrow \quad k = 2$$

Thus,

$$Z(s) = \frac{2(s+3)}{s^2+2s+2}$$

6. (c)

Given circuit:



By applying the nodal equation at node 'a':

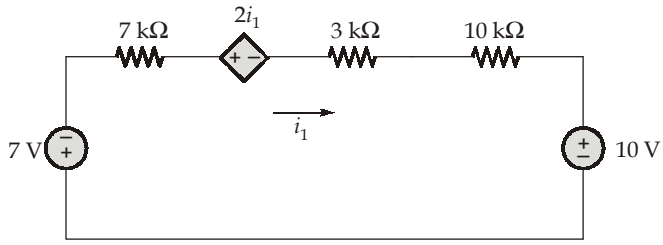
$$-2\text{mA} + \frac{V_{ab} + 3V_{ab} - 4}{10k} = 0$$

$$4V_{ab} - 4 = 20$$
$$4V_{ab} = 24$$
$$\Rightarrow \quad V_{ab} = 6 \text{ V}$$

Hence, the terminal voltage, $V_{ab} = 6$ V

7. (c)

Given network can be simplified by using the source transformation theorem.



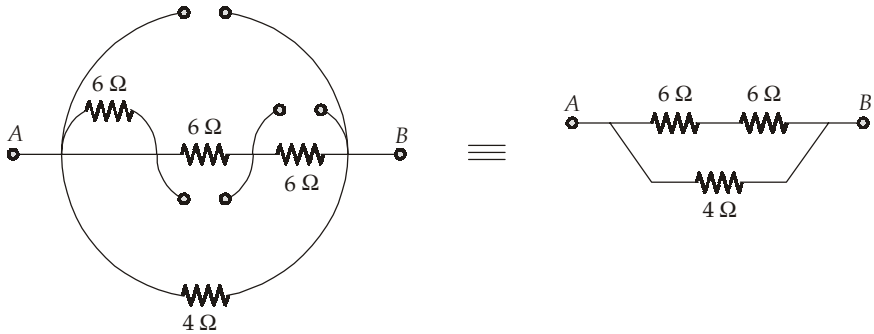
Using KVL:
$$i_1 = \frac{-7 - 10 - 2i_1}{20k}$$
$$20 \times 10^3 \times i_1 = -17 - 2i_1$$
$$20{,}002 i_1 = -17$$
$$\Rightarrow \quad i_1 = \frac{-17}{20{,}002} = -0.85 \text{ mA}$$

Hence, the current $i_1 = -0.85$ mA

8. (d)

When finding the Norton resistance replace all independent sources with their internal resistances (i.e., voltage sources are short-circuited and current sources are open-circuited).

Replacing independent sources by their internal resistances,



$$R_N = \frac{12 \times 4}{12 + 4} = \frac{48}{16} = 3\ \Omega$$

Thus, the Norton equivalent resistance across terminals A and B is 3 Ω.

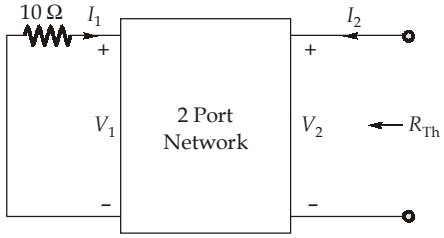
9. (d)

A ratio of voltage or current at one port to the voltage or current at the other port is called a Transfer Function of terminated two-port network.

10. (c)

For maximum power transfer, $R_L = R_{Th}$

Substituting the independent sources with their internal impedances to calculate the Thevenin resistance, we get



$$V_1 = 40I_1 + 60I_2$$
$$V_2 = 80I_1 + 120I_2$$

Here, $V_1 = -10I_1$

$$-10I_1 = 40I_1 + 60I_2$$
$$-5I_1 = 6I_2$$
$$V_2 = \frac{-6}{5} \times 80I_2 + 120I_2 = 24I_2$$
$$R_{Th} = R_L = \frac{V_2}{I_2} = 24\ \Omega$$

Therefore, the load resistance required for maximum power transfer is:

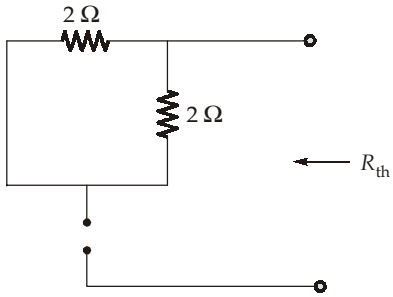
$$R_L = 24\ \Omega$$

11. (d)

At half power frequencies, the power is half of the power at resonance not the current, impedance, or voltage across R. Hence, none of the given statements are true.

12. (d)

For Thevenin's equivalent resistance, R_{th}:



$$\Rightarrow \quad R_{th} = 2 \parallel 2 + \infty = \infty$$

Thus, the Thevenin's equivalent resistance is infinite.

13. (c)

For any value of C, I_1 always leads V_s by 90°, and I_2 will always lags V_s by ϕ.

where, $$\phi = \tan^{-1}\left(\frac{\omega L}{R}\right) = \tan^{-1}\left(\frac{2\times 2}{2}\right),$$
$$= \tan^{-1}(2)$$
$$= 63.43°$$

$\therefore$ I_1 leads I_2 by 90° + 63.43° = 153.43°

14. (b)

Given, $v(t) = 100\sin(\omega t + 20°)$ V

$i(t) = 5\sin(\omega t - 10°)$ A

The impedance, $Z = \dfrac{V}{I} = \dfrac{100\angle 20°}{5\angle -10°} = 20\angle 30°$

$= 20[\cos 30° + j\sin 30°]$

$= 20\left[\dfrac{\sqrt{3}}{2} + j\dfrac{1}{2}\right]$

$Z = 10\sqrt{3} + j10\ \Omega = R + jX\ \Omega$

Hence, $R = 10\sqrt{3},\ X = 10$

Reactive power absorbed by the circuit is

$$P_{\text{reactive}} = \frac{i_{\max}^2 X}{2} = \frac{1}{2}\times 25\times 10 = 125 \text{ VAR}$$

15. (a)

From the given pole-zero plot,

$$Z(s) = \frac{\left(s + \frac{1}{\sqrt{2}}\right)\left(s + \sqrt{2}\right)}{(s+1)}$$

For $s = j\omega$:

$$Z(j\omega) = \frac{\left(j\omega + \frac{1}{\sqrt{2}}\right)\left(j\omega + \sqrt{2}\right)}{(j\omega+1)}$$

Given, $i(t) = 2\cos(t - 45°)$

$\therefore$ $\omega = 1$ rad/sec

$\therefore$ $$Z(j1) = \frac{\left(j + \frac{1}{\sqrt{2}}\right)\left(j + \sqrt{2}\right)}{(1+j)}$$

$$|Z| = \frac{\sqrt{1+2}\times\sqrt{1+\frac{1}{2}}}{\sqrt{2}} = \frac{\sqrt{3}\times\sqrt{\frac{3}{2}}}{\sqrt{2}} = \frac{3}{2}$$

$\therefore$ $|V| = |Z| \times |i(t)|$

$= \dfrac{3}{2}\times 2 = 3$ V

Hence, the magnitude of the voltage phasor is 3 V.

16. (b)

In a series RC circuit, the voltage across the resistor is in phase with the current, while the current leads the supply voltage.

Therefore, the output voltage (across R) leads the input voltage.

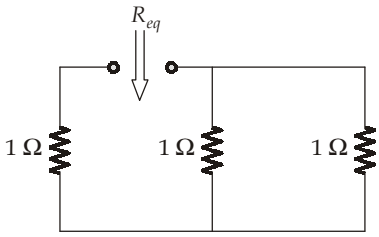
17. (b)

For a connected graph with 'n' nodes the minimum number of branches (a tree) is $(n - 1)$, not 'n'.

18. (b)

The time constant of a network is given by,

$$\tau = \frac{L_{eq}}{R_{eq}}$$



Given: $L_{eq} = 1\ \text{H}$

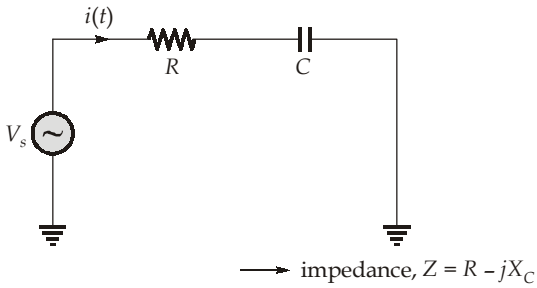
Equivalent resistance: $R_{eq} = 1 + (1 \| 1) = 1 + 0.5 = 1.5\ \Omega$

$\therefore \quad \tau = \frac{1}{1.5} = \frac{2}{3}\ \text{sec}$

Hence, the time constant of the circuit is $\frac{2}{3}\text{sec}$.

19. (c)

Given, series R-C circuit,

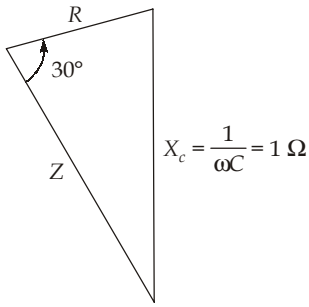


Given, $i(t) = \sqrt{2}\sin(\omega t + 30°)$

but, $i(t) = \frac{V_s}{Z} = \frac{V_s}{\sqrt{R^2 + X_C^2}} \angle \tan^{-1}\left(\frac{X_C}{R}\right)$

on comparing, $\tan^{-1}\left(\frac{X_C}{R}\right) = 30°$

(or) impedance triangle,



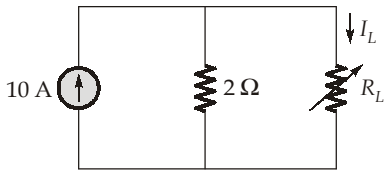
$$\therefore \quad \frac{X_C}{R} = \tan 30°$$

$$R = \frac{X_C}{\tan 30°} = \frac{1}{\left(\frac{1}{\sqrt{3}}\right)}$$

$$\therefore \quad R = \sqrt{3}\ \Omega = 1.732\ \Omega$$

20. (d)

Given,



For maximum power transfer, $R_L = 2\ \Omega$

$$\therefore \quad \text{Power, } P = \frac{V^2}{4R_L} \quad \text{(or)} \quad P = I_L^2 R_L$$

Current through the load,

$$I_L = \frac{10 \times 2}{2+2} = 5\ \text{A}$$

$$\therefore \quad P = (5)^2 \times 2 = 50\ \text{W}$$

Voltage across current generator, $V = I_L \times R_L$

$$= 5 \times 2 = 10\ \text{V}$$

21. (d)

Given, Resistance of coil, $R = 50\ \Omega$

Inductance of coil, $L = 0.5\ \text{H}$

We know that,

$$V = L\frac{di}{dt}$$

$$100 = 0.5\frac{di}{dt}$$

$$\Rightarrow \quad \frac{di}{dt} = 200\ \text{A/s}$$

Hence, the rate of change of current at $t = 0^+$ is 200 A/s.

22. (c)

For a two-port transmission network to be reciprocal,

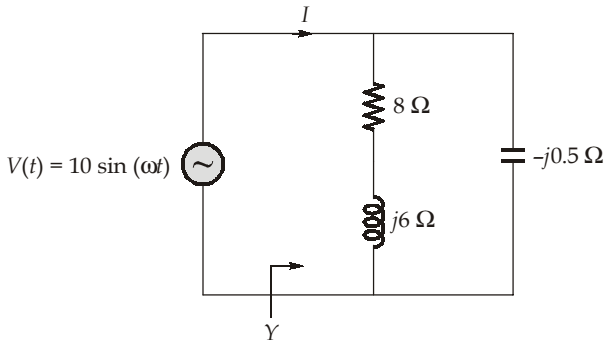
$$\begin{vmatrix} A & B \\ C & D \end{vmatrix} = 1$$

(or)

$$\begin{vmatrix} B & D \\ A & C \end{vmatrix} = -1$$

23. (d)

Given circuit:



$$\therefore \quad Y = \frac{1}{8+j6} + \frac{1}{-j0.5} = \frac{8-j6}{100} + j2$$

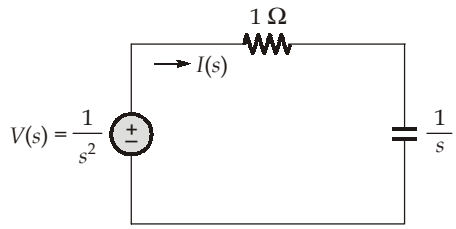
$$= 0.08 - j0.06 + j2 = 0.08 + j1.94 = 1.98 \angle 87.68° \text{ } \mho$$

$$\therefore \quad I = VY = 10\angle 0° \times 1.98 \angle 87.68 = 19.8 \angle 87.68° \text{ A}$$

$\Rightarrow$ Hence, I = 19.8 ∠87.68° A

24. (a)

By transforming the given network into the s-domain



$$\therefore \quad I(s) = \frac{V(s)}{1+\frac{1}{s}} = \frac{1}{s^2\left(1+\frac{1}{s}\right)} = \frac{1}{s(s+1)}$$

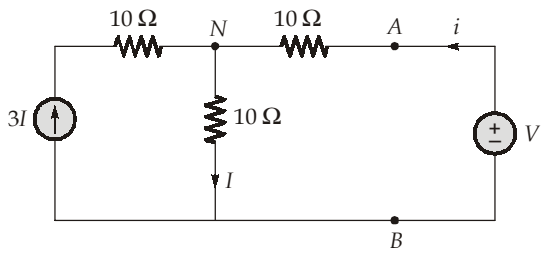
$$\therefore \quad I(s) = \frac{1}{s} - \frac{1}{s+1}$$

$$\therefore \quad i(t) = (1-e^{-t})u(t)$$

at t = 2 sec, $\quad i(2) = 1 - e^{-2} = 0.86$ A

25. (c)

Given circuit:



Using nodal analysis at node N,

$$-3I + I - i = 0$$

$$i = -2I$$

but, $i = \dfrac{V - V_N}{10}$; where, V_N is node voltage at N.

and $$V_N = 10I$$

$$\therefore \quad i = \frac{V - 10I}{10} = \frac{V - 10\left(\dfrac{i}{-2}\right)}{10} = \frac{V + 5i}{10}$$

$$i = \frac{V + 5i}{10}$$

$$V + 5i = 10i$$

$$V = 5i$$

$$\Rightarrow \quad \frac{V}{i} = 5\ \Omega$$

Hence, the Thevenin's resistance seen from terminals A-B is 5 Ω.

26. (b)

For $t = 0^+$, $$v(t)\big|_{t=0^+} = \frac{1}{C}\int_{0^-}^{0^+} i\,dt$$

$v(t)\big|_{t=0^+}$ will be maximum for only unit impulse current because an impulse delivers instantaneous charge to the capacitor.

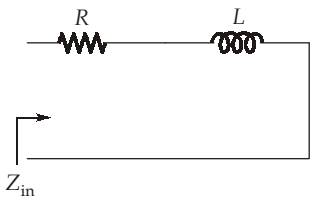
For a unit step or ramp input, the voltage across the capacitor will remains same as at $t = 0^-$ i.e., 0 V.

Hence, the maximum voltage at $t = 0^+$ occurs for a unit impulse function.

27. (d)

Given, $$Z_{in} = 100 + j30\ \Omega$$

The equivalent series circuit is shown below:



$$Z_{in} = R + jX_L = 100 + j30$$

On comparing, $$R = 100\ \Omega$$

$$\therefore \quad X_L = 30$$

$$\Rightarrow \quad \omega L = 30$$

$$\therefore \quad L = \frac{30}{2\pi f} = \frac{30}{100 \times 10^3 \times 2\pi}$$

$$\therefore \quad L = 48\ \mu H$$

28. (b)

For the series circuit,

$$\text{Damping ratio, } \xi = \frac{R}{2}\sqrt{\frac{C}{L}}$$

$$\text{Substituting values, } \xi = \frac{2}{2}\sqrt{\frac{2}{2}} = 1 \quad \Rightarrow \quad \text{Critically damped}$$

For the parallel circuit

$$\text{Substituting values, } \xi = \frac{1}{2R}\sqrt{\frac{L}{C}}$$

$$\xi = \frac{1}{2\times 2}\sqrt{\frac{2}{2}} = \frac{1}{4} < 1 \quad \Rightarrow \quad \text{Underdamped}$$

29. (c)

The total equivalent resistance of the circuit is,

$$R_{eq} = 3 + (2 \| 4 \| 1) = 3 + 0.57 = 3.57\ \Omega$$

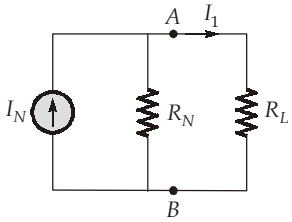
$$\therefore \quad I_1 = \frac{40}{3.57} = 11.2\ \text{A}$$

$$I_3 = I_1 \times \frac{4}{4 + (1 \| 2)} = \frac{4}{4.67} \times 11.2$$

$$\therefore \quad I_3 = 9.6\ \text{A}$$

30. (a)

The Norton's equivalent of the given network is shown below:



For the first case:

$$P_{\text{absorbed}} = 12\ \text{W} = I_1^2 \times R_L$$

$$\Rightarrow \quad 12\ \text{W} = 3 \times I_1^2 \quad \Rightarrow \quad I_1 = 2\ \text{A}$$

$$I_1 = \frac{I_N \cdot R_N}{R_N + R_L} \quad \Rightarrow \quad 2R_N + 6 = I_N R_N \qquad \ldots(\text{i})$$

For the second case:

$$R_L = 8\ \Omega$$

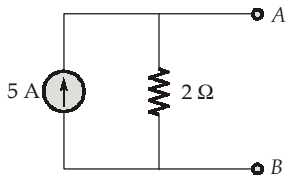
$$P_{\text{absorbed}} = 8\ \text{W}$$

$$\Rightarrow \quad 8 = I_1^2 \times 8 \quad \Rightarrow I_1 = 1\ \text{A}$$

$$I_1 = \frac{I_N R_N}{R_N + R_L} \quad \Rightarrow \quad I_N R_N = (8 + R_N) \qquad \ldots(\text{ii})$$

form (i) and (ii)

$$8 + R_N = 2R_N + 6 \Rightarrow R_N = 2\ \Omega$$
$$2I_N = 10 \Rightarrow I_N = 5\ \text{A}$$



31. (d)

For coil L_1 :

$$L_1 + M_{12} + M_{13} = 1 + 0.5 + 1 = 2.5\ \text{H}$$

For coil L_2 :

$$L_2 + M_{23} + M_{12} = 2 + 1 + 0.5 = 3.5\ \text{H}$$

For coil L_3 :

$$L_3 + M_{13} + M_{23} = 5 + 1 + 1 = 7\ \text{H}$$

Hence, the total inductance is,

$$L_{eq} = L_1 + M_{12} + M_{13} + L_2 + M_{23} + M_{12} + L_3 + M_{13} + M_{23} = 2.5 + 3.5 + 7 = 13\ \text{H}.$$

32. (b)

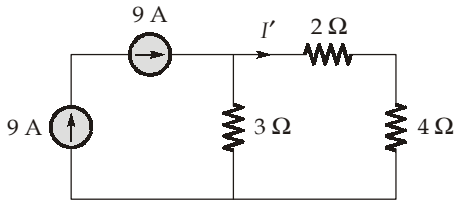
In the given circuit, two independent current sources are connected in series, so they must carry the same current.

i.e. $$I_1 = I_2$$
$$x^2 = 5x - 6$$
$$x^2 - 5x + 6 = 0$$
$\therefore$ $$x = 2, 3$$

For maximum power flow across the 2 Ω resistor, the current flow through it should be maximum.

So, for $x = 3$

$\therefore$ $$I_1 = I_2 = 9\ \text{A}$$



Let I' be the current through the 2 Ω resistor,

$\therefore$ $$I' = \frac{9\times 3}{3+2+4} = 3\ \text{A}$$

Hence, the maximum power absorbed by the 2 Ω resistor is:

$$P_{2\ \Omega} = (I')^2 \times 2 = (3)^2 \times 2 = 18\ \text{W}$$

33. (a)

Quantity	Dual
Mesh	Node
Link	Twig
Tieset	Cutset
Loop current	Node voltage

34. (c)

At resonance, the current circulates around the loop formed by L and C.

35. (c)

For wireless power transfer using electrical resonance circuits, both the transmitter and receiver circuits must resonate at the same frequency.

36. (c)

An ideal constant current source possesses infinite internal resistance, not zero.

38. (a)

A high power factor improves energy efficiency by reducing the amount of reactive power and increasing the utilization of real (active) power.

Section B : Digital Circuits

39. (b)

We have,

$$\sqrt{[22(r-1)]_r} = [1(r-2)]_r$$

Expanding, $\left[(2\times r^2)+(2\times r^1)+\left((r-1)\times r^0\right)\right] = \left[(1\times r^1)+\left((r-2)\times r^0\right)\right]^2$

On squaring both sides we get

$$[22(r-1)]_r = [1(r-2)]_r^2$$

or $[2r^2] + [2r] + (r-1) = (r + r - 2)^2$

$2r^2 + 3r - 1 = (2r - 2)^2$

$(2r^2 + 3r - 1) = (4r^2 + 4 - 8r)$

or $2r^2 + 5 - 11r = 0$

On solving, we get

$r = 5;\ 0.5$

Since $(r-1)$ and $(r-2)$ are digits present in the equation, if implies $r = 0.5$ is not valid.

Thus, $r = 5$

40. (d)

- Y NAND $Y = \overline{YY} = \overline{Y}$
- Y NOR $Y = \overline{Y + Y} = \overline{Y}$
- Y NAND $1 = \overline{Y \cdot 1} = \overline{Y}$
- Y NOR $1 = \overline{Y + 1} = 0$

41. (c)

The bulb is ON when both switches S_1 and S_2 are in the same state, either both ON or both OFF.

S_1	S_2	Bulb
0	0	ON
0	1	OFF
1	0	OFF
1	1	ON

The above truth table represents the Ex-NOR operation.

Hence, Bulb ON condition : $S_1 \odot S_2 = \overline{S_1 \oplus S_2}$

42. (d)

Whenever both b_3 and b_2 are 1, then 0100 is added to the number.

$$b_3\, b_2\, b_1\, b_0 = (1100)_B = (12)_{10}$$

So, for all numbers greater than or equal to 12, 0100 is added.

Therefore, the circuit is a Binary to radix-12 converter.

43. (a)

Data input = 100

CLK	D_i	SI = $D_i \oplus Q_0$	Q_3	Q_2	Q_1	Q_0
0	–	–	0	1	1	0
1	0	0 →	0	0	1	1
2	0	1 →	1	0	0	1
3	1	0 →	0	1	0	0

Thus, the final value stored is 0100.

44. (c)

1. True - SRAM uses cross-coupled inverters (flip-flops), making it bistable and capable of retaining data as long as power is applied. Hence, no refresh is required.
2. True -DRAM stores data using a capacitor per bit and needs periodic refreshing.
3. False - EEPROM is non-volatile (retains data even without power).
4. True - Cache memory is typically implemented using SRAM for higher speed.

So correct statements are 1, 2 and 4.

46. (c)

Zero has two representations in

(a) sign magnitude as 0000 and 1000

(b) 1's complement as 0000 and 1111

However, in 2's complement, zero has only one unique representation 0000.

Hence, option (c) is correct.

47. (d)

The maximum number of different Boolean functions involving 'n' Boolean variables is 2^{2^n}.

So, $2^{2^n} = 65536$

On solving we get, $n = 4$

48. (d)

From the logic circuit, the function f is given by:

$$f = f_1 f_2 + f_3$$

Now, $f_1 f_2 = \Sigma(8, 9, 10) \cdot \Sigma(7, 8, 12, 13, 14, 15)$

The common term between f_1 and f_2 is 8

So, $f_1 f_2 = \Sigma(8)$

Therefore,

$$f = f_1 f_2 + f_3$$
$$f = \Sigma(8) + \Sigma(9)$$
$$f = \Sigma(8, 9)$$

Hence, the correct option is (d).

49. (b)

For the given decoder, when $a = 0$ and $b = 1$, y is the output. Apply this to the given circuits.

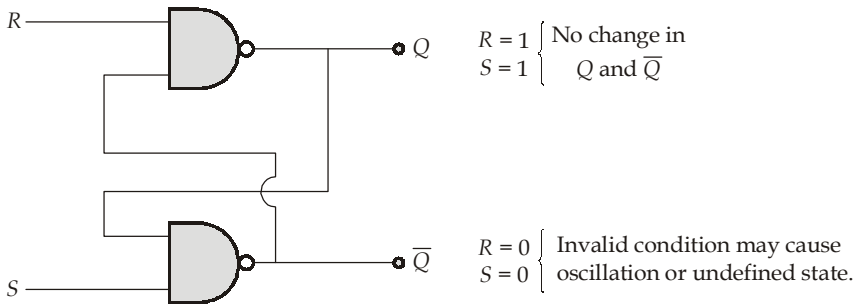
(a) It gives w

(b) It gives z

(c) It gives z

Option (b) is equivalent to given decoder for all possible values.

50. (a)



Thus, when both $R = 0$ and $S = 0$, the circuit may oscillate due to both outputs trying to be low simultaneously.

51. (b)

For J-K flip-flop, $Q_{n+1} = J\overline{Q}_n + \overline{K}Q_n$

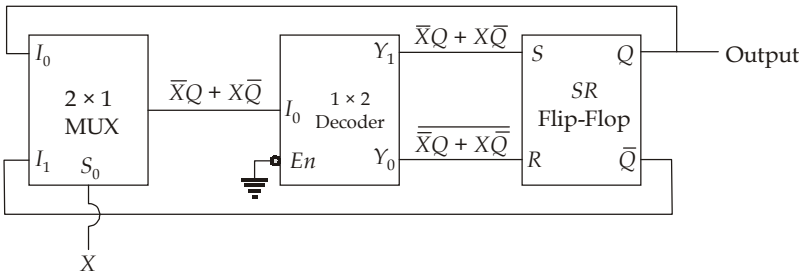
For the given circuit, $Q_{n+1} = (X \oplus Y)\overline{Q}_n + \overline{X}Q_n \quad \because J = X \oplus Y \text{ and } K = X$

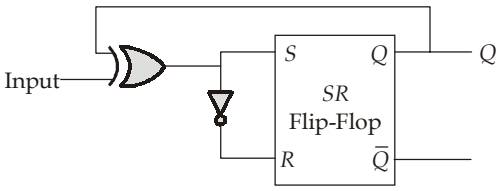
$= \overline{X}Y\overline{Q}_n + \overline{X}Q_n + XY\overline{Q}_n = \overline{X}Q_n + \overline{X}Y + XY\overline{Q}_n$

$= \overline{X}(Y + Q_n) + X\overline{Y}\,\overline{Q}_n$

52. (d)

The MUX in the circuit is working as an EX-OR gate and the 1 × 2 decoder as a NOT gate. Thus the circuit could be redrawn as





Thus, the circuit will function as a T-flip flop

$\because \quad S = X \oplus Q_n$

$R = \overline{X \oplus Q_n}$

For SR-flip flop, $Q_{n+1} = S + \overline{R}Q_n = (Q_n \oplus X) + \overline{\overline{(Q_n \oplus X)}}Q_n = (X \oplus Q_n)(1 + Q_n)$

$Q_{n+1} = X \oplus Q_n$

Excitation equation for T-flip flop.

53. (c)

	2's complement	Decimal value
	1111 1011 (Divider)	5
(a)	1110 0100	28
(b)	1101 0111	41
(c)	1110 0111	25
(d)	1101 1011	37

So, 25 is divisible by 5, we can conclude that $1110\ 0111_2$ is divisible by $1111\ 1011_2$.

54. (c)

The K-map corresponds to the function:

$$f = \overline{a}\,\overline{c} + a\overline{d} + ab\overline{c} + \overline{c}\,d$$

	$\overline{c}\,\overline{d}$	$\overline{c}\,d$	$c\,d$	$c\,\overline{d}$
$\overline{a}\,\overline{b}$	1	1		
$\overline{a}\,b$	1	1		
$a\,b$	1	1		1
$a\,\overline{b}$	1	1		1

It is not equivalent to given K-map.

Hence, option (c) is not equivalent to the given K-map.

55. (d)

$A \odot A = 1$; for $n = 1$

$A \odot A \odot A \odot A \Rightarrow 1 \odot A \odot A = A \odot A = 1;\ n = 3$ | n is odd

$\Downarrow\ \Downarrow\ \Downarrow$

$1\ \ 2\ \ 3$

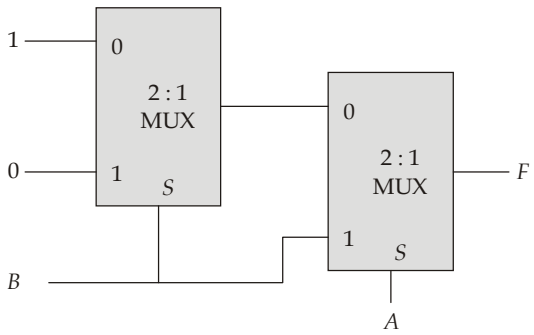
$A \odot A \odot A = 1 \odot A = A;\ n = 2 \Rightarrow n$ is even

$\Downarrow\ \Downarrow$

$1\ \ 2$

Hence, the result remains unchanged when 'n' is even and complements when 'n' is odd.

56. (d)



For the left multiplexer: $P = 1 \cdot \overline{B} + 0 \cdot B = \overline{B}$

For the right multiplexer: $F = P \cdot \overline{A} + B \cdot A = \overline{B}\,\overline{A} + BA = \overline{A \oplus B}$

57. (a)

In an 8-bit counter, the range would be from 0-255. Hence to go from 10101011 (171) to 00101001(41), the counter has to go initially from 171 to 255 and then wrap around from 0 to 41.

Hence to go from 171 to 255, 255 – 171 = 82 clock pulses will be required.

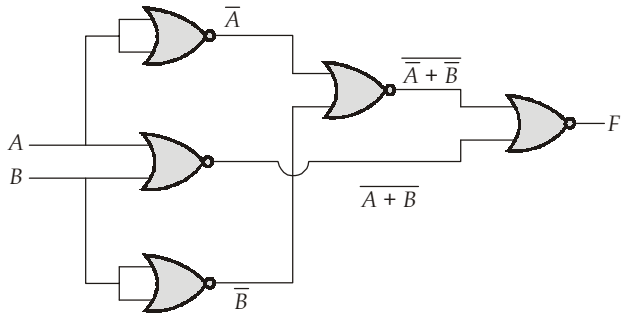
Then from 0 to 41, 41 clock pulses will be required.

Hence, in total 82 + 1 + 41 = 124 clock pulses are required.

59. (c)

1. True - The full-scale input corresponds to the maximum input value mapping to maximum digital output code.
2. True - For an n-bit ADC, the number of quantization levels is 2^n.
3. True – INL measures deviation of actual transfer characteristic from straight-line ideal.

60. (c)



From the circuit, $F = \overline{\overline{\overline{A}+\overline{B}}+\overline{A+B}}$

$F = (\overline{A}+\overline{B})(A+B)$

$F = A \odot B$

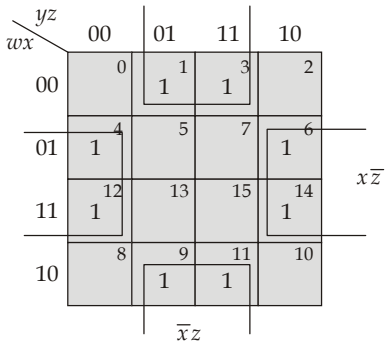
Therefore, Gate 'X' is a NOR Gate.

61. (b)

We have,

$$f(w, x, y, z) = \Sigma(1, 3, 4, 6, 9, 11, 12, 14)$$

From the K-map representation:



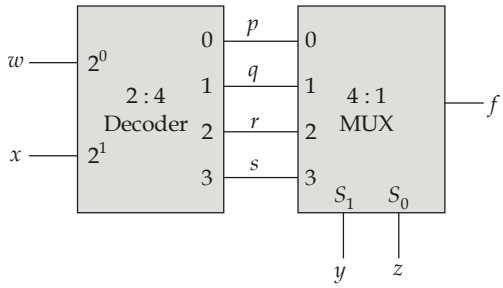
Thus, $f(w, x, y, z) = \Sigma(1, 3, 4, 6, 9, 11, 12, 14)$

$= x\overline{z} + \overline{x}z$

$= x \oplus z$

Therefore $f(w, x, y, z)$ is a two variable function i.e., it is independent of two variables.

63. (d)



Using the decoder: $P = \overline{w}\overline{x};\ q = \overline{w}x;\ r = w\overline{x};\ s = wx$

And using the multiplexer (MUX): $f = \bar{w}\bar{x}\bar{y}\bar{z} + \bar{w}x\bar{y}z + w\bar{x}y\bar{z} + wxyz$

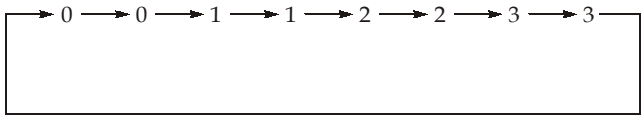
$$f(w, x, y, z) = \Sigma m(0, 5, 10, 15)$$

$$f(w, x, y, z) = \Sigma\pi(1, 2, 3, 4, 6, 7, 8, 9, 11, 12, 13, 14)$$

Therefore, option (d) is correct.

64. (b)

The required switching sequence of the synchronous counter is



1. In the counter switching sequence, the highest decimal number is '3'. To represent state '3', a minimum of 2 flip-flop are required.
2. In the switching sequence each decimal number is repeating twice, to distinguish this repetition 1 more flip-flop is required.

$\therefore$ The minimum number of JK flip-flops required to design the counter = 2 + 1 = 3.

65. (b)

Circuit-1 does not have any feedback. Hence, it cannot be called as a sequential circuit.

66. (d)

1. True – An ideal DAC would have no glitch (real DACs do exhibit glitches due to switching).
2. True – Multiplying DACs accept an analog input and multiply it by a digital word (used in modulators).
3. True – Thermometer-coded DACs exhibit monotonic behavior (single transitions per code step) and reduce major monotonicity errors.
4. True – Segmented DACs use thermometer-coded MSBs and binary-coded LSBs to balance monotonicity and comparator/resistor count.

All statements are correct $\rightarrow$ (d).

67. (b)

1. True – ECL typically has small noise margins compared to CMOS - hence, statement(1) is correct.
2. True – ECL uses a constant current bias and dissipates considerable static power compared to CMOS.
3. True – ECL is used where extremely low propagation delay is required.
4. False – ECL is not easy to integrate at very large scale because of high power consumption and complexity.

So 1, 2, 3 are true.

68. (b)

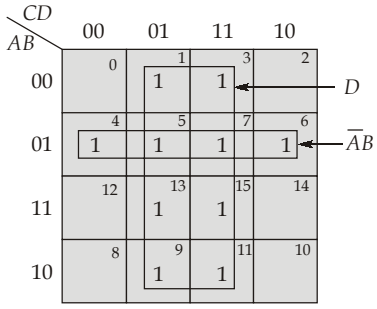
Given $R = 0.002$

$$R = \frac{1}{2^n - 1}$$

$$2^n - 1 = \frac{1}{0.002} \Rightarrow 2^n = 501$$

$$n \cong 9$$

69. (b)



$F = \bar{A}B + D$

70. (a)

1. True - The SAR ADC implements binary search via an internal DAC and comparator.
2. True - Sigma-delta ADCs oversample and use digital filters to enhance resolution.
3. True - Flash ADCs are fastest but require $2^N - 1$ comparators.

71. (c)

Tristate logic gates have three possible output states: the logic '1' state, the logic '0' state and high-impedance state not an indeterminate state.

72. (d)

A latch operates based on level sensitivity (no clock input required), while a flip-flop operates based on edge triggering (requires a clock). Hence, statement (I) is false and statement (II) is true.

74. (d)

As $$(A + BC)' \xleftrightarrow{\text{Dual}} [A \cdot (B + C)]' \neq A'(B' + C')$$

Therefore, statement (I) is incorrect.

75. (a)

In 2's complement arithmetic, overflow is flagged when the carry into the sign bit and the carry out of the sign bit differ. This condition occurs when the result exceeds the valid range for signed number representation.

❍❍❍❍