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# ESE 2025 : Mains Test Series

UPSC ENGINEERING SERVICES EXAMINATION

## Electronics & Telecommunication Engineering

### Test-2 : Digital Circuits + Signals and Systems + Microprocessors & Microcontroller [All topics]

Name : .....

Roll No :

| Test Centres | | | | Student's Signature |
|---|---|---|---|---|
| Delhi ☐ | Bhopal ☐ | Jaipur ☐ | Pune ☐ | |
| Kolkata ☐ | Hyderabad ☑ | | | |

**Instructions for Candidates**

1. Do furnish the appropriate details in the answer sheet (viz. Name & Roll No).
2. There are Eight questions divided in TWO sections.
3. Candidate has to attempt FIVE questions in all in English only.
4. Question no. 1 and 5 are compulsory and out of the remaining THREE are to be attempted choosing at least ONE question from each section.
5. Use only black/blue pen.
6. The space limit for every part of the question is specified in this Question Cum Answer Booklet. Candidate should write the answer in the space provided.
7. Any page or portion of the page left blank in the Question Cum Answer Booklet must be clearly struck off.
8. There are few rough work sheets at the end of this booklet. Strike off these pages after completion of the examination.

**FOR OFFICE USE**

| Question No. | Marks Obtained |
|---|---|
| Section-A | |
| Q.1 | |
| Q.2 | |
| Q.3 | |
| Q.4 | |
| Section-B | |
| Q.5 | |
| Q.6 | |
| Q.7 | |
| Q.8 | |
| Total Marks Obtained | 180 |

Signature of Evaluator ..... Cross Checked by .....

# IMPORTANT INSTRUCTIONS

**CANDIDATES SHOULD READ THE UNDERMENTIONED INSTRUCTIONS CAREFULLY. VIOLATION OF ANY OF THE INSTRUCTIONS MAY LEAD TO PENALTY.**

## DONT'S

1. Do not write your name or registration number anywhere inside this Question-cum-Answer Booklet (QCAB).
2. Do not write anything other than the actual answers to the questions anywhere inside your QCAB.
3. Do not tear off any leaves from your QCAB, if you find any page missing do not fail to notify the supervisor/invigilator.
4. Do not leave behind your QCAB on your table unattended, it should be handed over to the invigilator after conclusion of the exam.

## DO'S

1. Read the Instructions on the cover page and strictly follow them.
2. Write your registration number and other particulars, in the space provided on the cover of QCAB.
3. Write legibly and neatly.
4. For rough notes or calculation, the last two blank pages of this booklet should be used. The rough notes should be crossed through afterwards.
5. If you wish to cancel any work, draw your pen through it or write "Cancelled" across it, otherwise it may be evaluated.
6. Handover your QCAB personally to the invigilator before leaving the examination hall.

**Section A : Digital Circuits + Signals and Systems + Microprocessors & Microcontroller**

**Q.1 (a)** Design a 3-bit binary counter using T-flip-flops. **[12 marks]**

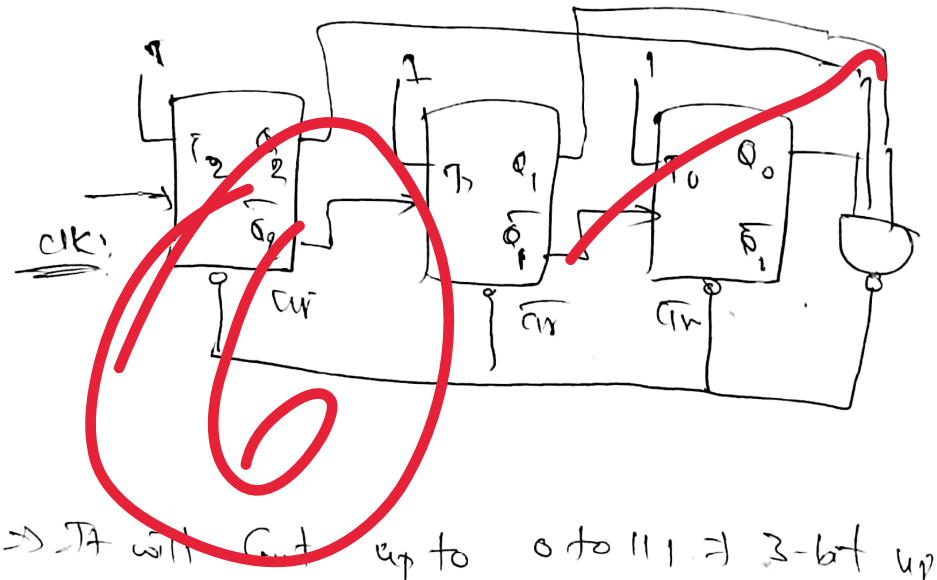
Sol.

Given: no of bits = 3 :

We Req = 3-flip flop for implementation

Flip-flop: T-flip-flop

Design, Up-Counter (000 to 111)




⇒ It will Count up to 0 to 111 ⇒ 3-bit up Counter

Truth table must for full marks

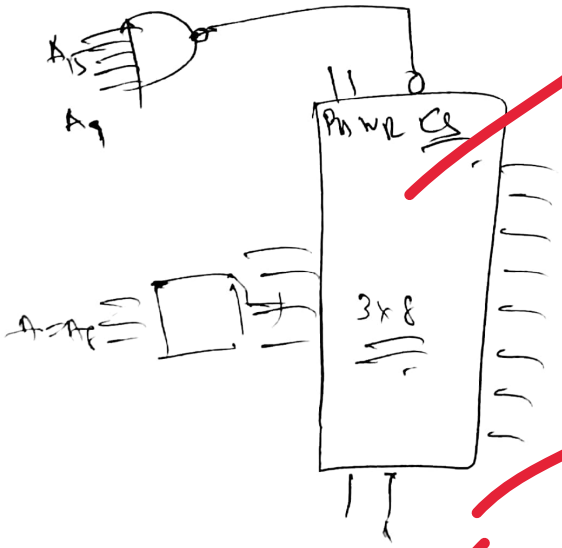
**Q.1 (b)** **(i)** Draw the circuit for interfacing 512 bytes of memory to 8085 microprocessor using 3 × 8 decoder.

**(ii)** Write an assembly language program to move a block of Data of 16 bytes starting from address 2050H to another location starting from 2070H in 8085 microprocessor.

**[7 + 5 marks]**

Ans)

Given 512 bytes. $= 2^9 \Rightarrow$ 0 to 8 :: A




S.A ⇒ 0000 = 0000H

EA ⇒ 01FF 01FFH.

S.A = 0000H

EA = 01FFH

Q.1 (c) (i) Draw the signal flow graph (Butterfly structure) for the computation of 8-point IDFT using inverse Radix-2 DIF-FFT.

(ii) State and prove Initial-value theorem of z-transform.

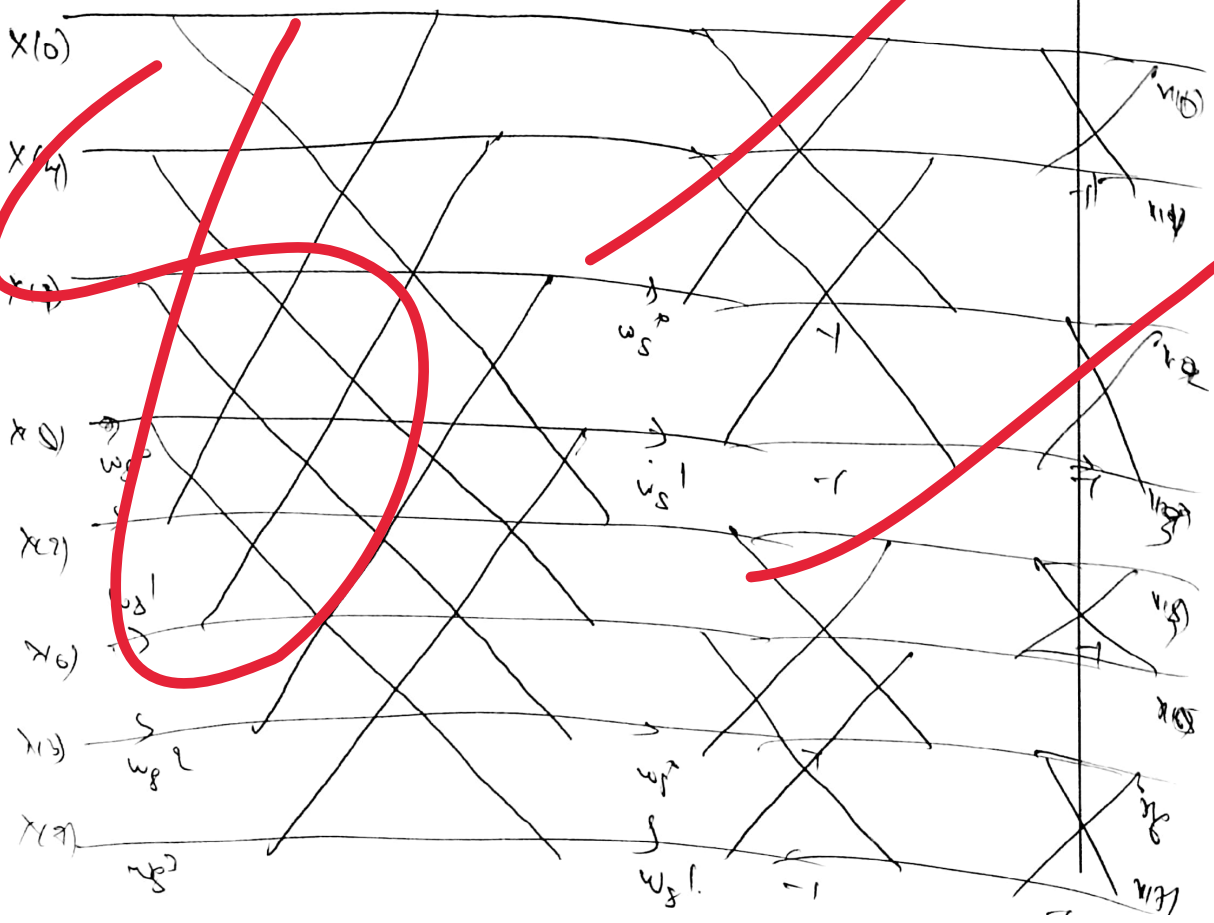
**[8 + 4 marks]**

(ii) (ii) Z-Transform

Initial value theorem: $\lim_{n \to 0} x(n) = \lim_{z \to \infty} (1 - z^{-1}) X(z)$

Initial value of discrete signal can be calculated by finding final value by put $z = 1$ : $(1 - z^{-1})$ multiplying :

(i)



8-point Inverse DFT.

$W_8^0 = 1$ ;

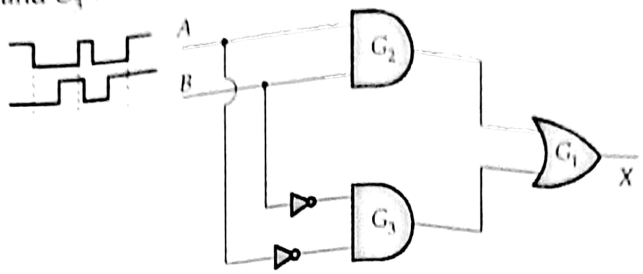
$W_8^1 = -j$

$W_8^2 = \frac{1}{\sqrt{2}} + j\frac{1}{\sqrt{2}}$

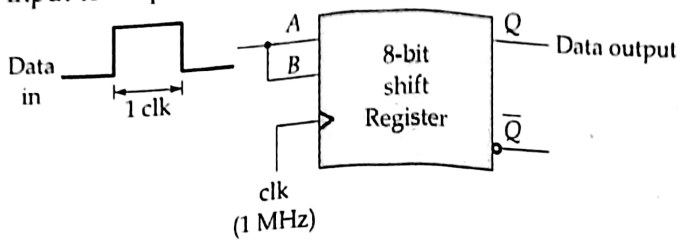
$W_8^3 = \frac{1}{\sqrt{2}} - j\frac{1}{\sqrt{2}}$ ,

$W_N^{kn} = e^{-j\frac{2\pi}{N}kn}$

**Q.1 (d)** (i) Draw the timing diagram for the logic circuit in the figure shown with outputs of $G_1$, $G_2$ and $G_3$ with input waveform $A$ and $B$ as indicated.




(ii) Consider the serial in-serial out shift register which is used to provide time delay from input to output.

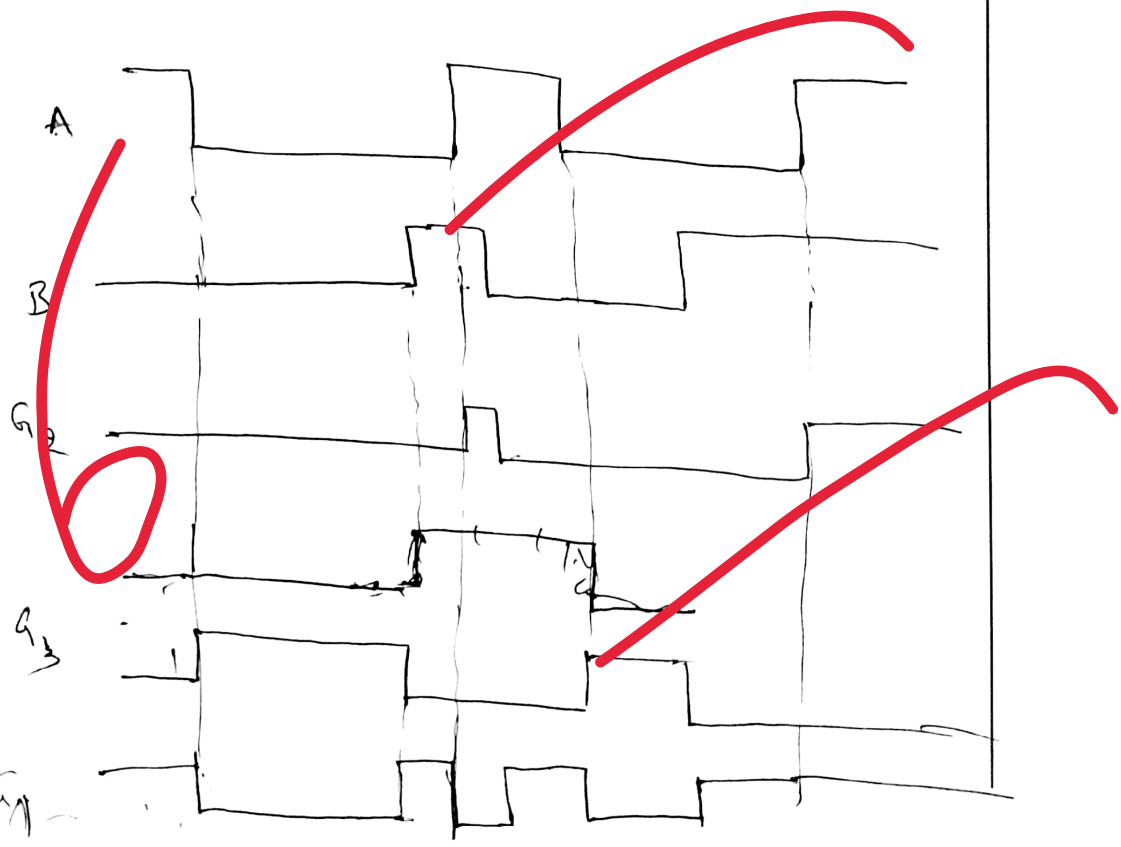



Draw and calculate the output and delay provided by the above shift register in clear steps.

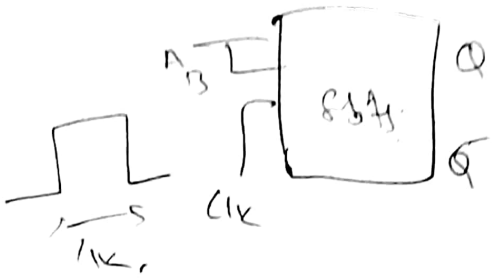
**[6 + 6 marks]**

Sol: Given $G_2 = AB$, $G_3 = \overline{A}\overline{B}$, $G_1 = G_2 + G_3$

$G_3 = \overline{A+B}$ $G_1 = \overline{A}\overline{B} = A \odot B$



(11)

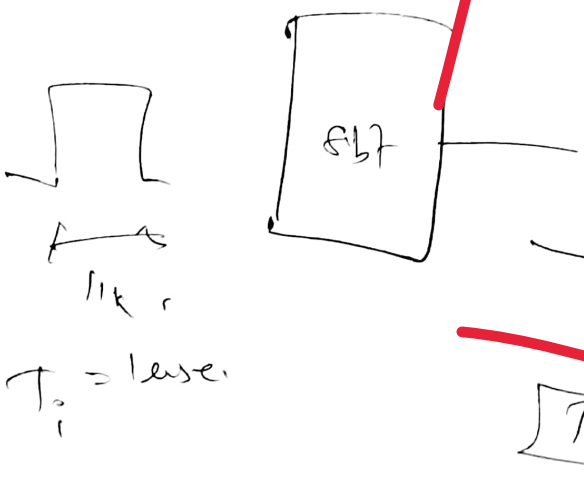



→ Given: SISO → serial input serial o/p:

Time → (9+1) $T_{Clk}$:

Time = 15 $T_{Clk}$ = 15 × 1μsec = 15 μsec

delay.




$T_0$ = 1μsec.

$T_0$ = 15μsec

Q.1 (e) Consider the signal $y(t) = e^{-2t}u(t)$ is the output of a causal all-pass system for which the system function is

$$H(s) = \frac{s-1}{s+1}$$

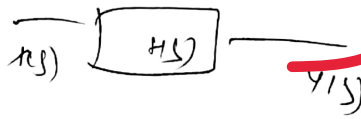
(i) Find and sketch at least two possible inputs $x(t)$ that could produce $y(t)$.

(ii) From the solutions obtained in part (i), what is the input $x(t)$ if it known that a stable system exists that will have $x(t)$ as an output and $y(t)$ as the input? Find the impulse response $h(t)$ for this system.

**[6 + 6 marks]**

Sol,

$y(t) = e^{-2t}u(t)$ ; $H(s) = \frac{s-1}{s+1}$




$Y(s) = H(s)X(s)$

$\frac{1}{(s+2)} = \frac{s-1}{s+1} \cdot X(s)$

$X(s) = \frac{s+1}{(s-1)(s+2)}$

$X(s) = \frac{A}{s-1} + \frac{B}{s+2}$

$= \frac{2}{3} \cdot \frac{1}{s-1} + \frac{1}{3} \cdot \frac{1}{s+2}$

$x(t) = \frac{2}{3}e^{t} + \frac{1}{3}e^{-2t}$

two input that produce y(t)

$x(t) = \frac{2}{3}e^{t} + \frac{1}{3}e^{2t}$

(ii) from part $x(t) = \frac{2}{3}e^{t} + \frac{1}{3}e^{2t}$

if input $x_1(t) = \frac{1}{3}e^{2t}$ then o/p output will produce stable o/p for the input.

if $x_1(t) = \frac{1}{3}e^{2t}$ will get BIBO

on other hand $\frac{2}{3}e^{t}$ pole $s = 1$ right side it will become unstable.

$H(s) = ?$ $\quad y(t) = e^{2t} \rightarrow x(t) = \frac{1}{3}e^{2t}$

$Y(s) = H(s)\,X(s)$

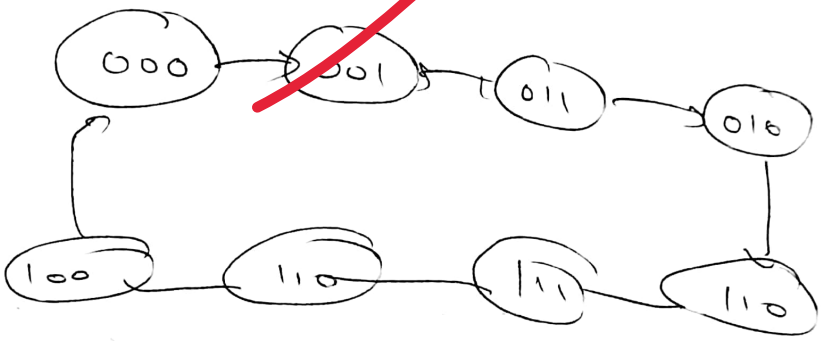
$\frac{1}{s-2} = \frac{1}{3}\cdot\frac{1}{s-2}\cdot H(s)$

$H(s) = 3$ : $h(t) = 3u(t)$

**Q.2 (a)** Implement the state diagram and sequential circuit diagram using JK flip-flops for 3-bit Gray code counter. **[20 marks]**

Sol: Gray Code Counter : n = 3-bits

State diagram: 0, 1, 3, 2, 6, 7, 5, 4




Truth Table

| $Q_2$ $Q_1$ $Q_0$ | $Q_2^+$ $Q_1^+$ $Q_0^+$ | $J_2$ $K_2$ $J_1$ $K_1$ $J_0$ $K_0$ |
|---|---|---|
| 0 0 0 | 0 0 1 | 0 x 0 x 1 x |
| 0 0 1 | 0 1 1 | 0 x 1 x x 0 |
| 0 1 0 | 1 1 0 | 1 x x 0 0 x |
| 0 1 1 | 0 1 0 | 0 x x 0 x 1 |
| 1 0 0 | 0 0 0 | x 1 0 x 0 x |
| 1 0 1 | 1 0 0 | x 0 0 x x 1 |
| 1 1 0 | 1 1 1 | x x x 0 1 x |
| 1 1 1 | 1 1 0 | x 0 x 0 x 0 |

Excitation Table for T & D flip

| $Q_1$ | $Q_0$ | $Q_1^+$ | $Q_0^+$ |
|---|---|---|---|
| 0 | 0 | 0 | x |
| 0 | 1 | 1 | x |
| 1 | 0 | x | 1 |
| 1 | 1 | x | 0 |

$J_2$ : $\rightarrow T_2 = \bar{Q}_1 Q_0$

$K_2$ : $= 1$ $\quad K_2 = \bar{Q}_1 \bar{Q}_0$

$J_1$ : $= J_1 = \bar{Q}_0 Q_2$

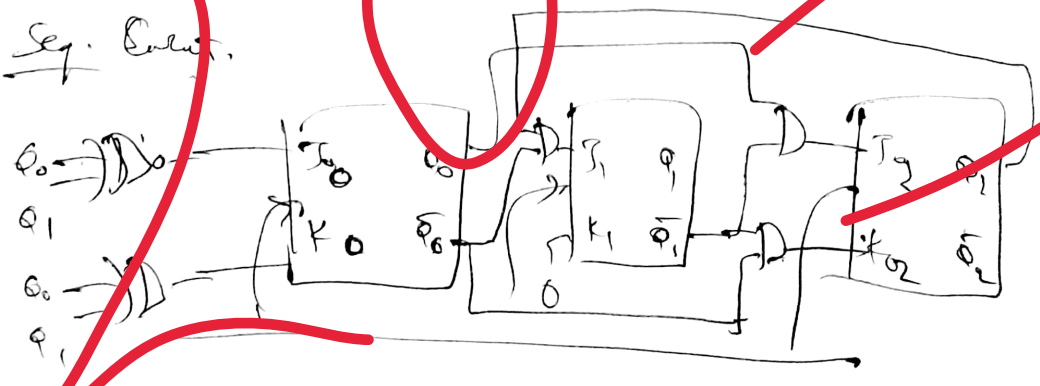
$K_1$ : $= 0$

$K_0 = \bar{Q}_0 Q_2 + Q_1 \bar{Q}_0$

$= 0 \oplus Q_0$

$J_0$ : $J_0 = \bar{Q}_0 \bar{Q}_1 + Q_0 Q_1 = Q_0 \odot Q_1$

Seq. Ckt.



Q.2 (b) (i) Determine and sketch $y(t)$, the convolution of the two signals given below:

$$x(t) = \begin{cases} 2, & -1 \le t \le 1 \\ 1, & 1 < t \le 3 \\ 0, & \text{elsewhere} \end{cases}$$

and $h(t) = 2\delta(t+1) + \delta(t+2)$

(ii) The output $y(t)$ of a causal LTI system is related to the input $x(t)$ by the equation

$$\frac{dy(t)}{dt} + 10y(t) = \int_{-\infty}^{\infty} x(\tau)z(t-\tau)d\tau - x(t)$$

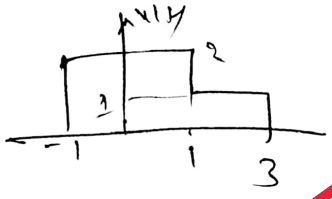
where, $z(t) = e^{-t}u(t) + \delta(t)$

Determine the impulse response of the system.

**[10 + 10 marks]**

Sol

$$x(t) = 2[u(t+1) - u(t-1)] + u(t-1) - u(t-3)$$




$$h(t) = 2\delta(t+1) + \delta(t+2)$$

$$y(t) = [x(t) * h(t)]$$

$$y(t) = [2u(t+1) - 2u(t-1) + u(t-1) - u(t-3)] * [2\delta(t+1) + \delta(t+2)]$$

Property: $\{x(t) * \delta(t-t_0)\} = x(t-t_0)$

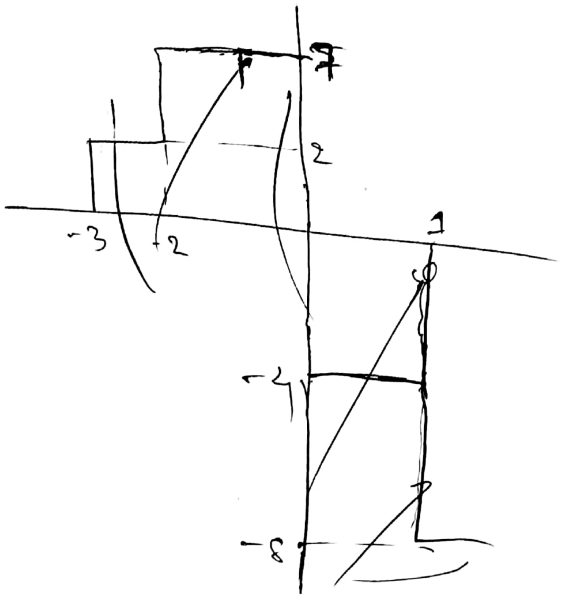
$$y(t) = 2u(t+1+1) - 2u(t-1+1) + 2u(t+1-1) - 2u(t-3)$$

$$+ 2u(t+1+2) - 2u(t-1+2) + u(t+2-1) - u(t-3+2)$$

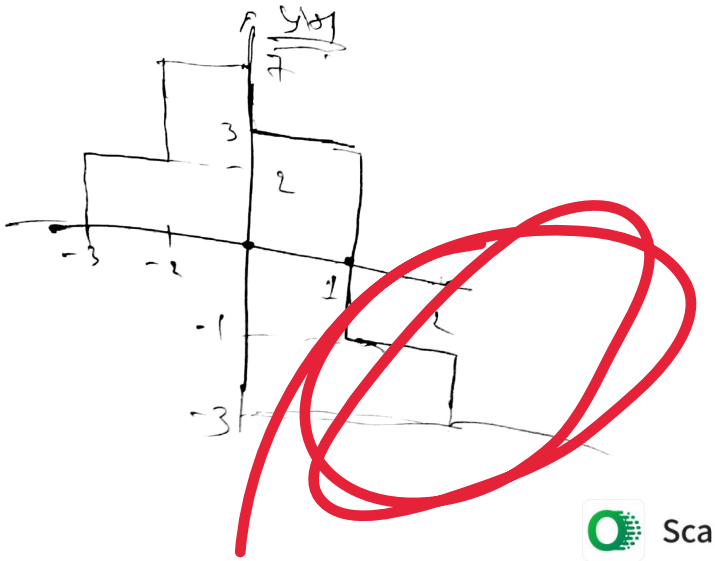
$y(n) = 5u(n+2) - 4u(n+1) + 2u(n+3) - 2u(n-3)$

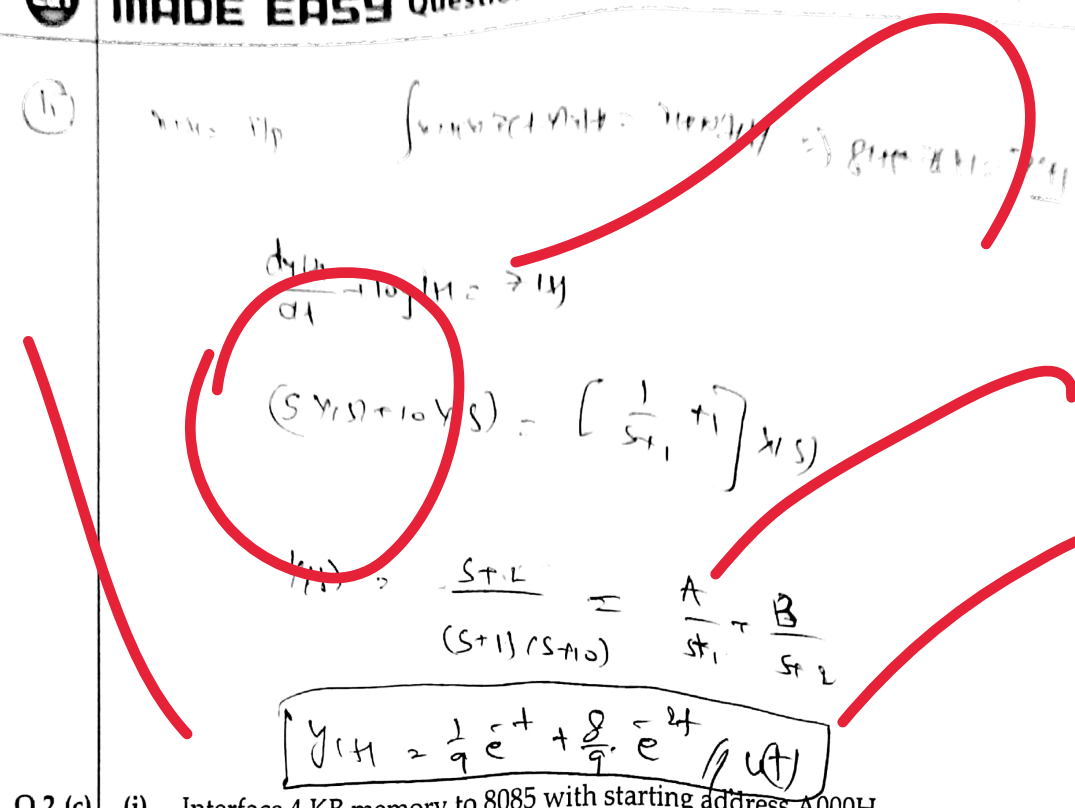
$+ 4u(n-1)$

$y(n) = 2u(n+3) + 5u(n+2) - 4u(n+1) - 4u(n-1) - 2u(n-3)$




$y(-n)$





**Q.2 (c)** **(i)** Interface 4 KB memory to 8085 with starting address A000H. Design address decoding circuit using (i) 3 × 8 decoder and (ii) using only NAND gates.

**(ii)** Write an algorithm and assembly language program, to perform the multiplication of two 8 bit numbers using 8085.

**[10 + 10 marks]**

Sol: (i)

Starting address = A000H

memory = 4KB = $2^{12}$ B

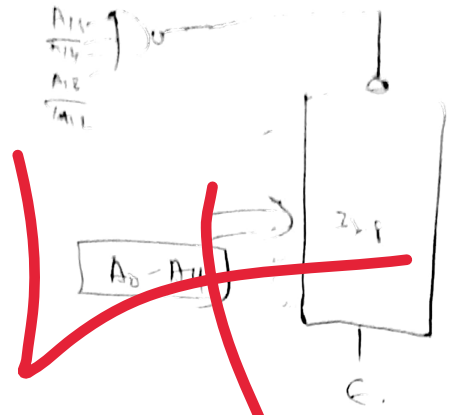
$A_{15} - A_{12} = 1$ (A000 - FFFF)

$\Rightarrow$ $A_{15} - A_{12} - A_{11} - A_{10} - A_9 - A_8 - A_7 - A_6 - A_5 - A_4 - A_3 - A_2 - A_1 - A_0$

1 0 1 0 0 0 0 0 0 0 0 0 $\Rightarrow$ A000

1 0 1 1 1 1 1 1 1 1 1 1 $\Rightarrow$ AFFF

Decoding Circuit = $A_{15}\overline{A_{14}}A_{13}\overline{A_{12}}$



∴ A = A000

[A → A FFF

∴ Designed 8K8 and NAND of 4kB Pgm.

(17) Given: multiplication of two 8 bits numbers.

Let say take: ~~[illegible]~~, ~~[illegible]~~ ⇒ 15H, 25H.

Program:

~~MOV B,#15~~

MOV B, #15H

MOV A, #25H;

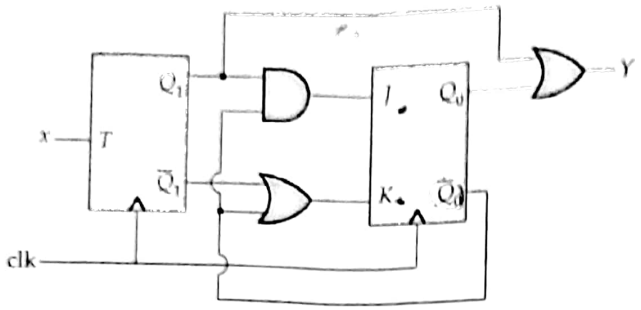
MUL A;

STA 1000H;

HLT;


op ⇒ 15
25
⇒ 375

Q.3 (a) (i) Draw the state diagram of the sequential circuit shown in figure below:

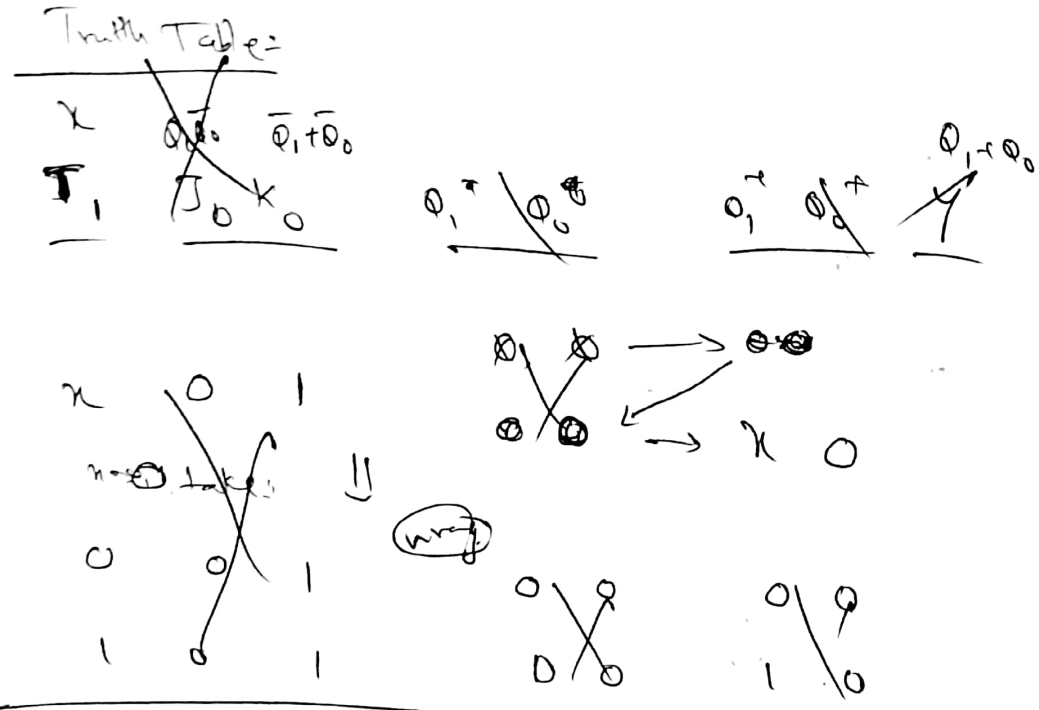



(ii) Find the z-transform of the given signal $x[n]$ using scaling in the z-domain property.

$x[n] = a^n \sin(\omega_0 n)\, u[n]$.

**[10 + 10 marks]**

Truth Table :-



Sol:

$J_0 = Q_1 \bar{Q}_0$ ; $T_1 = x$ = input

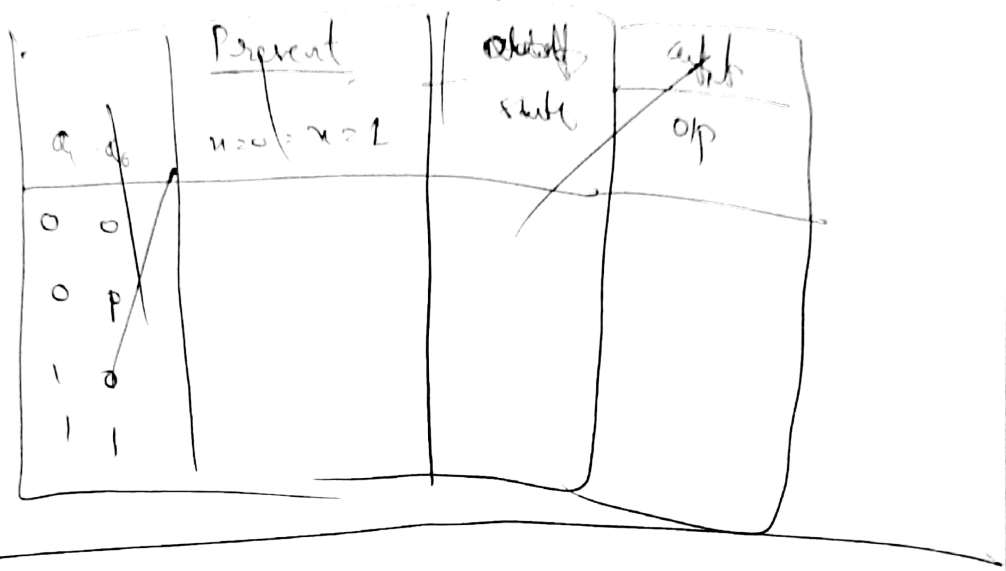
$K_0 = \bar{Q}_1 + \bar{Q}_0$ ; $y = Q_1 + Q_0$

input = x ;

output = y ;

Initial State, $Q_1, Q_0$

next state, $Q_1^+ Q_0^+$




(11)

$$x(n) = a^n \sin(\omega_0 n) u(n)$$

$$\Downarrow$$

applying Z-Transform

$$x(z) = \sin(\omega_0 n) u(n)$$

$$\Downarrow$$

$$X(z) = \frac{z^2 - z\sin\omega}{z^2 - 2z\cos\omega + 1}$$

$$\Downarrow$$

$a^n x(n) \Rightarrow X\left(\frac{z}{a}\right)$ - property: multiplication

$$X(z) = \frac{\left(\frac{z}{a}\right)^2 - \left(\frac{z}{a}\right)\sin\omega}{\left(\frac{z}{a}\right)^2 - 2\left(\frac{z}{a}\right)\cos\omega + 1}$$

$$X(z) = \frac{\frac{z^2}{a^2} - \frac{z\sin\omega a}{a}}{\frac{z^2}{a^2} - \frac{2z\sin\omega}{a} + 1}$$

$$X(z) = \frac{z^2 - az\sin\omega}{z^2 - 2az\sin\omega + a^2}$$

8

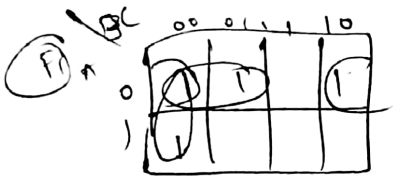
Q.3 (b) (i) Implement the following Boolean function using 3 × 4 × 2 PLA, also write the PLA programming table.

$F_1(A, B, C) = \Sigma m(0, 1, 2, 4)$

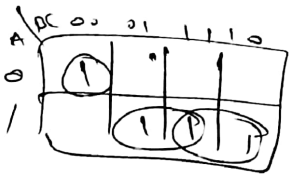
$F_2(A, B, C) = \Sigma m(0, 5, 6, 7)$

(ii) A 6-bit dual slope ADC uses a reference of 12 V and a fixed count of 010110. Convert the maximum input voltage accurately in digital form.

**[15 + 5 marks]**

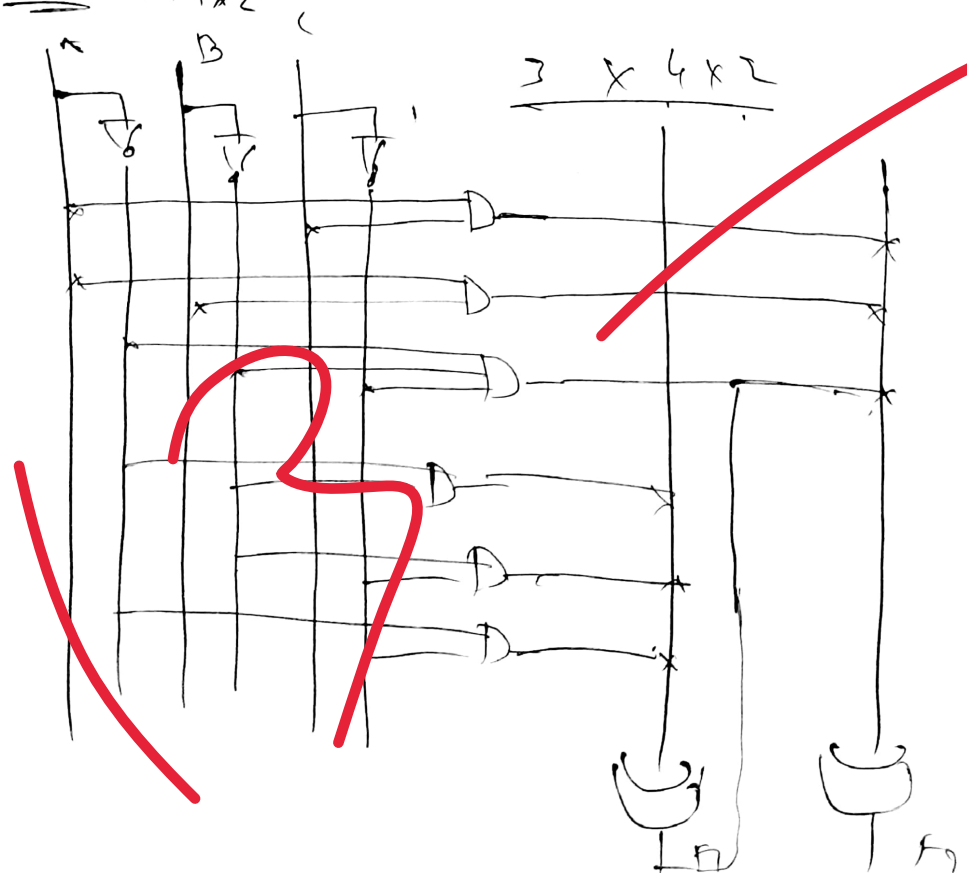


$F_1(A,B,C) = \bar{A}\bar{C} + B\bar{C} + \bar{A}B$



$F_2(A,B,C) = AC + AB + \bar{A}B\bar{C}$

PLA: 3×4×2



(ii) $V_R = 12V$; $n = 6$ bits;

Given $\Rightarrow (010110)_2$

$$V_0 = \frac{V_{ref}}{2^n - 1} \times (\text{Digital})$$

$$V_0 = \frac{12}{2^6 - 1} \times (010110)_2$$

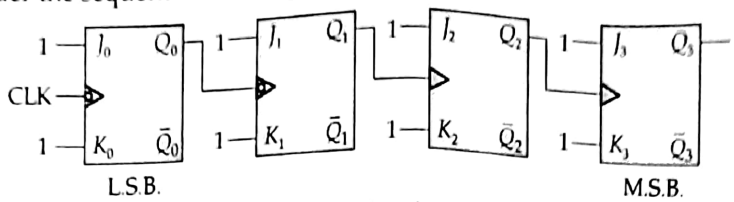
$(010110) = 2^1 \times 1 + 2^2 \times 1 + 2^4 \times 1 = 8 + 4 + 2 = 14$

$$V_0 = \frac{12}{63} \times 14$$

$V_0 = 2.66$ volts

$V_0 \approx 2$ accurately

Q.3 (c) Consider the sequential circuit given below:



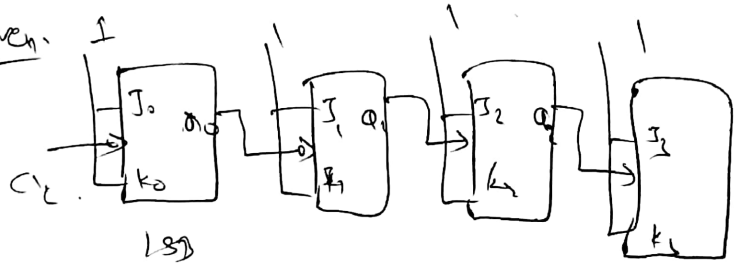

(i) Find the count sequence of the circuit given above. Assume initial condition of flip-flop to be zero.

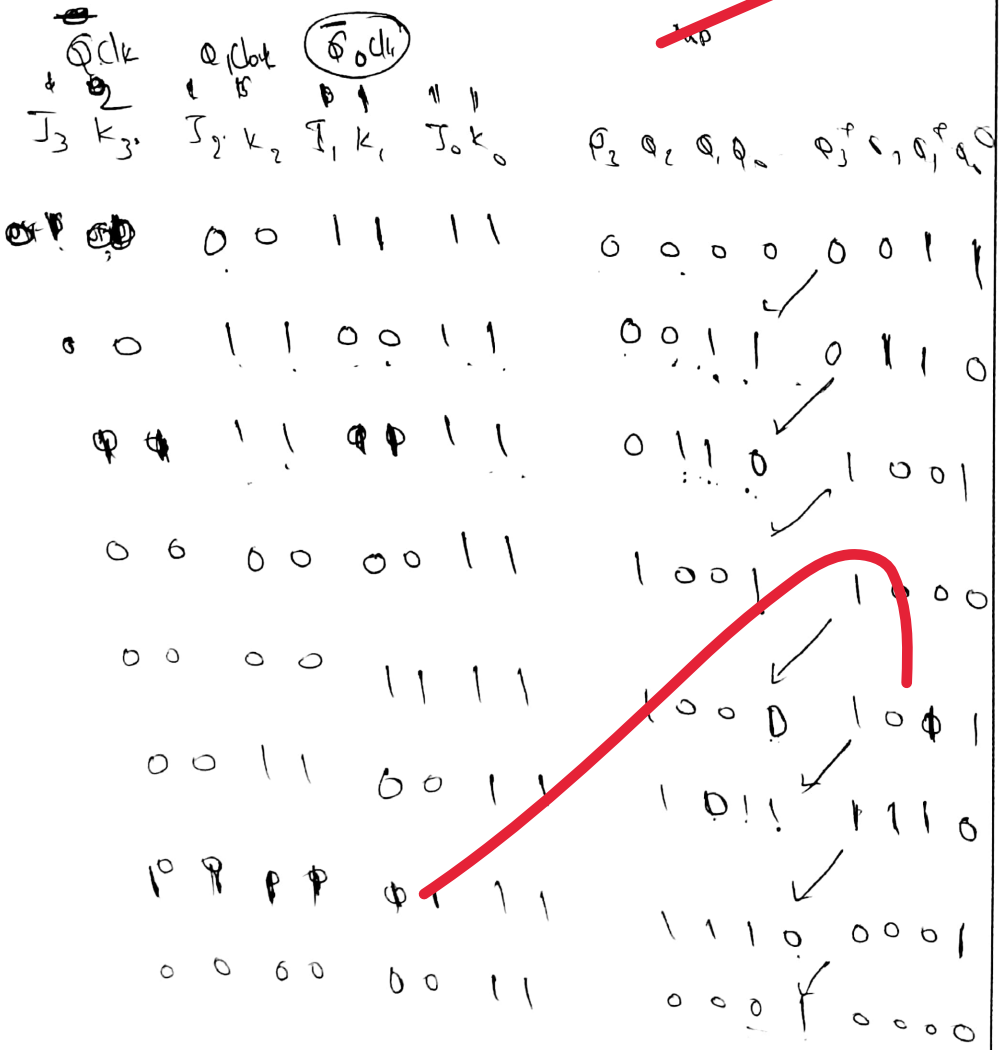
(ii) If clock frequency is 160 kHz. Find the frequencies of $Q_0$ and $Q_2$.

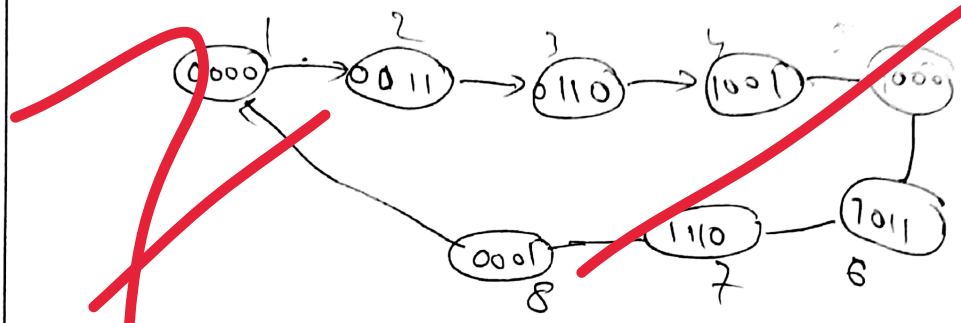
(iii) Sketch the waveforms of clock, $Q_0$, $Q_1$, $Q_2$ and $Q_3$.

**[8 + 4 + 8 marks]**

Sol: Given.





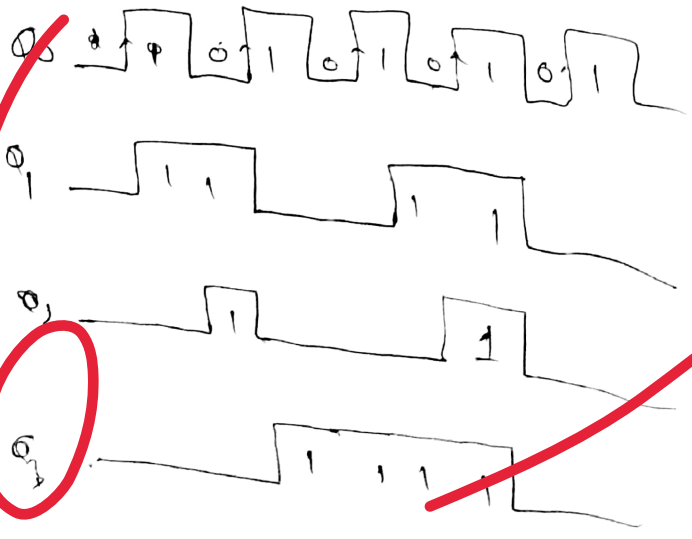

(ii) $f_{input} = 160\ KHz$;

$f_{Q_0}, f_{Q_2} = ?$

$f_{Q_2} = \frac{f}{2} = \frac{160}{2} = 80\ KHz$;

$f_{Q_0} = \frac{f}{8} = \frac{160}{8} = 20\ KHz$;

(iii)




Wave form

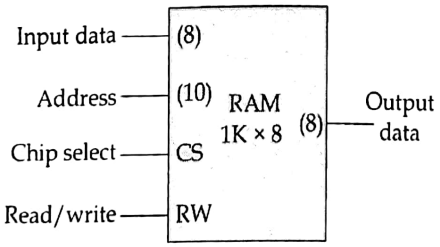
Q.4 (a) (i) Explain how linear convolution is performed using DFT. Find the linear convolution of $x[n] = \{1, 1, 1\}$ and $h[n] = \{1, 1\}$ using DFT.

(ii) Derive the relationship between discrete Fourier series coefficients ($C_k$) and discrete Fourier Transform $X(k)$ of a signal $x[n]$.

**[15 + 5 marks]**

**Q.4 (b)** **(i)** Implement the logic function $F(A, B, C, D) = \Sigma m(0, 1, 2, 3, 4, 7, 9, 10)$ using 4 : 1 MUX only. (Assume only inputs are available)

**(ii)** Construct a 4 K × 8 RAM with 1 K × 8 RAM chips. The 1 K × 8 RAM is as shown below:




**[10 + 10 marks]**

Q.4 (c) (i) Write an 8051 assembly language program for converting the packed BCD number stored at the location 9000H into its equivalent binary number and store the result at 9001H.

(ii) Write an 8086 assembly language program to find the sum $\sum_{i=1}^{10} i$ and store the result in accumulator.

**[12 + 8 marks]**

## Section B : Digital Circuits + Signals and Systems + Microprocessors & Microcontroller

**Q.5 (a)** **(i)** Find the Laplace transform of the function

$f(t) = 2e^{-t}\cos 10t - t^4 + 6e^{-(t-10)}$ for $t > 0$

**(ii)** Find the Fourier transform for the following signal:

$$x(t) = \frac{\sin(2\pi t)}{\pi(t-1)}$$

**[8 + 4 marks]**

Sol (i) $f(t) = 2e^{-t}\cos 10t - t^4 + 6e^{-(t-10)}$ $t > 0$

$f(t) = 2e^{-t}\cos 10t$

$\Downarrow$ L.T

$F(s) = L\{2e^{-t}\cos 10t\}$

$F(s) = 2 \cdot \left.\frac{s}{s^2 - 10^2}\right|_{s \to s+1} = \frac{2(s+1)}{(s+1)^2 - 100}$ ①

$f_2(t) = t^4$

$f_1(s) = \frac{4!}{s^5}$ ; $\mathcal{L}\{t^n\} = \frac{n!}{s^{n+1}}$

$f_2(s) = \frac{24}{s^5}$ — (2)

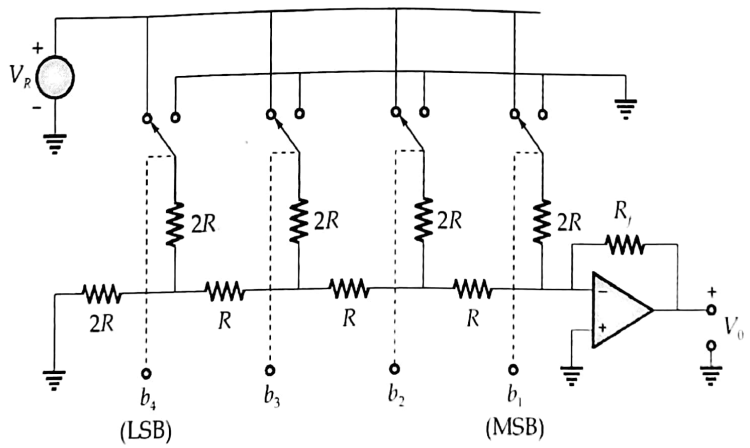
$f_3(t) = 6e^{-(t-10)} = 6e^{-t+10}$

$F_3(s) = 6\frac{e^{+10s}}{s+1}$ $\quad \mathcal{L}\{x(t-t_0)\} = X(s)e^{-st_0}$

$F_3(s) = \frac{6e^{10s}}{s+1}$ — (3)

$F(s) = \frac{2(s+1)}{(s+1)-100} - \frac{24}{s^5} + \frac{6e^{10s}}{s+1}$

Q.5 (b) Consider the $R$-$2R$, 4-bit converter shown below,




Assume the feedback resistance $R_f$ of the op-amp is variable, the resistance $R$ = 5 kΩ and $V_R$ = 10 V. Determine the value of $R_f$ that should be connected to achieve the following output conditions:

**(i)** The value of 1 LSB at the output is 1 V.

**(ii)** An analog output of 8 V for a binary input of 1000.

**(iii)** The actual maximum output voltage of 10 V.

**[12 marks]**

$R = 5\,k\Omega$; $R_f = ?$

$V_R = 10\,V$

Given: R-2R ladder

The o/p voltage of given system.

$$V_o = \frac{V_r}{2^n - 1} \cdot \frac{R_f}{R} \quad \text{(Decimal Eq. binary)}$$

(i) 1 LSB = 1V

(ii) $V_o = 8$, Decimal Eq = (1000) = 8

(iii) $V_o = 10\,V$ — max.

(i) $V_R = 10$, $R_f = \frac{V_r}{2^n - 1}$ ; n = 4 bits

$$1 = \frac{10}{2^4 - 1}$$

(i) $8 = \frac{10}{2^4 - 1} \cdot \frac{R_f}{5}$ (k)

$$R_f = \frac{5(2^n - 1)}{10} = 7.5\ k\Omega$$

Do not write in this margin

**Q.5 (c)** Compute and plot the convolution $y[n] = x[n] * h[n]$ using time domain approach where $x[n] = \left(\frac{1}{2}\right)^{(-n-1)} u[-n-1]$ and $h[n] = u[n-1]$.

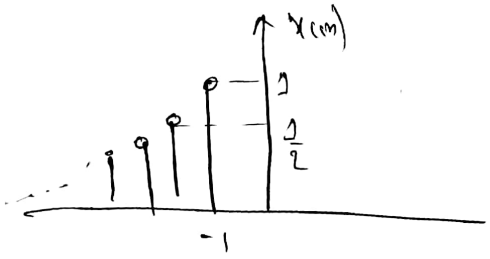
**[12 marks]**

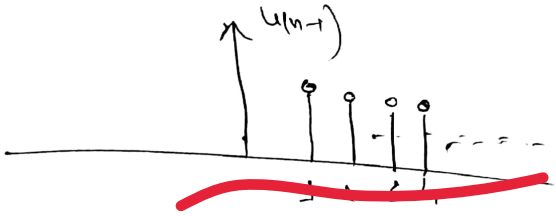
Sol:

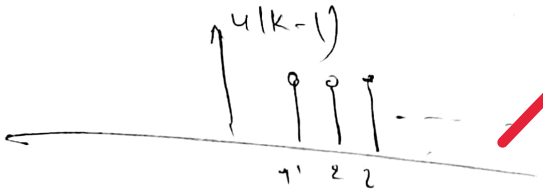
Given: $y(n) = x(n) * h(n)$

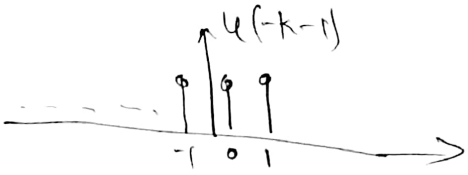
$x(n) = \left(\frac{1}{2}\right)^{-(n+1)} u(-n-1)$ ; $h(n) = u(n-1)$

$y(n) = \sum x(k)\, h(n-k)$ → Convolution



$$y[n] = \sum_{k=0}^{\infty} x[k]\, h(-k+n-1)$$

① $-k-1 > -1$

$k > 0$

② $-k-1 > n$

$-k > n+1$

$k < -n-1$

$-k+n-1 = -1$

$k+n = 0$

$k = -n$

$$y[n] = \begin{cases} x[k]\,h[k], & k < -1 \\ x[k]\,h[k], & k > -1 \end{cases}$$

$$x[n] = \left(\frac{1}{2}\right)^{-n-1} u(-n-1)$$

$$\Rightarrow \begin{cases} \frac{a}{1+a^2} & -\infty \text{ to } -1 \\ \end{cases}$$

$$= \frac{\frac{1}{2}}{1-\frac{1}{4}} = \frac{\frac{1}{2}}{\frac{3}{4}} = \frac{1}{2}\times\frac{4}{3}$$

$$h[n] = \begin{cases} \frac{2}{3} \end{cases}$$

$$y[n] = \left(\frac{1}{2}\right)^{-n-1} u(-n-1) * u(n-1)$$

$$= 2\left(\frac{1}{2}\right)^{-n} u(-n-1) * u(n-1)$$

$$= 2(2)^{n} u(-n-1) * u(n-1)$$

$$= 2 \cdot \frac{z}{z-2} \cdot \frac{z}{z-1} \cdot \frac{1}{z}$$

$$y[z] = \frac{2z}{(z-1)(z-2)}$$

Q.5 (d) Explain the function of following pins of 8086 microprocessor:

1. $\overline{BHE}$/S7
2. MN/$\overline{MX}$
3. $\overline{TEST}$
4. READY
5. RESET
6. INTR

[12 marks]

Sol:

1) $\overline{BHE}$/S7 :- In this pin in 8086 microprocessor goes high when low signal given, it will make state to hold in high. The tristate.

2) MN/$\overline{MX}$ :- MN = 1 = high = ON

$\overline{MX}$ = 0 = low = ON

It will used to indicate min and maximum of signal.

3) $\overline{Test}$ :- It will be used in up to test the signal that are avaible at the end of the instruction.

4) Ready :- It will be Active high signal, when the up has the device they are availble to take the signal or they are ready to trasfer the signal.

RESET I/O: It is used to Reset the up at a part whole all the pins come to a reset mode;

INTR: It is External interrupt hardware Signal to indicate the up to a interrupt request from the i/o device and External Communication.

**Q.5 (e)** Consider a three input Boolean function $f(a, b, c) = \Sigma m(0, 1, 2, 3, 7)$

**(i)** Implement the function using a minimal network of 2 × 4 decoder and OR gates.

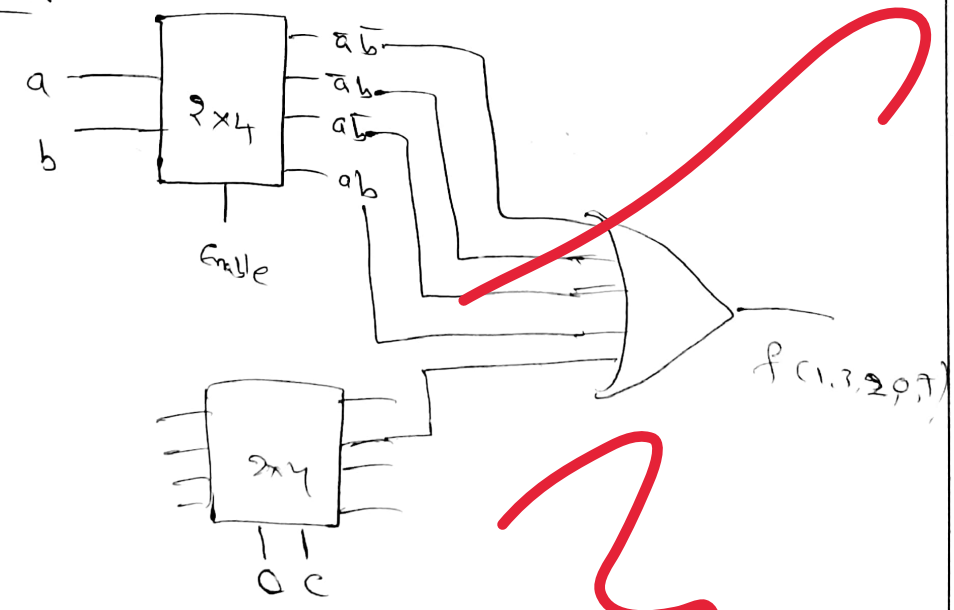
**(ii)** Implement the function using a minimal network of 4 × 1 multiplexers.

**(iii)** Implement the function using a minimal network of 2 × 1 multiplexers.

**[4 + 4 + 4 marks]**

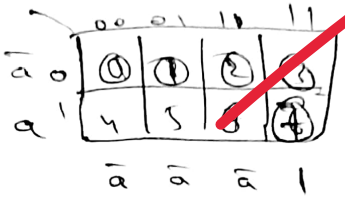
Ans: (i) $f(a,b,c) = \Sigma m(0,1,2,3,7)$

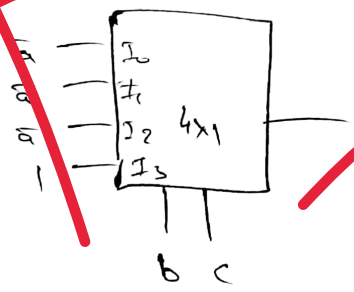
decoder:



(ii) 4×1 mux:

$\Sigma(a,b,c) = \Sigma(0,1,2,3,7)$

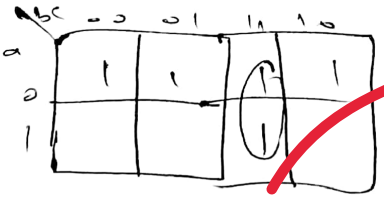


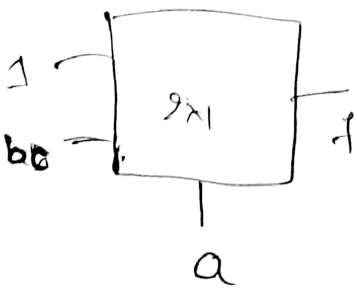

$\Sigma f(1,0,2,3,7)$

(iii) 8×1 MUX:- $\Sigma(a,b,c) = \Sigma(0,1,2,3,7)$

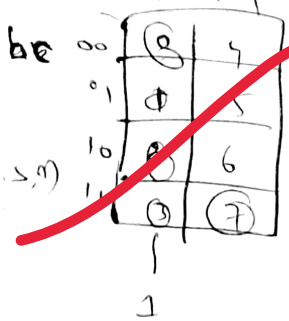
Truth table




$\therefore \bar{a} + bc = \Sigma f(a,b,c)$




Explicit: $\bar{a}$ a




Selection line

Q.6 (a) (i) Write an 8086 assembly language program to add the two BCD data 29H and 98 H and store the result in BCD form in the memory locations 2000 H : 3000 H and 2000 H : 3001 H.

(ii) Explain the series of steps performed by 8086 microprocessor during processing of an interrupt request.

**[10 + 10 marks]**

Sol: (ii) Interrupt Request (INR):

⇒ The Interrupt is the External Signal which is interrupt the ongoing Execution of the Program: During the INTR: The process is going on its Execution of Current instruction and then it will Store the next instruction in the Stack pointer.

Then it will be Executed the interrupt Signal and then it will Come back its original loop and then it will Continous further instructions.

(1) Given Data: A = 29H
B = 98H;

Add this and store in the 2000H : 3000H and 2001H : 3001H.

⇒ Program

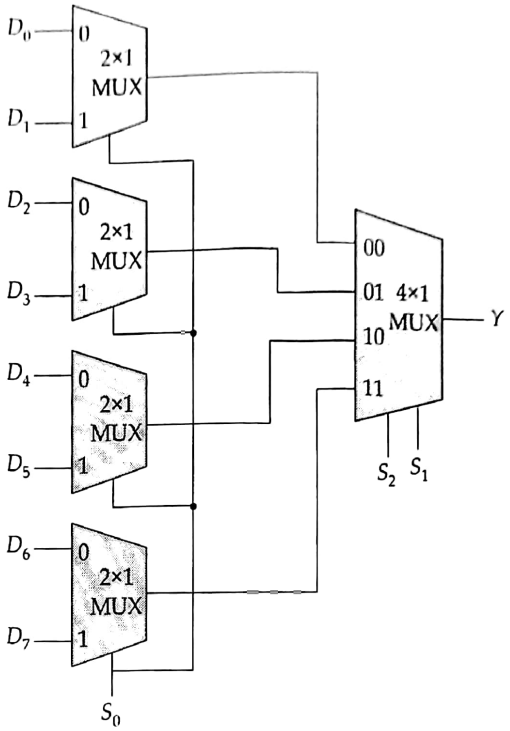
```
MOV A, 29H;
MOV B, A;
MOV C, 98H;
ADD C;
STA 2000H;
HLT.
```

Q.6 (b) (i) Minimize the SOP terms given for a Boolean function,

$f(A, B, C, D) = \Sigma m(2, 3, 8, 10, 11, 12, 14, 15)$

Implement the minimized function using NAND gates alone.

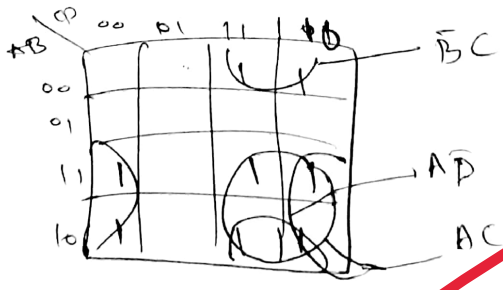
(ii) Determine the logic equation for the output by constructing the truth table for the logic circuit shown in figure below:




**[12 + 8 marks]**

Sol:

$f(A,B,C,D) = \Sigma m(2,3,8,10,11,12,14,15)$



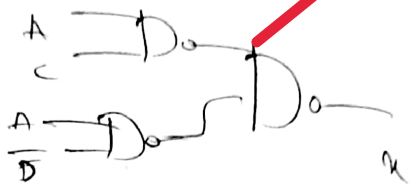

$f(A,B,C,D) = \bar{B}C + A\bar{D} + AC$

It is used to implement using only NAND gate.

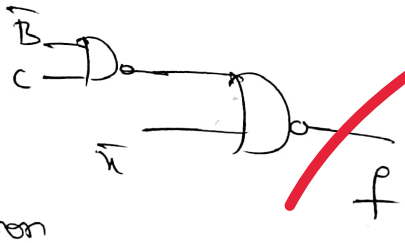
$f(A,B,C,D) = \bar{A}\bar{C} + \bar{A}\bar{D} + BC$

$x = \bar{A}\bar{C} + \bar{A}\bar{D}$

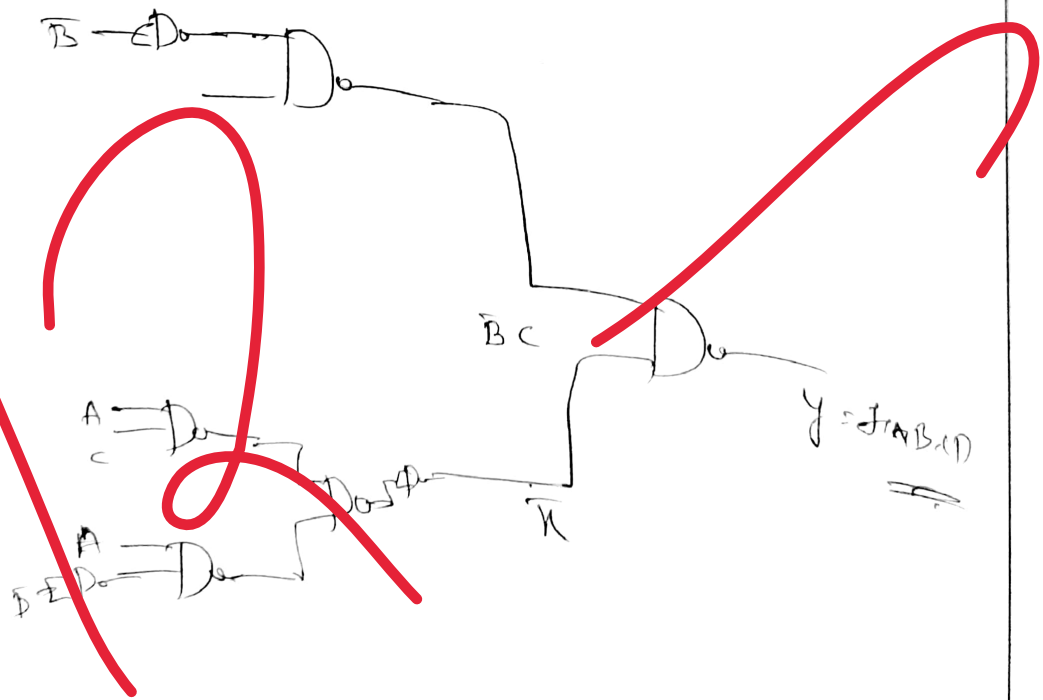
$x = \overline{\bar{A}\bar{C}}\,\overline{\bar{A}\bar{D}}$



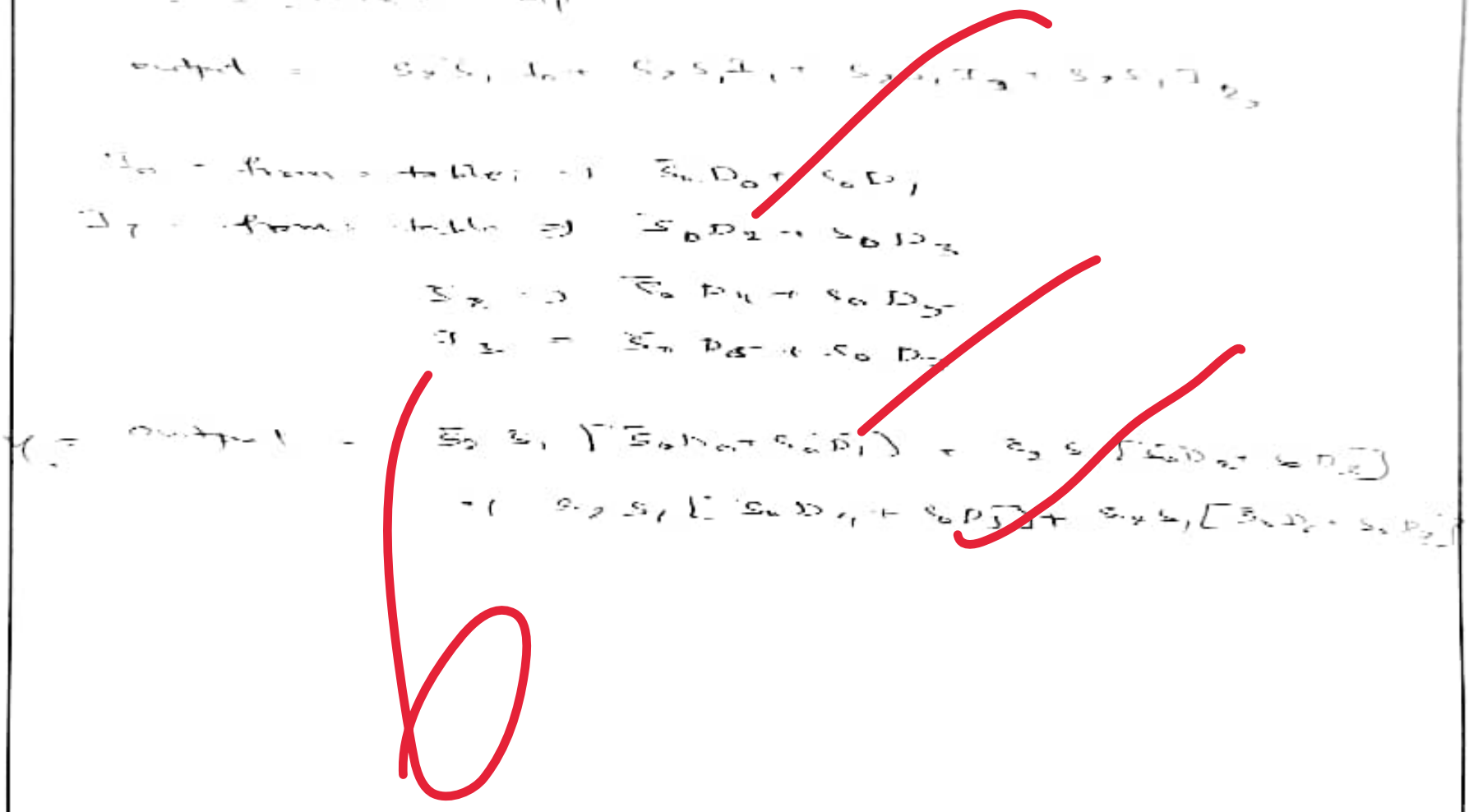

$f(A,B,C,x) = \overline{\overline{x + \bar{B}C}} = \overline{x}\,\overline{\bar{B}C}$




NAND Realization



(11)



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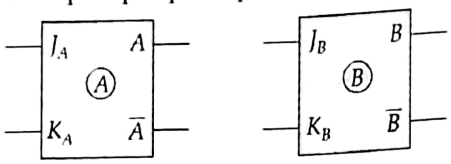
Q.6 (c) A sequential circuit has two J-K flip flops $A$ and $B$ as shown below, two inputs $x$ and $y$, and one output $Z$. The flip flop input equations and circuit output equation are




$J_A = Bx + \bar{B}\bar{y}$; $K_A = \bar{B}x\bar{y}$

$J_B = \bar{A}x$; $K_B = A + x\bar{y}$

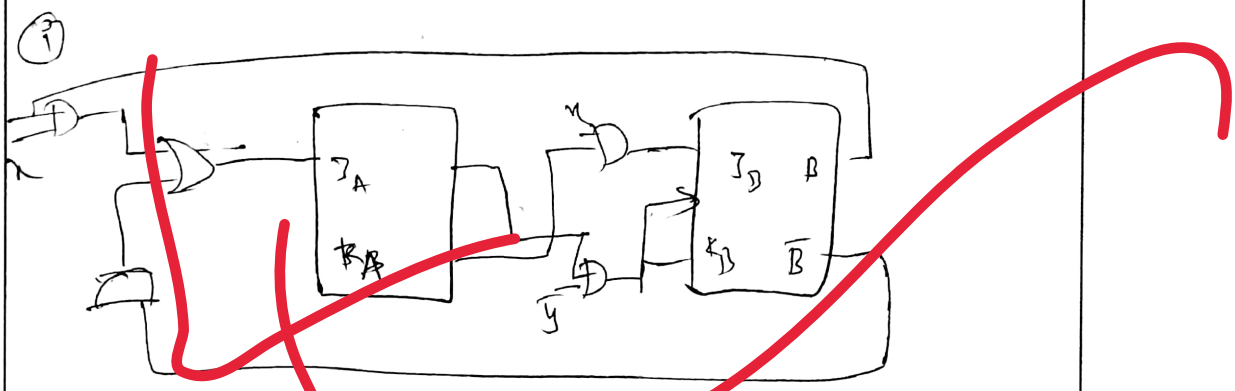
$Z = A\bar{x}\bar{y} + B\bar{x}\bar{y}$

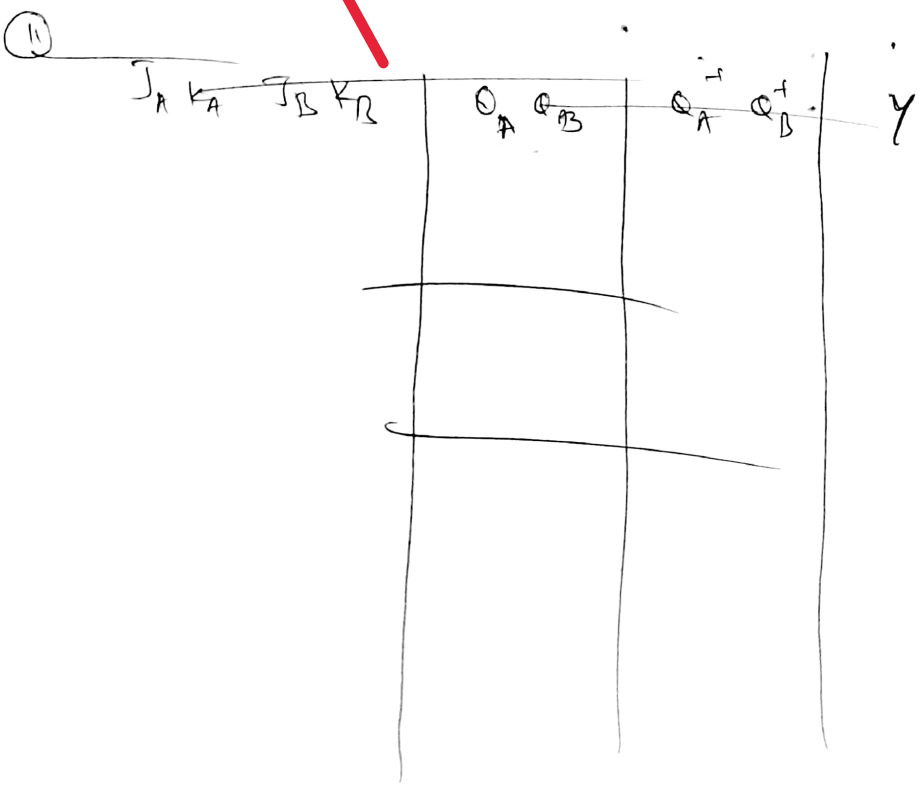
**(i)** Draw the logic diagram of the circuit.

**(ii)** Tabulate the state table.

**(iii)** Derive the state equations for $A$ and $B$.

**[20 marks]**



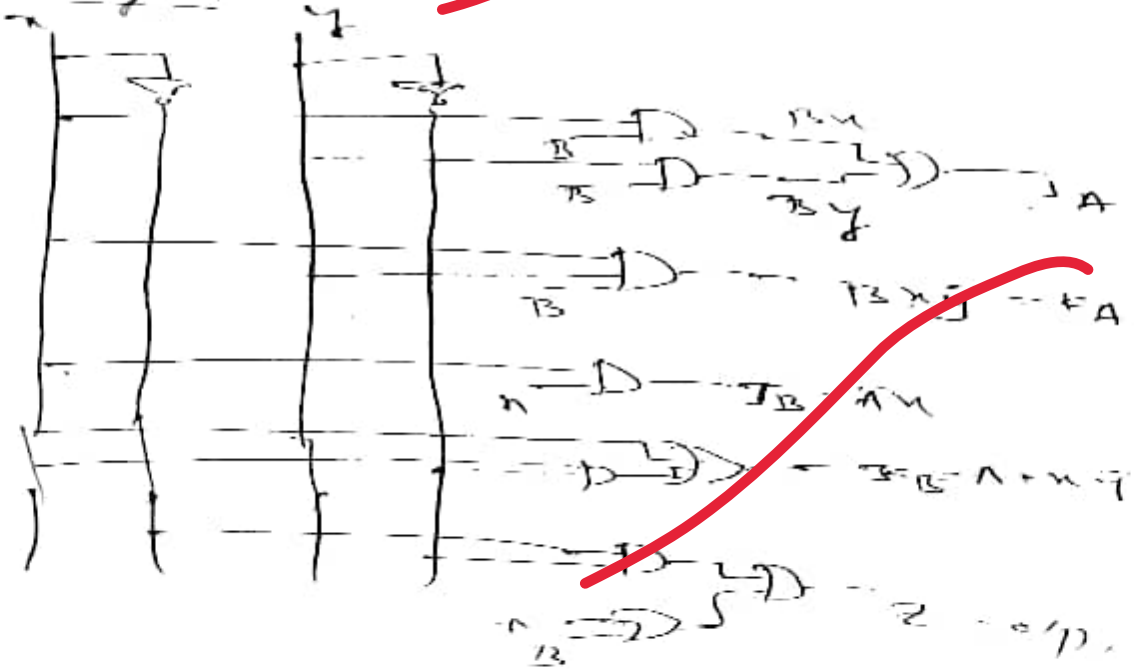


$J_A = B\bar{x} + \bar{B}y$ $K_A = \bar{B}\bar{x}\bar{y}$

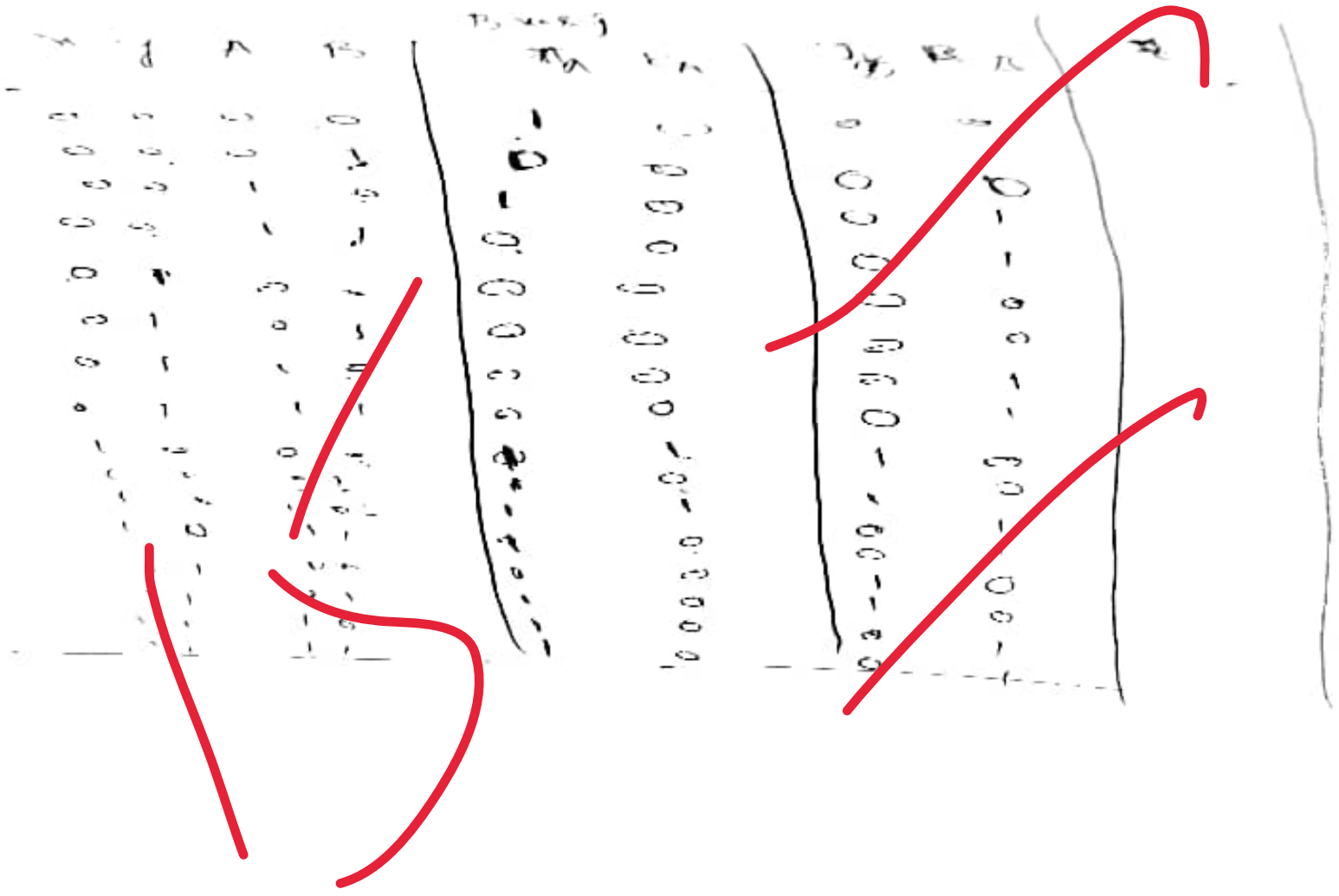
$J_B = Ax$ $K_B = A + \bar{x}\bar{y}$

$Z = A\bar{x}\bar{y} + B\bar{x}y$ $(A + B)\bar{x}\bar{y}$

Logic diagram:




(iii) State table:



Q.7 (a) (i) With a neat block diagram, explain the operation of counter type *ADC*. Give advantages and disadvantages of counter type *ADC*.

(ii) Define fan-out of a gate. A two-input NAND gate specifications are given as $I_{OH(max)} = 0.4$ mA, $V_{OH(min)} = 2.7$ V, $V_{IH(min)} = 2$ V, $V_{IL(max)} = 0.8$ V, $V_{OL(max)} = 0.4$ V, $I_{OL(max)} = 8$ mA, $I_{IL(max)} = 0.4$ mA, $I_{IH(max)} = 25\ \mu A$, $t_{PLH} = t_{PHL} = 15$ nsec and supply voltage of 5 V. Determine

1. High state noise margin.
2. Low state noise margin.
3. Number of NAND gate inputs that can be driven from the output of a NAND gate of this type.

**[12 + 8 marks]**

Q 7 (b) Each of the following arithmetic operation is correct in atleast one number system. Determine the possible bases in each operation.

(i) $3441 + 4235 = 7676$

(ii) $\frac{142}{y} = 16$

(iii) $23 + 44 + 14 + 32 = 223$

(iv) $21 \times 16 = 366$

(v) $\frac{302}{20} = 12.1$

(vi) $\sqrt{51} = 6$

[20 marks]

Q.7 (c) (i) Consider a discrete-time low-pass filter whose impulse response $h[n]$ is known to be real and whose frequency response magnitude in the region $-\pi \le \omega \le \pi$ is given as,

$$\left|H\left(e^{j\omega}\right)\right| = \begin{cases} 1; & |\omega| \le \dfrac{\pi}{3} \\ 0; & \text{otherwise} \end{cases}$$

Determine the real-valued impulse response $h[n]$ for this filter when the corresponding group-delay function is $\tau_g(\omega) = \dfrac{3}{2}$.

(ii) Design a block level architecture of a 5 coefficient FIR filter by using appropriate number of multipliers, adders and registers. Assume that all the input operands are available in 4 bit, 2's complement fixed point representation. The architecture should give one output per clock cycle.

**[10 + 10 marks]**

Q.8 (a) (i) Draw the block diagram of programmable peripheral interface 8255A.

(ii) Explain BSR (Bit Set/Reset) mode of 8255A

(iii) Write a BSR control word subroutine to set bits $PC_7$ and $PC_3$ and reset them after some delay, using the below I/O port addresses.

| $\overline{CS}$ | | | | | | | | Hexadecimal Address | Port |
|---|---|---|---|---|---|---|---|---|---|
| $A_7$ | $A_6$ | $A_5$ | $A_4$ | $A_3$ | $A_2$ | $A_1$ | $A_0$ | | |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | = 80H | A |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | = 81H | B |
| 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | = 82H | C |
| 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | = 83H | Control Register |

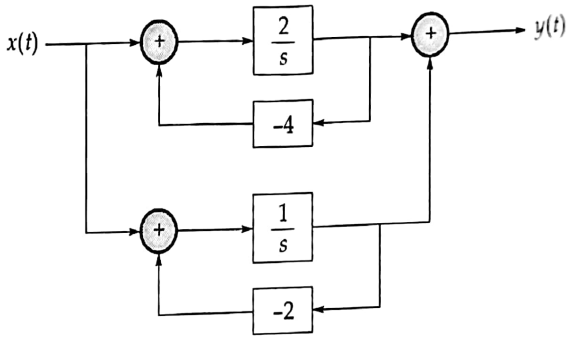
**[20 marks]**

Q.8 (b) (i) Suppose we are given the following information about a continuous time periodic signal $x(t)$ with period 3 and Fourier series coefficients $a_k$:

1. $a_k = a_{k+2}$
2. $a_k = a_{-k}$
3. $\int_{-0.5}^{0.5} x(t)dt = 1$
4. $\int_{0.5}^{1.5} x(t)dt = 2$

Determine $x(t)$.

(ii) A causal LTI system '$S$' has the block diagram representation as shown in figure below.

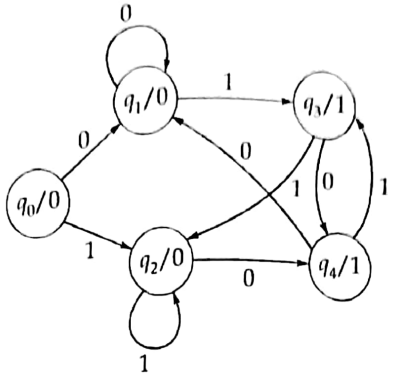



Determine a differential equation relating the input $x(t)$ to the output $y(t)$ of this system.

[10 + 10 marks]

Digital screen designer

Q.8 (c) Consider the state diagram of Moore machine shown below:




Get the excitation equations and Boolean equations for output Z of Mealy machine. Also design the Mealy machine using J-K flip-flop.

**[20 marks]**

Space for Rough Work