MADE EASY

Leading Institute for ESE, GATE & PSUs

ESE 2025 : Mains Test Series

UPSC ENGINEERING SERVICES EXAMINATION

Electronics & Telecommunication Engineering

Test-2 : Digital Circuits + Signals and Systems + Microprocessors & Microcontroller [All topics]

Name : ....

Roll No :

Test Centres				Student's Signature
Delhi ☐ ✓	Bhopal ☐	Jaipur ☐	Pune ☐	
Kolkata ☐	Hyderabad ☐			

Instructions for Candidates

1. Do furnish the appropriate details in the answer sheet (viz. Name & Roll No).
2. There are Eight questions divided in TWO sections.
3. Candidate has to attempt FIVE questions in all in English only.
4. Question no. 1 and 5 are compulsory and out of the remaining THREE are to be attempted choosing at least ONE question from each section.
5. Use only black/blue pen.
6. The space limit for every part of the question is specified in this Question Cum Answer Booklet. Candidate should write the answer in the space provided.
7. Any page or portion of the page left blank in the Question Cum Answer Booklet must be clearly struck off.
8. There are few rough work sheets at the end of this booklet. Strike off these pages after completion of the examination.

FOR OFFICE USE

Question No.	Marks Obtained
Section-A	
Q.1	41
Q.2	40
Q.3	33
Q.4	/
Section-B	
Q.5	39
Q.6	36
Q.7	/
Q.8	/
Total Marks Obtained	189

Signature of Evaluator: Ch. Rupf-1- ....

Cross Checked by ....

• Good attempt deep at.
• Keep it up.

IMPORTANT INSTRUCTIONS

CANDIDATES SHOULD READ THE UNDERMENTIONED INSTRUCTIONS CAREFULLY. VIOLATION OF ANY OF THE INSTRUCTIONS MAY LEAD TO PENALTY.

DONT'S

1. Do not write your name or registration number anywhere inside this Question-cum-Answer Booklet (QCAB).
2. Do not write anything other than the actual answers to the questions anywhere inside your QCAB.
3. Do not tear off any leaves from your QCAB, if you find any page missing do not fail to notify the supervisor/invigilator.
4. Do not leave behind your QCAB on your table unattended, it should be handed over to the invigilator after conclusion of the exam.

DO'S

1. Read the Instructions on the cover page and strictly follow them.
2. Write your registration number and other particulars, in the space provided on the cover of QCAB.
3. Write legibly and neatly.
4. For rough notes or calculation, the last two blank pages of this booklet should be used. The rough notes should be crossed through afterwards.
5. If you wish to cancel any work, draw your pen through it or write "Cancelled" across it, otherwise it may be evaluated.
6. Handover your QCAB personally to the invigilator before leaving the examination hall.

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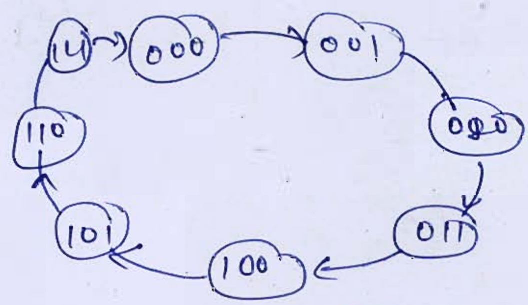
Section A : Digital Circuits + Signals and Systems + Microprocessors & Microcontroller

Q.1 (a) Design a 3-bit binary counter using T-flip-flops.

[12 marks]

let design 3 bit sync up counter using T flip-flops

state ~~table~~ diagram



state table

excitation table

Present state $Q_2\ Q_1\ Q_0$	Next state $Q_2^+\ Q_1^+\ Q_0^+$	T_2	T_1	T_1
0 0 0	0 0 1	0	0	1
0 0 1	0 1 0	0	1	1
0 1 0	0 1 1	0	0	1
0 1 1	1 0 0	1	1	1
1 0 0	1 0 1	0	0	1
1 0 1	1 1 0	0	1	1
1 1 0	1 1 1	0	0	1
1 1 1	0 0 0	1	1	1

K-map

$T_2 =$

$Q_2 \backslash Q_1Q_0$	00	01	11	10
0	0	0	1	0
1	0	0	1	0

$T_2 = Q_1 Q_0$

$T_1 =$

$Q_2 \backslash Q_1Q_0$	00	01	11	10
0	0	1	1	0
1	0	1	1	0

$T_1 = Q_0$

$T_0 =$

$Q_2 \backslash Q_1Q_0$	00	01	11	10
0				
1				

$\boxed{T_0 = 1}$

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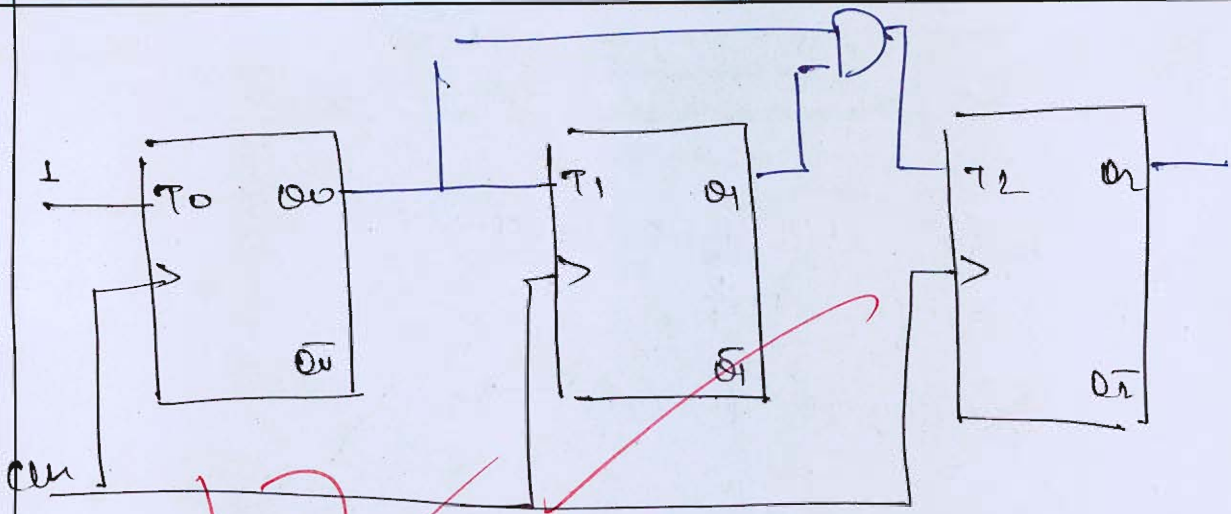


Q.1 (b) **(i)** Draw the circuit for interfacing 512 bytes of memory to 8085 microprocessor using 3 × 8 decoder.

(ii) Write an assembly language program to move a block of Data of 16 bytes starting from address 2050H to another location starting from 2070H in 8085 microprocessor.

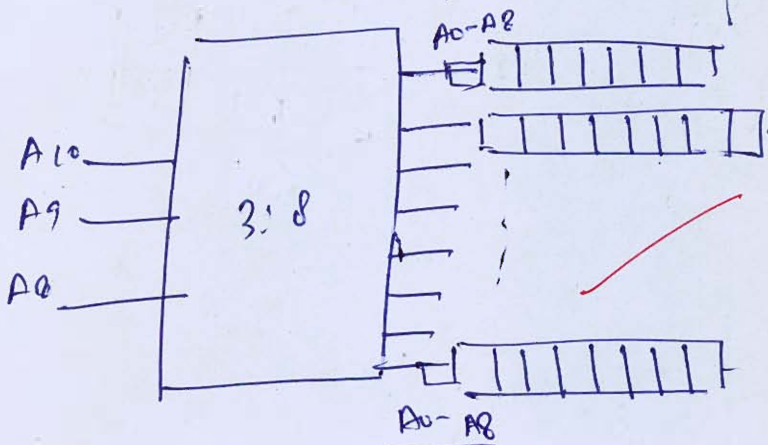
[7 + 5 marks]

512 Bytes :- $2^9 \times 8$

There in this case no. of address lines = 9

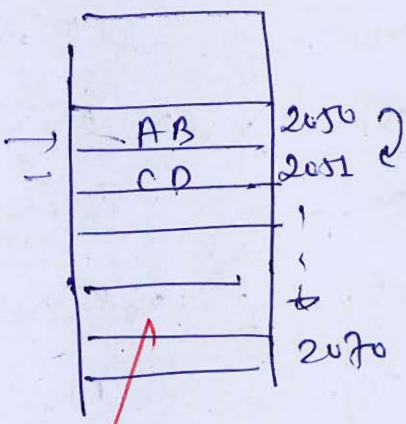
& no. of data lines = 8

$\underbrace{A_{15}\ A_{14}\ A_{13}\ A_{12}\ A_{11}\ A_{10}\ A_9}_{\text{higher order add line}}\ |\ \underbrace{A_8\ A_7\ A_6\ A_5\ A_4\ A_3\ A_2\ A_1\ A_0}_{\text{lower address Bus}}$



(11)

16 byte = 16×8 bit



~~LXI H, 2050~~

(i) LDA, 2050

~~MOV~~

STA, 2070

LDA 2051

STA, 2071

HALT

~~LDA,~~

~~L1: LXI H, 2050~~

~~INX H~~

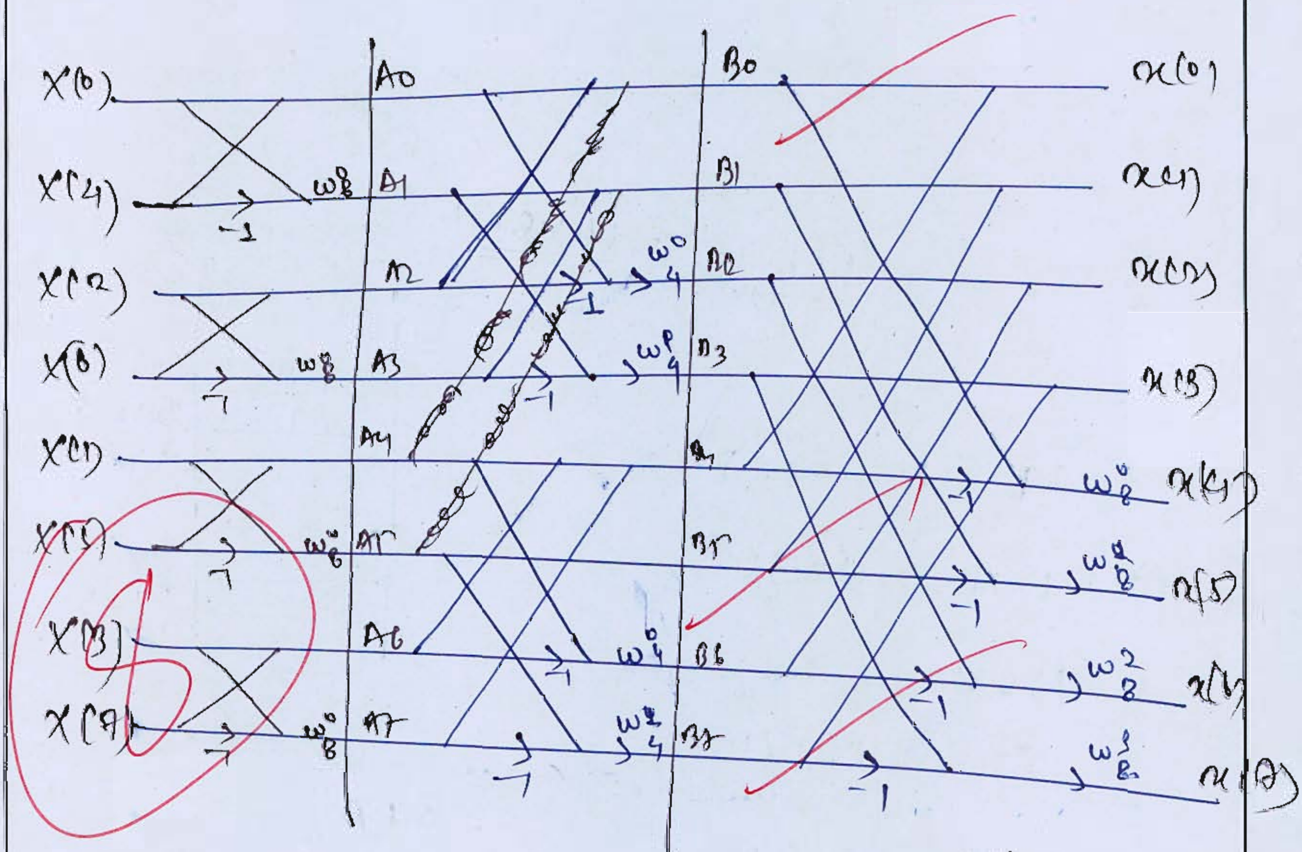
Q.1 (c) (i) Draw the signal flow graph (Butterfly structure) for the computation of 8-point IDFT using inverse Radix-2 DIF-FFT.

(ii) State and prove Initial-value theorem of z-transform.

[8 + 4 marks]

$x(n) = \{x(0), x(1), x(2), x(3), x(4), x(5), x(6), x(7)\}$

(1)



$A_0 = X(0) + X(4)$

$A_1 = (X(0) - X(4))\, W_8^0$

$A_2 = [X(2) + X(6)]$

$A_3 = [X(2) - X(6)]\, W_8^0$

$A_4 = [X(1) + X(5)]$

$A_5 = [X(1) - X(5)]\, W_8^0$

$A_6 = [X(3) + X(7)]$

$A_7 = (X(3) - X(7))\, W_8^0$

Similarly

$B_0 = (A_0 + A_2)$

$B_1 = A_1 + A_3$

$B_2 = (A_0 - A_2)\, W_4^0$

$B_3 = (A_1 - A_3)\, W_4^1$

$B_4 = (A_4 + A_6)$

$B_5 = (A_5 + A_7)$

$B_6 = (A_4 - A_6)\, W_4^0$

$B_7 = (A_5 + A_7)\, W_4^1$.

Do not write in this margin

where $W_N^{kn} = e^{\frac{j2\pi kn}{N}}$

$W_8^0 = 1$

& finally

$x(0) = B0 + B4.$
$x(1) = B1 + B5$
$x(2) = B2 + B6$
$x(3) = B3 + B7$

$x(4) = (B0 - B4) w_8^0$
$x(5) = (B1 - B5) w_8^1$
$x(6) = (B2 - B6) w_8^2$
& $x(7) = (B3 - B7) w_8^3$

(iv) Initial value Theorem :→ states that there exist some value at initial stage, i.e. $t=0$,

$y(t) \xrightarrow{IVT} = \lim_{t \to 0} y(t) =$ finite

Taking the laplace of $y(t)$

$\boxed{y(s) = \underset{IVT}{\text{Initial}} = \lim_{s \to \infty} s \cdot Y(s)}$

Similarly for Z-transform

$y(n) \xleftrightarrow{z} Y(z)$

In Z-~~time~~ domain $\lim_{n \to 0}$

$\boxed{\lim_{z \to \infty} Y(z).}$

Dear. Student, doit in Z-Transform only as it was asked in Question.

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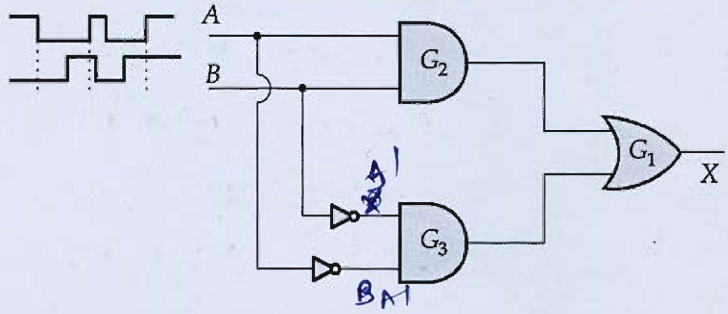
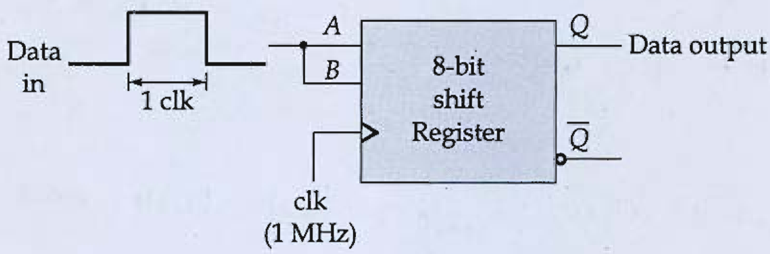
Q.1 (d) (i) Draw the timing diagram for the logic circuit in the figure shown with outputs of G_1, G_2 and G_3 with input waveform A and B as indicated.



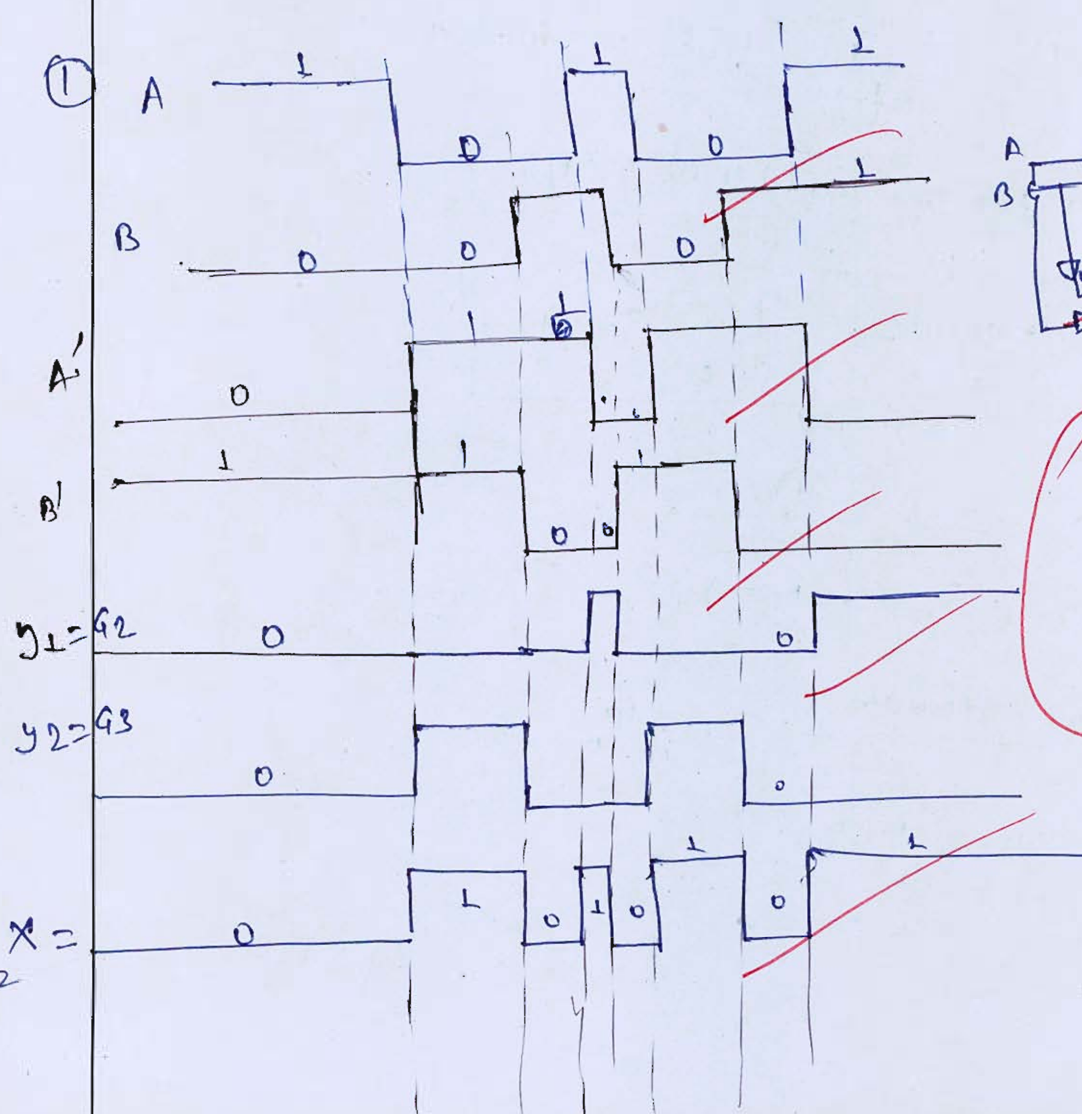
(ii) Consider the serial in-serial out shift register which is used to provide time delay from input to output.

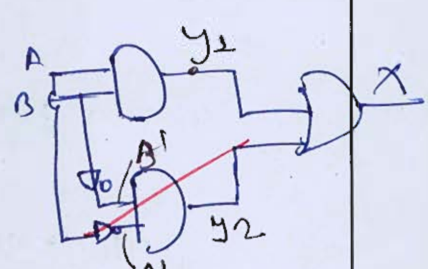


Draw and calculate the output and delay provided by the above shift register in clear steps.

[6 + 6 marks]

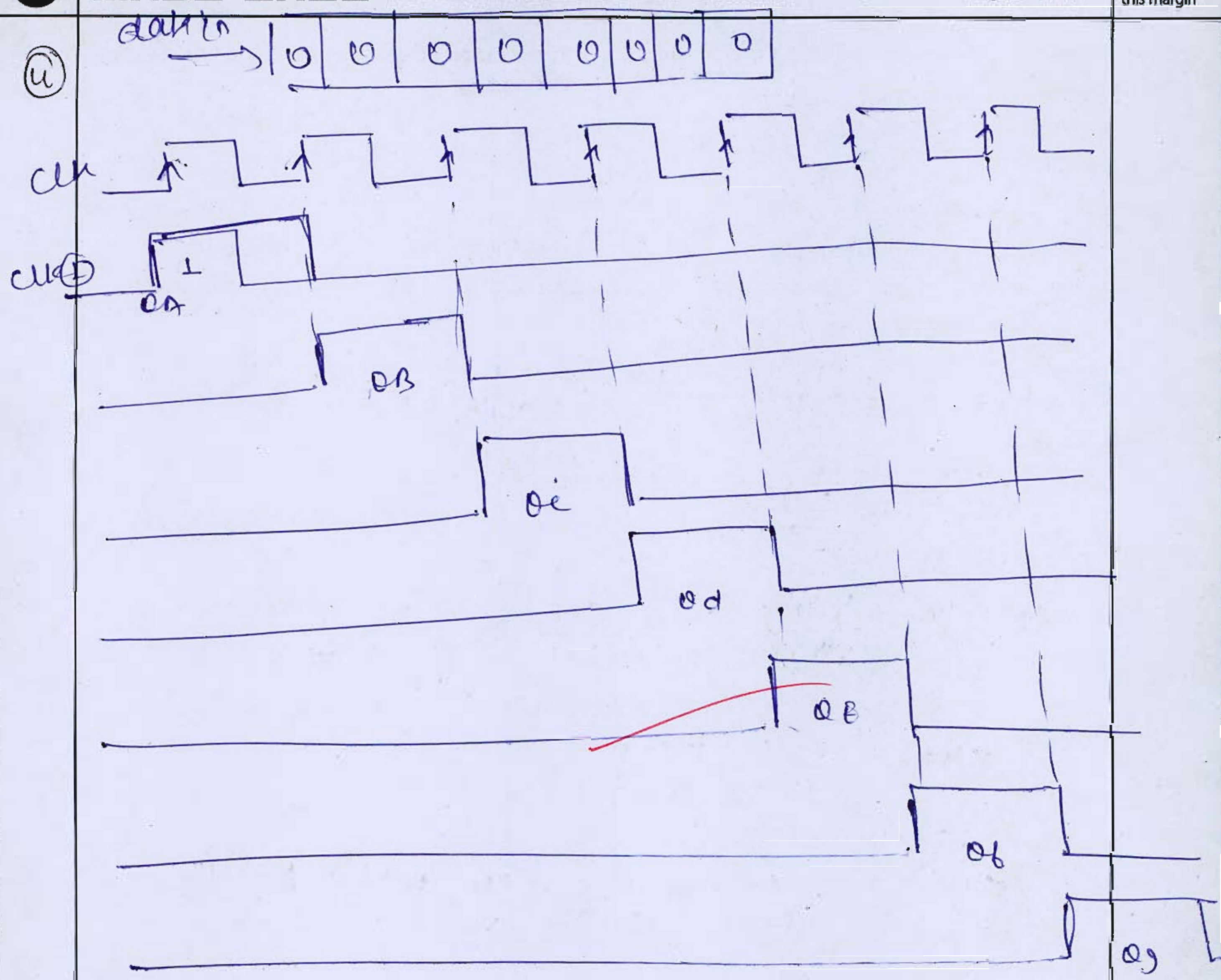
(1)





6

(ii)



$\boxed{\text{delay} = 8\,T_{clk}}$

6

Q.1 (e) Consider the signal $y(t) = e^{-2t}u(t)$ is the output of a causal all-pass system for which the system function is

$$H(s) = \frac{s-1}{s+1}$$

(i) Find and sketch at least two possible inputs $x(t)$ that could produce $y(t)$.

(ii) From the solutions obtained in part (i), what is the input $x(t)$ if it known that a stable system exists that will have $x(t)$ as an output and $y(t)$ as the input? Find the impulse response $h(t)$ for this system.

[6 + 6 marks]

$y(t) = e^{-2t}u(t) \xrightarrow{LT} \frac{1}{s+2}, \ \sigma > -2$

$H(s) = \frac{s-1}{s+1}$.

$H(s) = \frac{Y(s)}{X(s)} = \frac{s-1}{s+1} = \frac{1}{(s+2)\,X(s)}$

$X(s) = \frac{1}{(s+2)} \cdot \frac{(s+1)}{(s-1)}$

$X(s) = \frac{A}{(s+2)} + \frac{B}{(s-1)}$ By partial fraction

$A(s-1) + B(s+2) = (s+1)$

put $s = 1$, $B(3) = 2$

$\boxed{B = 2/3}$

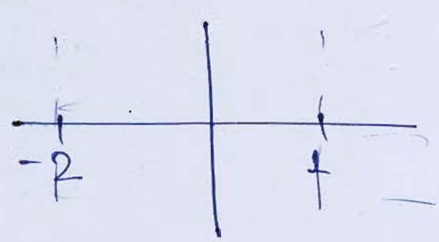
put $s = -2$, $A(-3) = -1$

$\boxed{A = \frac{1}{3}}$

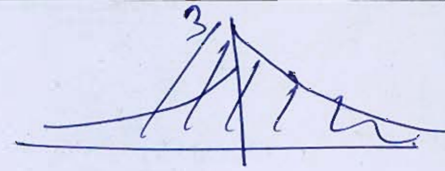
~~$x(t) = 3e$~~ Now $X(s) = \frac{\frac{1}{3}}{(s+2)} + \frac{2}{3(s-1)}$

Case 1 $\sigma > 1$

$x(t) = \left(\frac{1}{3}e^{-2t} + \frac{2}{3}e^{t}\right)u(t)$



which is causal system.



case (ii) $-2<\sigma<1$

$x(t) = \boxed{3e^{-2t}u(t) - \frac{2}{3}e^{t}u(-t)}$

(ii) If it is known that the system is stable

than

ROC; $\boxed{-2<\sigma<1}$

$\therefore$ $x(t) = 3e^{-2t}u(t) - \frac{2}{3}e^{t}u(-t)$

~~taking~~ Now given that

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Q.2 (a) Implement the state diagram and sequential circuit diagram using JK flip-flops for 3-bit Gray code counter.

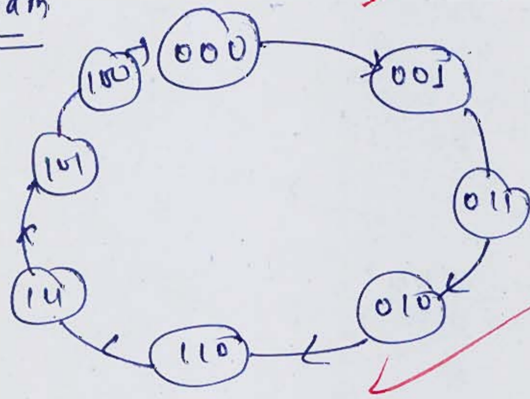
[20 marks]

Binary	Gray code
0 0 0	0 0 0
0 0 1	0 0 1
0 1 0	0 1 1
0 1 1	0 1 0
1 0 0	1 1 0
1 0 1	1 1 1
1 1 0	1 0 1
1 1 1	1 0 0

Excitation

Q_n	Q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

state diagram



state Table

	Present Q_2 Q_1 Q_0	Nx. state Q_2^+ Q_1^+ Q_0^+	J_2 K_2	J_1 K_1	J_0 K_0
m0	0 0 0	0 0 1	0 X	0 X	1 X
m1	0 0 1	0 1 1	0 X	1 X	X 0
m3	0 1 1	0 1 0	0 X	X 0	X 1
m2	0 1 0	1 1 0	1 X	X 0	0 X
m6	1 1 0	1 1 1	X 0	X 0	1 X
m7	1 1 1	1 0 1	X 0	X 1	X 0
m5	1 0 1	1 0 0	X 0	0 X	X 1
m4	1 0 0	0 0 0	X 1	0 X	0 X

J_2 =

$Q_2 \backslash Q_1Q_0$	00	01	11	10
0	0	0	0	1
1	X	X	X	X

$J_2 = Q_1 \bar{Q_0}$

K_2 =

$Q_2 \backslash Q_1Q_0$	00	01	11	10
0	X	X	X	X
1	1	0	0	0

$K_2 = \bar{Q_1}\bar{Q_0}$

J_1 =

$Q_2 \backslash Q_1Q_0$	00	01	11	10
0	0	1	X	X
1	0	0	X	X

$J_1 = \bar{Q_2} Q_0$

K_1 =

$Q_2 \backslash Q_1Q_0$	00	01	11	10
0	X	X	0	0
1	X	X	1	0

$K_1 = \cancel{Q_2 Q_0} = Q_2 Q_0$

J_0 =

$Q_2 \backslash Q_1Q_0$	00	01	11	10
0	1	X	X	0
1	0	X	X	1

$J_0 = \bar{Q_2}\bar{Q_1} + Q_2 Q_1$

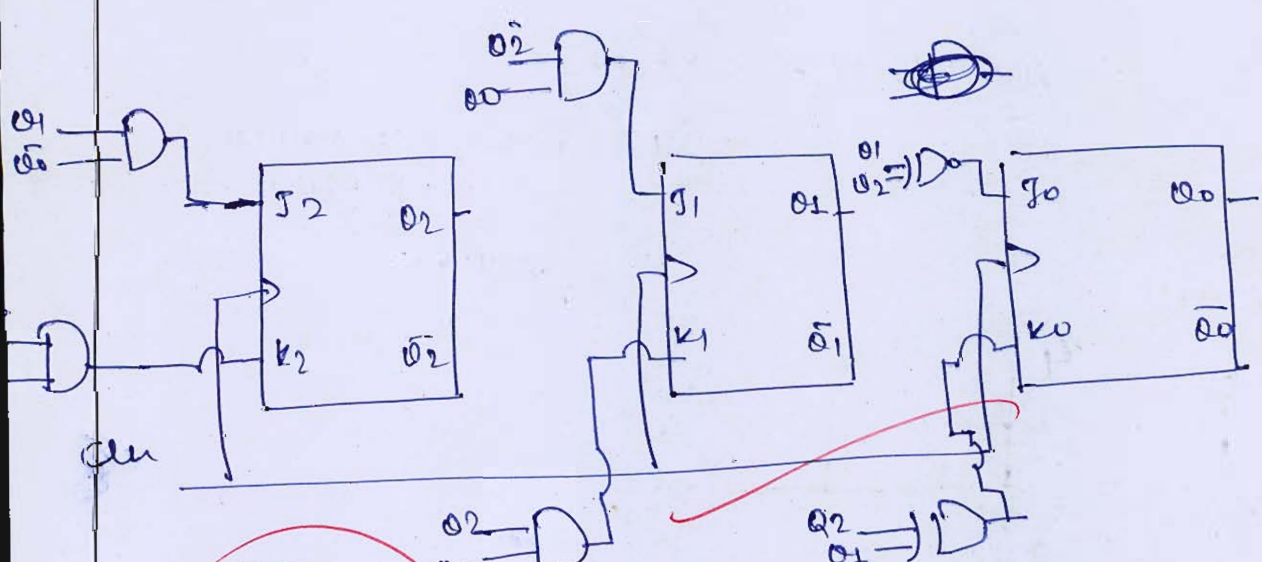
$\Rightarrow Q_2 \odot Q_1$

K_0 =

$Q_2 \backslash Q_1Q_0$	00	01	11	10
0	X	0	1	X
1	X	1	0	X

$K_0 = \bar{Q_2} Q_1 + Q_2 \bar{Q_1}$

$= Q_2 \oplus Q_1$



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Q.2 (b) **(i)** Determine and sketch $y(t)$, the convolution of the two signals given below:

$$x(t) = \begin{cases} 2, & -1 \le t \le 1 \\ 1, & 1 < t \le 3 \\ 0, & \text{elsewhere} \end{cases}$$

and $h(t) = 2\delta(t+1) + \delta(t+2)$

(ii) The output $y(t)$ of a causal LTI system is related to the input $x(t)$ by the equation

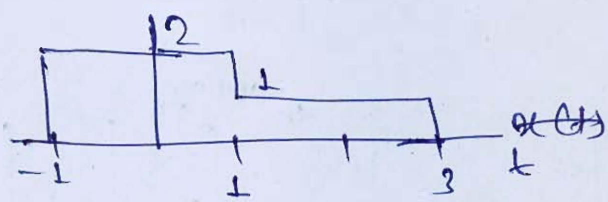
$$\frac{dy(t)}{dt} + 10y(t) = \int_{-\infty}^{\infty} x(\tau)z(t-\tau)d\tau - x(t)$$

where, $z(t) = e^{-t}u(t) + \delta(t)$

Determine the impulse response of the system.

[10 + 10 marks]

$x(t) =$



$h(t) = 2\delta(t+1) + \delta(t+2)$

$y(t) = x(t) * h(t)$

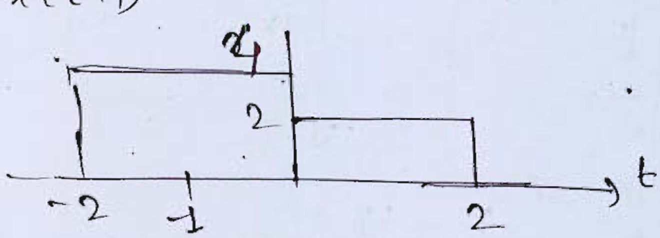
$= x(t) * (2\delta(t+1) + \delta(t+2))$

$= \underline{2x(t+1) + x(t+2)}$

↳ using convolution property

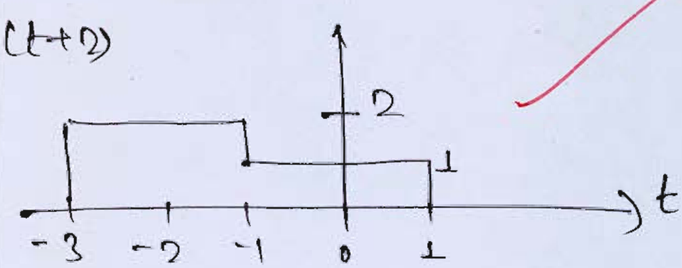
$\boxed{x(t) * \delta(t) = x(t)}$

$2\, x(t+1)$

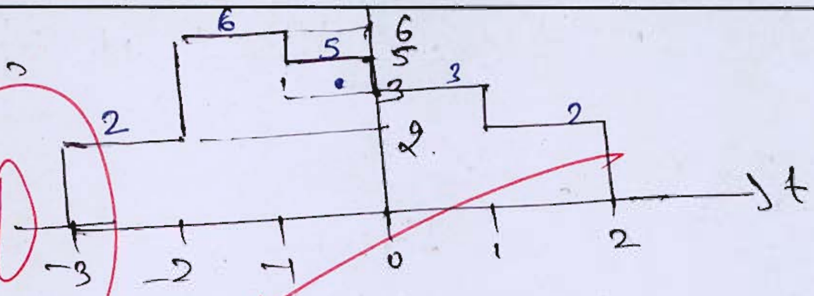


$+$

$x(t+2)$



$y(t) =$



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(4) $\frac{dy(t)}{dt} + 10y(t) = \int_{-\infty}^{\infty} x(\tau)\cdot z(t-\tau)\cdot d\tau - x(t)$

$\therefore \int_{-\infty}^{\infty} x(\tau) * z(t-\tau)\cdot d\tau = \underline{x(t) * z(t)}$

$\frac{dy(t)}{dt} + 10y(t) = x(t) * z(t) - x(t)$

Taking laplace transfom.

$z(s) = \frac{1}{s+1} + 1$

$s\,y(s) + 10\,y(s) = X(s)\cdot z(s) - X(s)$

$y(s)(s+10) = X(s)(z(s) - 1)$

$y(s)(s+10) = X(s)\left(\frac{1}{s+1} + \cancel{1} - \cancel{1}\right)$

$\frac{y(s)}{X(s)} = H(s) = \frac{1}{(s+1)(s+10)}$

By partial fraction

$H(s) = \frac{A}{(s+1)} + \frac{B}{(s+10)}$

$A(s+10) + B(s+1) = 1.$

Res $s = -1$, $A = \frac{1}{9}$ & Res $s = -10$, $B = -\frac{1}{9}$

$H(s) = \frac{1}{9} \times \frac{1}{(s+1)} - \frac{1}{9} \frac{1}{(s+10)}$

taking Inverse Laplace transform | for causal LTI

(i) $h(t) = \frac{1}{9}\left(e^{-t} - e^{-10t}\right)u(t)$ $\sigma > -1$

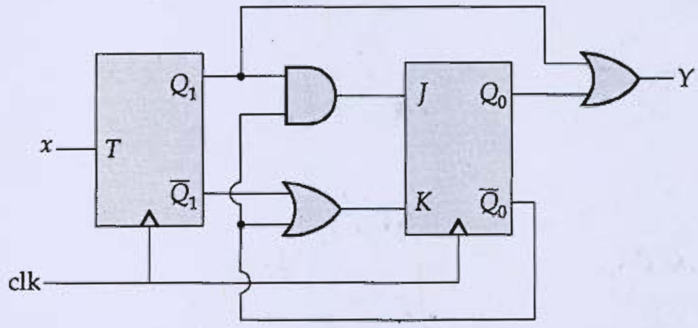
10

Q.2 (c) (i) Interface 4 KB memory to 8085 with starting address A000H.
Design address decoding circuit using (i) 3 × 8 decoder and (ii) using only NAND gates.

(ii) Write an algorithm and assembly language program, to perform the multiplication of two 8 bit numbers using 8085.

[10 + 10 marks]

Q.3 (a) (i) Draw the state diagram of the sequential circuit shown in figure below:



(ii) Find the z-transform of the given signal $x[n]$ using scaling in the z-domain property.

$$x[n] = a^n \sin(\omega_0 n)\, u[n].$$

[10 + 10 marks]

(1)

Present state Q_1 Q_0	input X	T	J K	next state Q_1^+ Q_0^+	y
0 0	0	0	0 1	0 0	0
0 0	1	1	0 1	1 0	0
0 1	0	0	0 1	0 0	1
0 1	1	1	0 1	1 0	1
1 0	0	0	1 1	1 1	1
1 0	1	1	1 1	0 1	1
1 1	0	0	0 0	1 1	1
1 1	1	1	0 0	0 1	1

$T = X$

$J = Q_1 \cdot \bar{Q}_0$

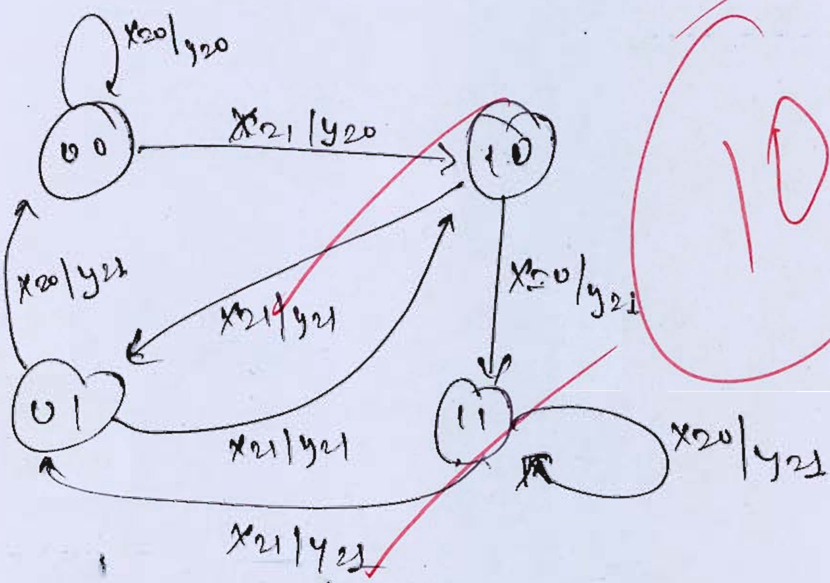
$K = \bar{Q}_1 + \bar{Q}_0$

$y = Q_1 + Q_0$

In this diagram we have 4 states viz, $\boxed{00, 01, 10, \& 11}$

one input = x

and output = y



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(ii)

$$x(n) - a^n u(n) \xrightarrow{ZT} \frac{1}{1-az^{-1}}.$$

$$x(n) - \sin \omega_0 (n) \xrightarrow{ZT} \frac{z^{-1}\sin\omega_0}{1-2z^{-1}\cos\omega_0 + z^{-2}}$$

$$x(n) \longleftrightarrow X(z)$$

$$\boxed{a^n x(n) \longrightarrow \cancel{\frac{1}{|a|}}\, X(z/a)}$$

$$x(n) = a^n \sin(\omega_0 n) u(n) \xrightarrow{ZT} \frac{1}{|a|} \times \frac{(z/a)^{-1}\sin\omega_0}{1-2(z/a)^{-1}\cos\omega_0 + (z/a)^{-2}}$$

$$= \boxed{\frac{z^{-1}a\cdot \sin\omega_0}{1-2z^{-1}a\cos\omega_0 + z^{-2}a^2}}$$

So by using the scaling in the z-domain property

$$\cancel{(a^n \sin w_0(n))} u(n) \longrightarrow \frac{a z^{-1} \sin w_0}{1 - a z^{-1} \cos w_0 + z^{-2} a^2}$$

S

Steps should be more clear.

Q.3 (b) (i) Implement the following Boolean function using 3 × 4 × 2 PLA, also write the PLA programming table.

$F_1(A, B, C) = \Sigma m(0, 1, 2, 4)$

$F_2(A, B, C) = \Sigma m(0, 5, 6, 7)$

(ii) A 6-bit dual slope ADC uses a reference of 12 V and a fixed count of 010110. Convert the maximum input voltage accurately in digital form.

[15 + 5 marks]

(1) $F_1(A, B, C) = \Sigma m(0, 1, 2, 4)$

$F_1 =$

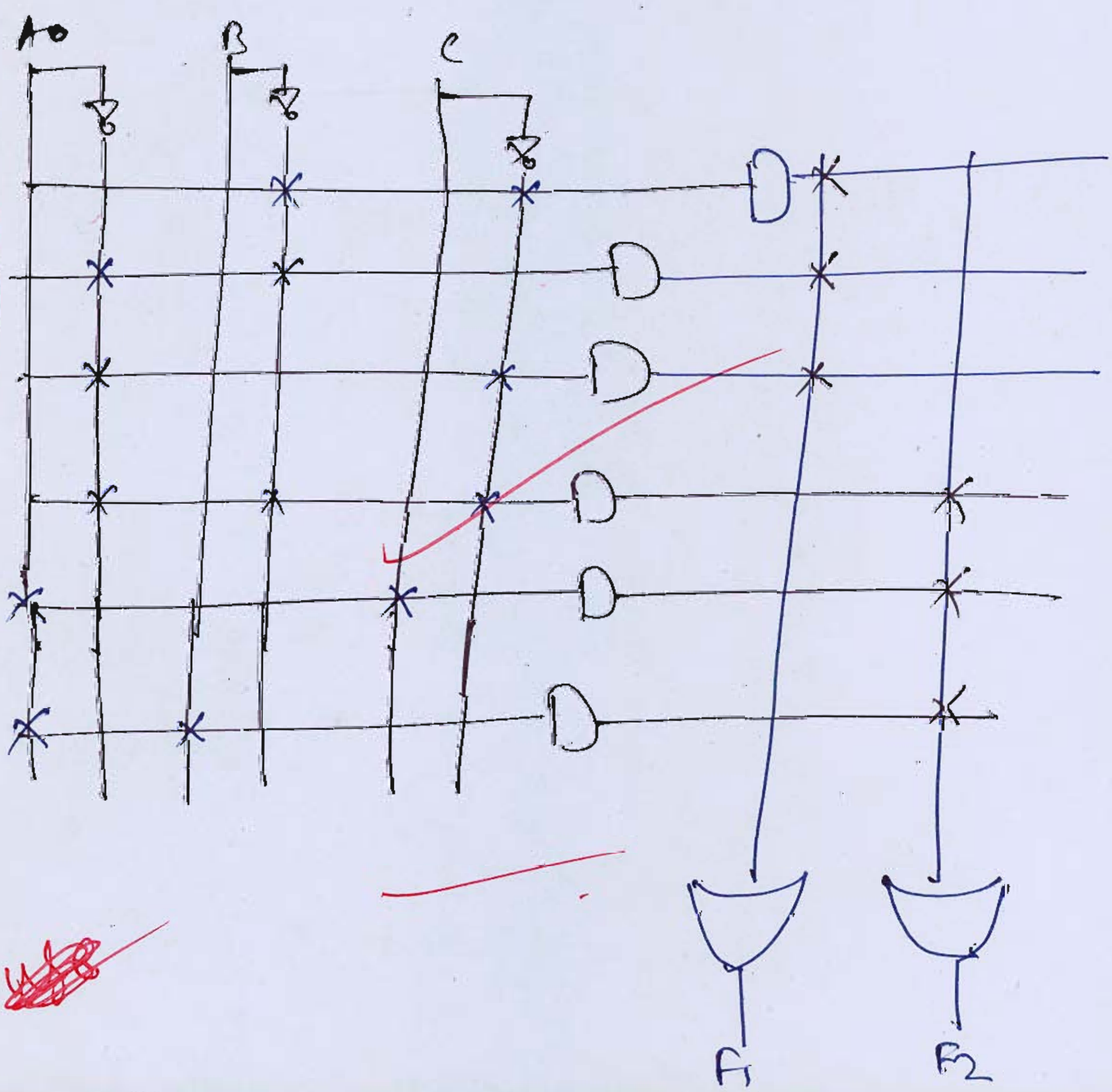
A \ BC	00	01	11	10
0	1	1	0	1
1	1	0	0	0

$F_2 =$

A \ BC	00	01	11	10
0	1	0	0	0
1	0	1	1	1

$F_1 = \bar{B}\bar{C} + \bar{A}\bar{B} + \bar{A}\bar{C}$

$F_2 = \bar{A}\bar{B}\bar{C} + AC + AB$



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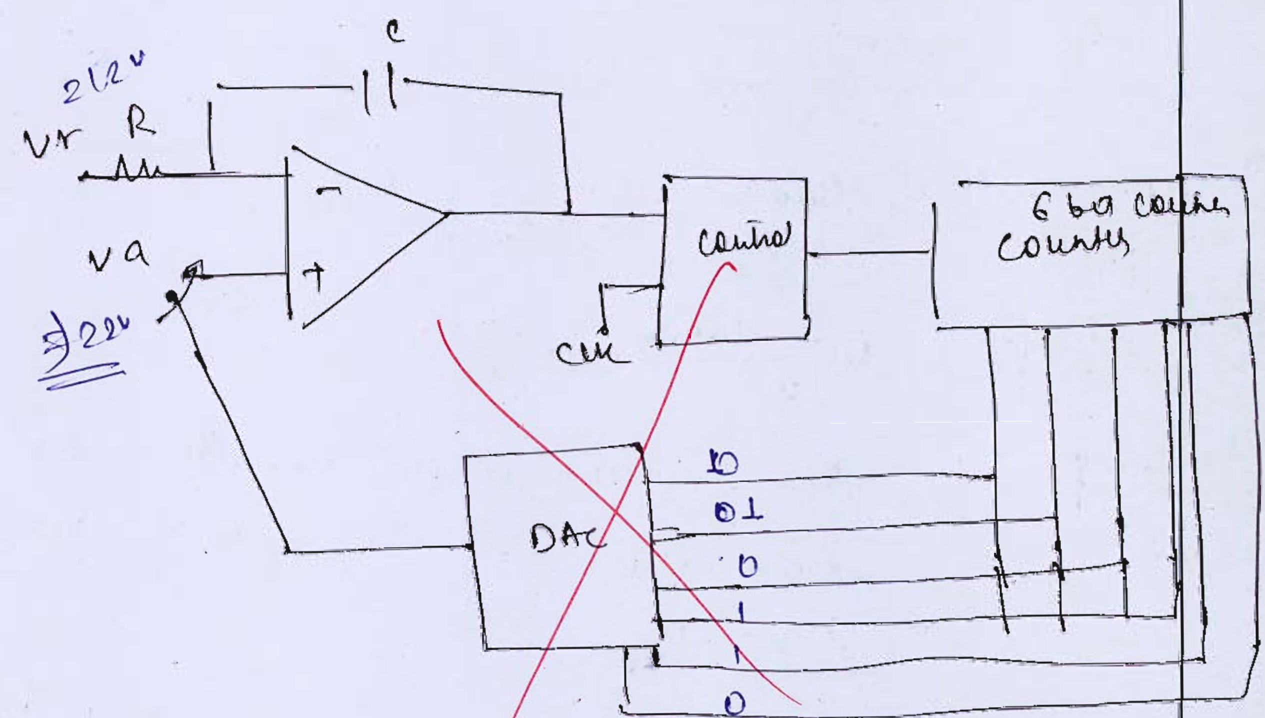
A B C

(i)



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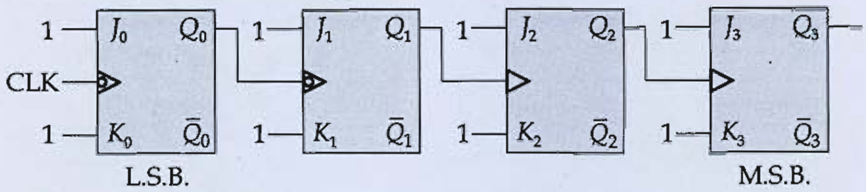
Don't write unnecessary content, especially when it is not asked in question

Q.3 (c) Consider the sequential circuit given below:



(i) Find the count sequence of the circuit given above. Assume initial condition of flip-flop to be zero.

(ii) If clock frequency is 160 kHz. Find the frequencies of Q_0 and Q_2.

(iii) Sketch the waveforms of clock, Q_0, Q_1, Q_2 and Q_3.

[8 + 4 + 8 marks]

(1) Initial count = $Q_3\ Q_2\ Q_1\ Q_0$
$\quad\quad 0\ \ 0\ \ 0\ \ 0$

(i)

$Q_0 \Big|_0 \xrightarrow{\text{toggles}} 1$

Q0

Q1 – remain in previous state = Q1 = 0

Q2 = also " " " " Q2 = 0

Q3 = 0

4

Q0 ~~toggles~~ — 1 → 0

Q0 → Q1 – will toggle 0 → 1.

Q1 → Q2 – will toggle 0 → 1

Q2 → Q3 – will also toggle → 1 0

Q.4 (a) **(i)** Explain how linear convolution is performed using DFT. Find the linear convolution of $x[n] = \{1, 1, 1\}$ and $h[n] = \{1, 1\}$ using DFT.

(ii) Derive the relationship between discrete Fourier series coefficients (C_k) and discrete Fourier Transform $X(k)$ of a signal $x[n]$.

[15 + 5 marks]

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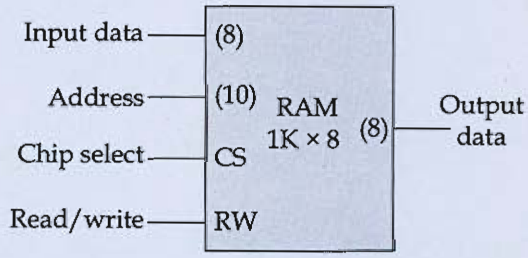
Q.4 (b) **(i)** Implement the logic function $F(A, B, C, D) = \Sigma m(0, 1, 2, 3, 4, 7, 9, 10)$ using 4 : 1 MUX only. (Assume only inputs are available)

(ii) Construct a 4 K × 8 RAM with 1 K × 8 RAM chips. The 1 K × 8 RAM is as shown below:



[10 + 10 marks]

Q.4 (c) **(i)** Write an 8051 assembly language program for converting the packed BCD number stored at the location 9000H into its equivalent binary number and store the result at 9001H.

(ii) Write an 8086 assembly language program to find the sum $\sum_{i=1}^{10} i$ and store the result in accumulator.

[12 + 8 marks]

Section B : Digital Circuits + Signals and Systems + Microprocessors & Microcontroller

Q.5 (a) **(i)** Find the Laplace transform of the function

$f(t) = 2e^{-t}\cos 10t - t^4 + 6e^{-(t-10)}$ for $t > 0$

(ii) Find the Fourier transform for the following signal:

$$x(t) = \frac{\sin(2\pi t)}{\pi(t-1)}$$

[8 + 4 marks]

(1) $f(t) = 2e^{-t}\cos 10t - t^4 + 6e^{-(t-10)}$ $t>0$

(i) $\cos 10t \xrightarrow{LT} \dfrac{s}{s^2+10^2}$ $\sigma > 0$

(ii) $e^{-t}\cos 10t \xrightarrow{LT} \dfrac{s+1}{(s+1)^2+10^2}$ $\underline{\underline{\sigma > -1}}$

(iii) $\boxed{t^n \xrightarrow{LT} \frac{n!}{s^{n+1}} \quad t>0}$

$t^4 \xrightarrow{LT} \frac{4!}{s^5} \quad t>0 \qquad \underline{\underline{\sigma > 0}}$

Similarly $\quad e^{-t} \longrightarrow \frac{1}{s+1} \qquad \underline{\sigma > -1}$

8

$e^{-(t-10)} \longrightarrow \frac{1}{s+1} \cdot e^{-s10} \qquad \underline{\underline{\sigma > -1}}$

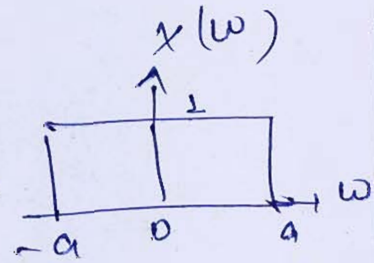
So combining all,

$$F(s) = \frac{s+1}{(s+1)^2+10^2} - \frac{4!}{s^5} + \frac{6e^{-10s}}{s+1} \qquad \underline{\sigma > 0.}$$

---

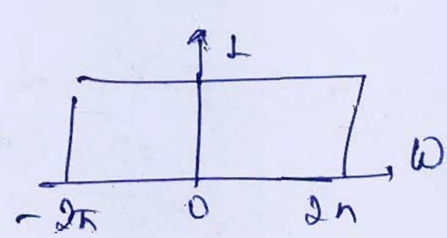
(11) $x(t) = \dfrac{\sin 2\pi t}{\pi(t-1)}$

We know $\dfrac{\sin at}{\pi t} \xrightarrow{FT}$



$\Rightarrow \dfrac{\sin a(t-1)}{\pi(t-1)} \xrightarrow{FT} e^{-j\omega} X(\omega)$

$\Rightarrow \dfrac{\sin 2\pi(t-1)}{\pi(t-1)} \xrightarrow{FT} e^{-j\omega} X(\omega)$

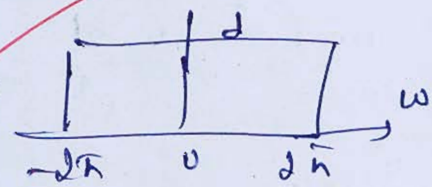


0 when $X(\omega) =$

$\Rightarrow \dfrac{\sin 2\pi t \cdot \cos 2\pi - \cancel{\sin 2\pi} \cos 2\pi t}{\pi(t-1)}$

$$\frac{\sin 2\pi t}{\pi(t-1)} \xleftrightarrow{FT} \underline{e^{-j\omega}\, X(\omega)}$$

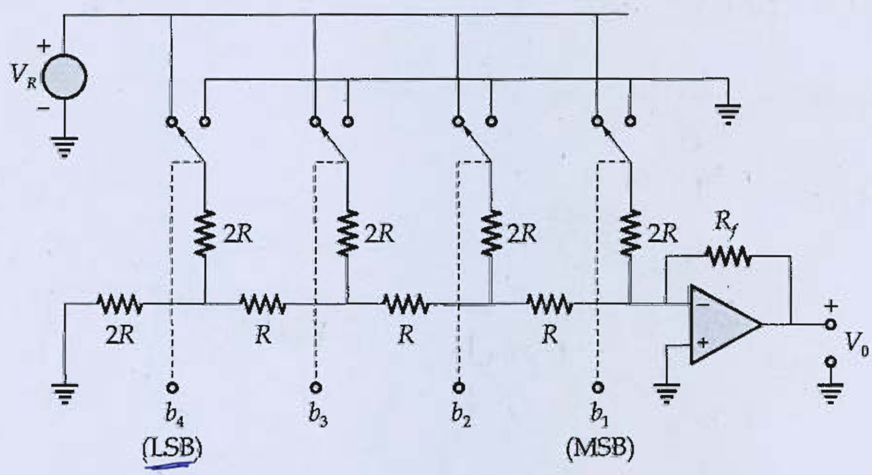
where $X(\omega)$



$$\frac{\sin 2\pi t}{\pi(t-1)} \xleftrightarrow{FT} e^{-j\omega}\, \text{rect}(\omega/4\pi)$$

6

Q.5 (b) Consider the R-$2R$, 4-bit converter shown below,



Assume the feedback resistance R_f of the op-amp is variable, the resistance $R = 5\ \text{k}\Omega$ and $V_R = 10$ V. Determine the value of R_f that should be connected to achieve the following output conditions:

(i) The value of 1 LSB at the output is 1 V.

(ii) An analog output of 8 V for a binary input of 1000.

(iii) The actual maximum output voltage of 10 V.

[12 marks]

$$V_0 = \frac{V_r}{2^n}\sum_{i=0}^{3} 2^i b_i \times \text{gain}$$

where $\boxed{\text{gain} = -\frac{R_f}{R}}$

(i)

(ii) $8 = \frac{10}{2^4} \times (8) \times \text{gain}$

$8 = \frac{\cancel{10}^{5}}{\cancel{16}_{\cancel{8}}} \times \cancel{8} \times \left(-\frac{R_f}{R}\right)$

$= \left|\frac{-R_f}{R}\right| = 8/5 \Rightarrow R = 5k$

$\underline{\underline{R_f = 8k}}$

4

(iii) The actual max. o/p $= 10V$

$10 = \frac{10}{2^4} \times \sum_{i=1}^{3} 2^i b_i \times \text{gain}$

= for max

$\Rightarrow$ 1111 → should be applied @ input

$\cancel{10} \Rightarrow \frac{\cancel{10}}{16} \times 15 \times \left(\frac{-R_f}{R}\right)$

$\boxed{\left|\frac{16}{15}\right| = \left|\frac{-R_f}{R}\right|}$

4

$R = \underline{\underline{5K}}$

$R_f = \frac{16}{\cancel{15}\,3} \times \cancel{5}$

$= \boxed{\frac{16}{3} \, k\Omega}$

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Q.5 (c) Compute and plot the convolution $y[n] = x[n] * h[n]$ using time domain approach where $x[n] = \left(\frac{1}{2}\right)^{(-n-1)} u[-n-1]$ and $h[n] = u[n-1]$.

[12 marks]

$x(n)\ \left(\frac{1}{2}\right)^{-n-1} u(-n-1) \qquad h(n) = u(n-1)$

$y(n) = x(n) * h(n)$

$$y(n) = \sum_{k=-\infty}^{\infty} h(k)\, x(-k+n)$$

$h(k) = u(k-1)$

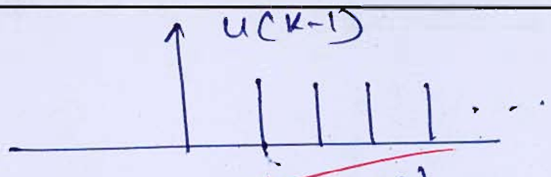
$x(n-k) = \left(1/2\right)^{(-(n-k)-1)} \quad u(-(n-k)-1)$

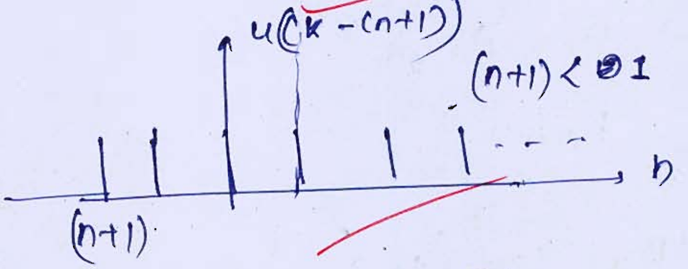
$= \left(\frac{1}{2}\right)^{-n+k-1} \quad u(-n+k-1)$

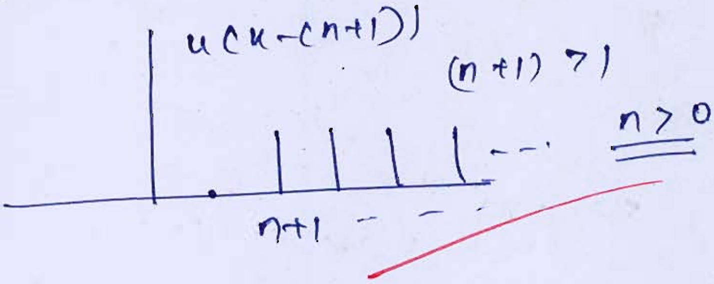
$= \left(\frac{1}{2}\right)^{k-n-1} \quad u(k-(n+1))$

$$y(n) = \sum_{k=-\infty}^{\infty} \left(\frac{1}{2}\right)^{-n-1} \left(\frac{1}{2}\right)^{k} u(k-1) \cdot u(k-(n+1))$$

$$= \left(\frac{1}{2}\right)^{-(n+1)} \sum_{k=-\infty}^{\infty} \left(\frac{1}{2}\right)^{k} u(k-1)\ u(k-(n+1))$$







$$y(n) = \begin{cases} \left(\frac{1}{2}\right)^{-(n+1)} \sum_{k=1}^{\infty} \left(\frac{1}{2}\right)^k & ; n < 0 \\ \left(\frac{1}{2}\right)^{-(n+1)} \sum_{k=n+1}^{\infty} \left(\frac{1}{2}\right)^k & ; n > 0 \end{cases}$$

10

for $n < 0$

$$y(n) \quad (2)^{n+1} \sum_{k \geq 1}^{\infty} (1/2)^k$$

$$y(n) = (1/2)^{-(n+1)} \times \frac{1/2}{1 - 1/2}$$

$$= (2)^{n+1} \times \frac{1/2}{1/2}$$

$$= \underline{\underline{2^{n+1}}}$$

for $\underline{n>0}$

$$y(n) = (2)^{n+1} \sum_{k=n+1}^{\infty} (1/2)^k$$

$$(2)^{n+1} \left(\frac{(1/2)^{n+1}}{1 - 1/2} \right.$$

$$\Rightarrow (2)^{n+1} \times 2 \times \left(\frac{1}{2}\right)^{n+1}$$

$$= 2^{n+2} \cdot 2^{-n-1}.$$

$$= 2^{-\cancel{n}+\cancel{n}+2-1}$$

$$= \underline{2.}$$

$$y(n) = \begin{cases} 2^{n+1} & ; n<0 \\ 2 & ; \underline{n>0} \end{cases}$$

2

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5 (d) Explain the function of following pins of 8086 microprocessor:

1. $\overline{BHE}/S7$
2. $MN/\overline{MX}$
3. $\overline{TEST}$
4. READY
5. RESET
6. INTR

[12 marks]

4. READY :- READY pin is used to check the the status of interrupt pin.
If the peripheral is set to, give interrupts than READY pin becomes high else low.

5. RESET : It is used to reset the entire microprocessor content,
i.e., if PC is executing some instruction ~~hold by~~ holding the address, will now show any Random value.

6 INTR

Q.5 (e) Consider a three input Boolean function $f(a, b, c) = \Sigma m(0, 1, 2, 3, 7)$

(i) Implement the function using a minimal network of 2 × 4 decoder and OR gates.

(ii) Implement the function using a minimal network of 4 × 1 multiplexers.

(iii) Implement the function using a minimal network of 2 × 1 multiplexers.

[4 + 4 + 4 marks]

(1)

a \ bc	00	01	11	10
0	1	1	1	1
1	0	0	1	0

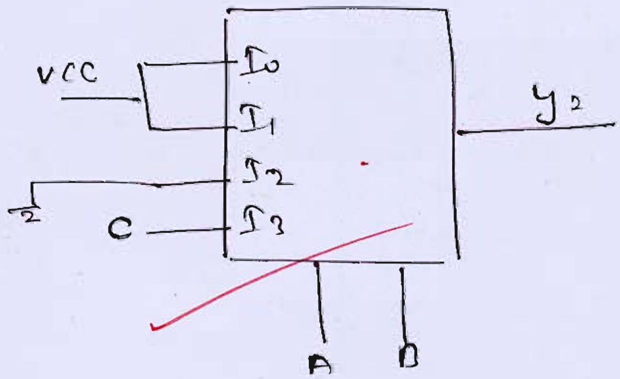
$f = \bar{a} + bc$

(ii) using 4:1 mux.

$f(a,b,c) = \Sigma m(0,1,2,3,7)$

now taking ab as a select line and c - as input

	I_0	I_1	I_2	I_3
$\bar{c}$	0	2	4	6
c	1	3	5	7
	1	1	0	c



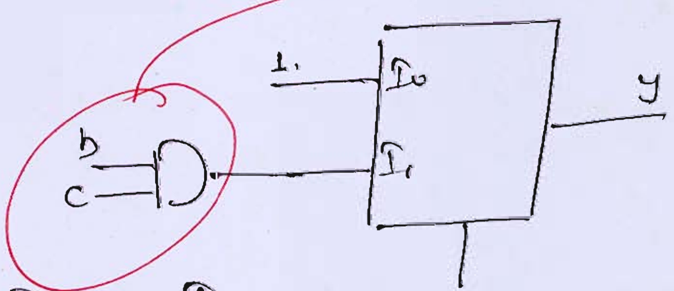
4

(iii)

$f_2 \; \bar{a} + bc$

taking a as a select line

design AND gate with 2X1 MUX.



$y = \bar{a} + abc$

for a = 1

$y_2 \; bc$

I_0	I_1
$\bar{a}$ bc	abc
0 0 0	1 0 0
0 0 1	1 0 1
0 1 0	1 1 0
0 1 1	1 1 1
1	bc

3

Q.6 (a) (i) Write an 8086 assembly language program to add the two BCD data 29H and 98 H and store the result in BCD form in the memory locations 2000 H : 3000 H and 2000 H : 3001 H.

(ii) Explain the series of steps performed by 8086 microprocessor during processing of an interrupt request.

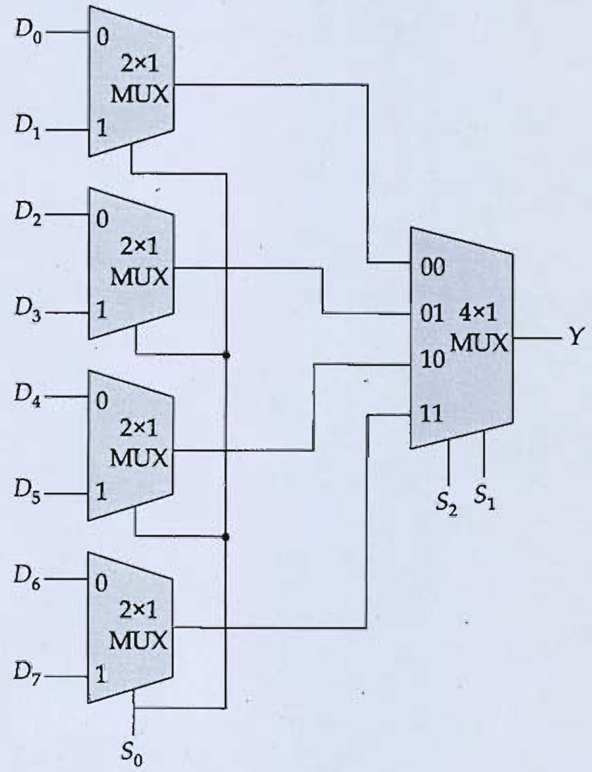
[10 + 10 marks]

Q.6 (b) **(i)** Minimize the SOP terms given for a Boolean function,

$f(A, B, C, D) = \Sigma m(2, 3, 8, 10, 11, 12, 14, 15)$

Implement the minimized function using NAND gates alone.

(ii) Determine the logic equation for the output by constructing the truth table for the logic circuit shown in figure below:



[12 + 8 marks]

(1) $f(A,B,C,D) = \sum m(2,3,8,10,11,12,14,15)$

AB \ CD	00	01	11	10
00	0	0	1	1
01	0	0	0	0
11	1	0	1	1
10	1	0	1	1

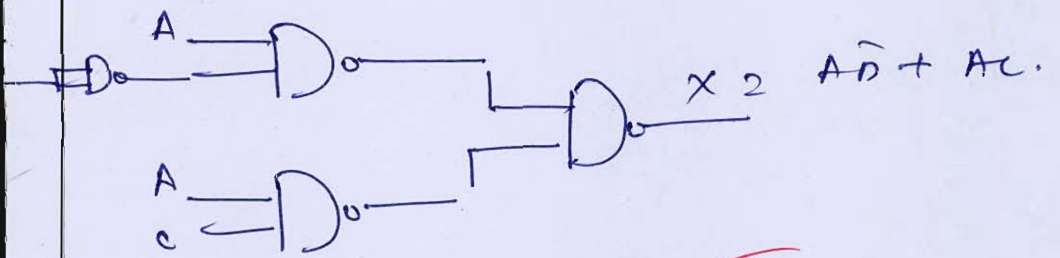
10

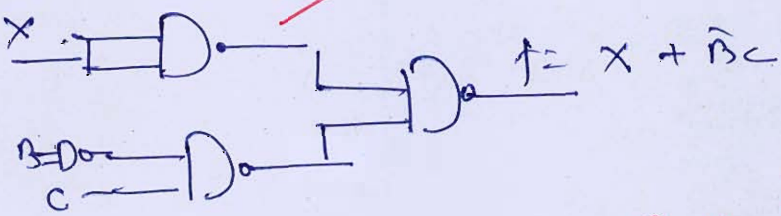
$f = A\bar{D} + AC + \bar{B}C$

$f = A\bar{D} + AC + \bar{B}C$

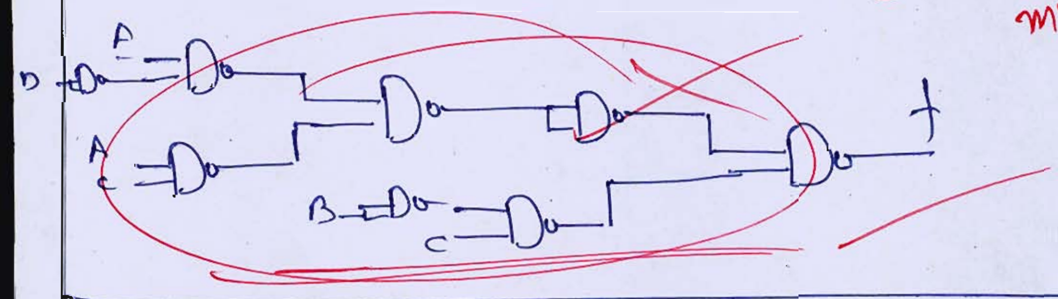
now consider $\underline{A\bar{D} + AC \Rightarrow X}$

$\underline{f = X + \bar{B}C}$





Can be used minimal.



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(11)

$Y =$

S_2 S_1 S_0	Y
0 0 0	$y = D0$
0 0 1	$y = D1$
0 1 0	D2
0 1 1	D3
1 0 0	D4
1 0 1	D5
1 1 0	D6
1 1 1	D7

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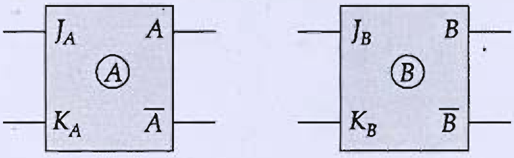
$y = \bar{S_2}\bar{S_1}\bar{S_0}D0 + \bar{S_2}\bar{S_1}S_0 D1 + \bar{S_2}S_1\bar{S_0}D2 + \bar{S_2}S_1S_0D3$

$+ S_2\bar{S_1}\bar{S_0}D4 + S_2\bar{S_1}S_0D5 + S_2S_1\bar{S_0}D6 + S_2S_1S_0D7$

6

5 (c) A sequential circuit has two J-K flip flops A and B as shown below, two inputs x and y, and one output Z. The flip flop input equations and circuit output equation are



$J_A = Bx + \overline{B}\overline{y}$; $K_A = \overline{B}x\overline{y}$

$J_B = \overline{A}x$; $K_B = A + x\overline{y}$

$Z = A\overline{x}\,\overline{y} + B\overline{x}\,\overline{y}$

(i) Draw the logic diagram of the circuit.

(ii) Tabulate the state table.

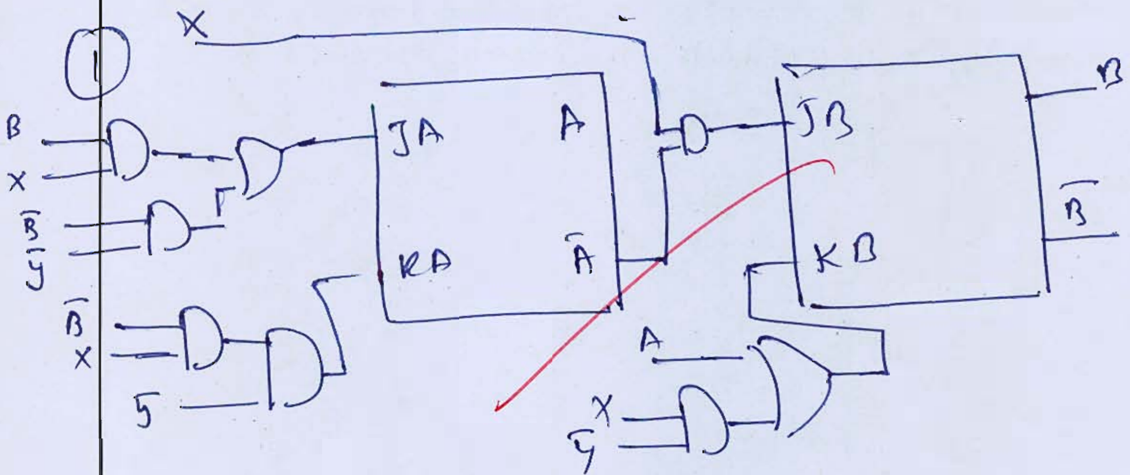
(iii) Derive the state equations for A and B.

[20 marks]

(ii)

Present state		Input		JA	KA	JB	KB	Next state		Z
A	B	x	y					A+	B+	
0	0	0	0	1	0	0	0	1	0	
0	0	0	1	0	0	0	0	0	0	
0	0	1	0	1	1	1	1	1	1	
0	0	1	1	0	0	1	0	0	1	
0	1	0	0	0	0	0	0	0	1	
0	1	0	1	0	0	0	0	0	1	
0	1	1	0	1	0	1	1	1	0	
0	1	1	1	1	0	1	0	1	1	
1	0	0	0	1	0	0	~~0~~1	1	0	
1	0	0	1	0	0	0	1	1	0	
1	0	1	0	1	1	0	1	0	0	
1	0	1	1	1	0	0	1	1	0	
1	1	0	0	0	0	0	1	1	0	
1	1	0	1	0	0	0	1	1	0	
1	1	1	0	1	0	0	1	1	0	
1	1	1	1	1	0	0	1	1	0	

(i)



(iv)

$A^+ =$

AB \ xy	00	01	11	10
00	1	0	0	1
01	0	0	1	1
11	1	1	1	1
10	1	1	1	0

$f(A^+) = AB + Ay + Bx + \bar{A}x\bar{y} + \bar{B}\bar{x}\bar{y}$

$B^+ =$

AB \ xy	00	01	11	10
00	0	0	1	1
01	1	1	1	0
11	0	0	0	0
10	0	0	0	0

20

$f(B^+) = \bar{A}\bar{B}x + \bar{A}B\bar{x} + \bar{A}xy$

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Q.7 (a) **(i)** With a neat block diagram, explain the operation of counter type *ADC*. Give advantages and disadvantages of counter type *ADC*.

(ii) Define fan-out of a gate. A two-input NAND gate specifications are given as
$I_{OH(\text{max})} = 0.4$ mA, $V_{OH(\text{min})} = 2.7$ V, $V_{IH(\text{min})} = 2$ V,
$V_{IL(\text{max})} = 0.8$ V, $V_{OL(\text{max})} = 0.4$ V, $I_{OL(\text{max})} = 8$ mA,
$I_{IL(\text{max})} = 0.4$ mA, $I_{IH(\text{max})} = 25$ μA, $t_{\text{PLH}} = t_{\text{PHL}} = 15$ nsec
and supply voltage of 5 V. Determine

1. High state noise margin.
2. Low state noise margin.
3. Number of NAND gate inputs that can be driven from the output of a NAND gate of this type.

[12 + 8 marks]

Q.7 (b) Each of the following arithmetic operation is correct in atleast one number system. Determine the possible bases in each operation.

(i) $3441 + 4235 = 7676$

(ii) $\frac{142}{7} = 16$

(iii) $23 + 44 + 14 + 32 = 223$

(iv) $21 \times 16 = 366$

(v) $\frac{302}{20} = 12.1$

(vi) $\sqrt{51} = 6$

[20 marks]

c) (i) Consider a discrete-time low-pass filter whose impulse response $h[n]$ is known to be real and whose frequency response magnitude in the region $-\pi \le \omega \le \pi$ is given as,

$$\left|H\left(e^{jw}\right)\right| = \begin{cases} 1; & |\omega| \le \dfrac{\pi}{3} \\ 0; & \text{otherwise} \end{cases}$$

Determine the real-valued impulse response $h[n]$ for this filter when the corresponding group-delay function is $\tau_g(\omega) = \dfrac{3}{2}$.

(ii) Design a block level architecture of a 5 coefficient FIR filter by using appropriate number of multipliers, adders and registers. Assume that all the input operands are available in 4 bit, 2's complement fixed point representation. The architecture should give one output per clock cycle.

[10 + 10 marks]

Q.8 (a) (i) Draw the block diagram of programmable peripheral interface 8255A.

(ii) Explain BSR (Bit Set/Reset) mode of 8255A

(iii) Write a BSR control word subroutine to set bits PC_7 and PC_3 and reset them after some delay, using the below I/O port addresses.

$\overline{CS}$								Hexadecimal Address	Port
A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
1	0	0	0	0	0	0	0	= 80H	A
1	0	0	0	0	0	0	1	= 81H	B
1	0	0	0	0	0	1	0	= 82H	C
1	0	0	0	0	0	1	1	= 83H	Control Register

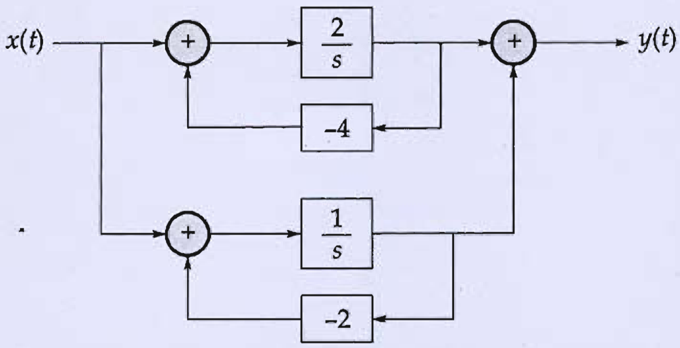
[20 marks]

b) **(i)** Suppose we are given the following information about a continuous time periodic signal $x(t)$ with period 3 and Fourier series coefficients a_k:

1. $a_k = a_{k+2}$
2. $a_k = a_{-k}$
3. $\int_{-0.5}^{0.5} x(t)dt = 1$
4. $\int_{0.5}^{1.5} x(t)dt = 2$

Determine $x(t)$.

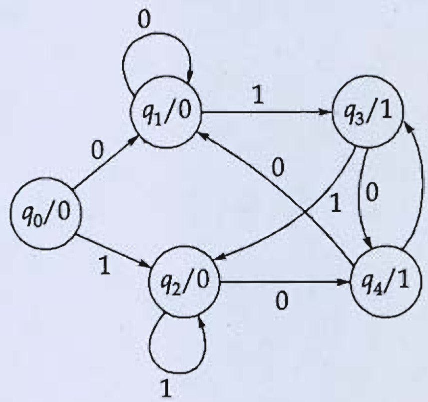
(ii) A causal LTI system 'S' has the block diagram representation as shown in figure below.



Determine a differential equation relating the input $x(t)$ to the output $y(t)$ of this system.

[10 + 10 marks]

Q.8 (c) Consider the state diagram of Moore machine shown below:



Get the excitation equations and Boolean equations for output Z of Mealy machine. Also design the Mealy machine using J-K flip-flop.

[20 marks]

OOOO

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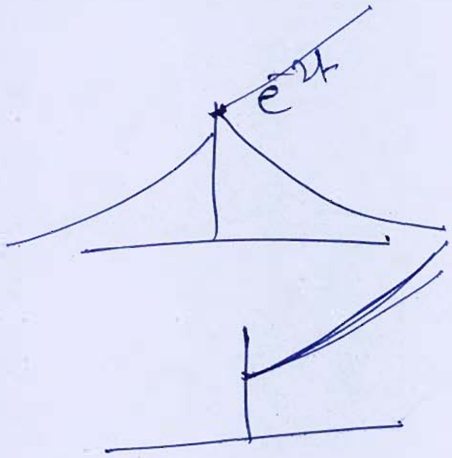
Space for Rough Work



D_0	D_1
0	1
2	3

$\bar{a}$	B	C	a	B	C
0	0	0	1	0	0
0	0	1	1	0	1
0	1	0	1	1	0
0	1	1	1	1	1

I_1 AC

sin cat

sin(at − a)

sin (a−b)

sin a cos b − sin b cos a

sin 2πt · cos(2π a) − ~~sin at~~ cos(2πt)

sin 2πt · cos 2a

$(\bar{a}+b)(\bar{a}+c)$

Space for Rough Work

Space for Rough Work

Space for Rough Work