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ESE 2025 : Mains Test Series

UPSC ENGINEERING SERVICES EXAMINATION

Electronics & Telecommunication Engineering

Test-2 : Digital Circuits + Signals and Systems + Microprocessors & Microcontroller [All topics]

Name : ....

Roll No :

Test Centres				Student's Signature
Delhi ☐	Bhopal ☐	Jaipur ☐	Pune ☐	
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Instructions for Candidates

1. Do furnish the appropriate details in the answer sheet (viz. Name & Roll No).
2. There are Eight questions divided in TWO sections.
3. Candidate has to attempt FIVE questions in all in English only.
4. Question no. 1 and 5 are compulsory and out of the remaining THREE are to be attempted choosing at least ONE question from each section.
5. Use only black/blue pen.
6. The space limit for every part of the question is specified in this Question Cum Answer Booklet. Candidate should write the answer in the space provided.
7. Any page or portion of the page left blank in the Question Cum Answer Booklet must be clearly struck off.
8. There are few rough work sheets at the end of this booklet. Strike off these pages after completion of the examination.

FOR OFFICE USE

Question No.	Marks Obtained
Section-A	
Q.1	36
Q.2	39
Q.3	/
Q.4	/
Section-B	
Q.5	41
Q.6	44
Q.7	30
Q.8	/
Total Marks Obtained	190

Signature of Evaluator: Ch. Raj (?) .... Cross Checked by ....

• Can do better.

IMPORTANT INSTRUCTIONS

CANDIDATES SHOULD READ THE UNDERMENTIONED INSTRUCTIONS CAREFULLY. VIOLATION OF ANY OF THE INSTRUCTIONS MAY LEAD TO PENALTY.

DONT'S

1. Do not write your name or registration number anywhere inside this Question-cum-Answer Booklet (QCAB).
2. Do not write anything other than the actual answers to the questions anywhere inside your QCAB.
3. Do not tear off any leaves from your QCAB, if you find any page missing do not fail to notify the supervisor/invigilator.
4. Do not leave behind your QCAB on your table unattended, it should be handed over to the invigilator after conclusion of the exam.

DO'S

1. Read the Instructions on the cover page and strictly follow them.
2. Write your registration number and other particulars, in the space provided on the cover of QCAB.
3. Write legibly and neatly.
4. For rough notes or calculation, the last two blank pages of this booklet should be used. The rough notes should be crossed through afterwards.
5. If you wish to cancel any work, draw your pen through it or write "Cancelled" across it, otherwise it may be evaluated.
6. Handover your QCAB personally to the invigilator before leaving the examination hall.

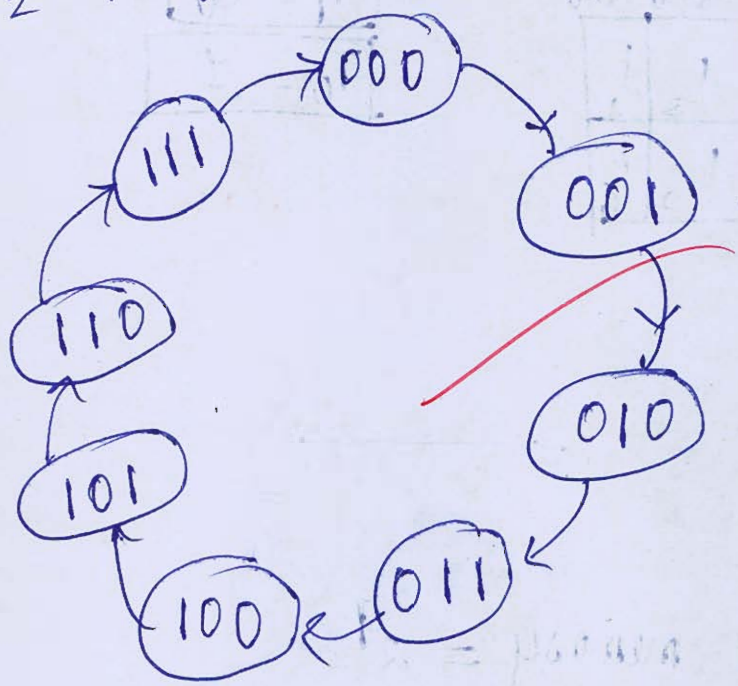
Section A : Digital Circuits + Signals and Systems + Microprocessors & Microcontroller

Q.1 (a) Design a 3-bit binary counter using T-flip-flops.

[12 marks]

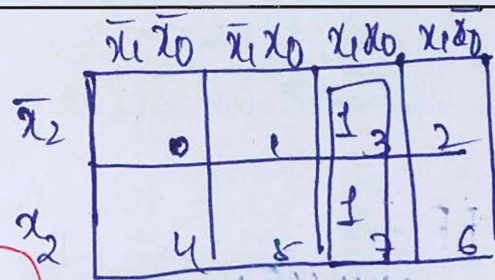
Solu:- 3-bit binary counter using T FF:-

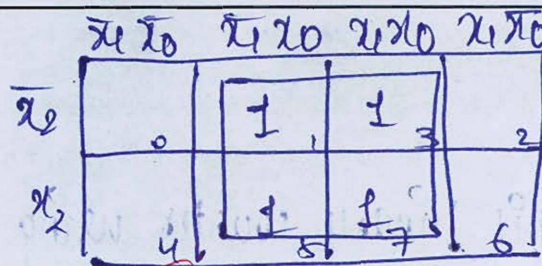
X_2 X_1 X_0 be the counter sequences:

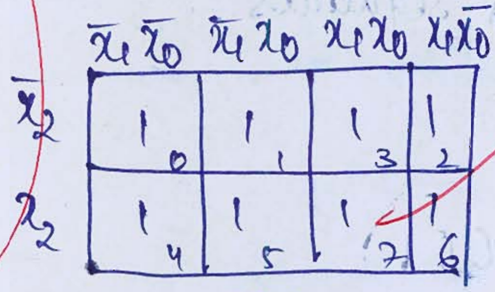


Q	Q^+	T
0	0	0
0	1	1
1	0	1
1	1	0

	X_2	X_1	X_0	X_2^+	X_1^+	X_0^+	T_2	T_1	T_0
0	0	0	0	0	0	1	0	0	1
1	0	0	1	0	1	0	0	1	1
2	0	1	0	0	1	1	0	0	1
3	0	1	1	1	0	0	1	1	1
4	1	0	0	1	0	1	0	0	1
5	1	0	1	1	1	0	0	1	1
6	1	1	0	1	1	1	0	0	1
7	1	1	1	0	0	0	1	1	1







$T_1 = x_0$

$T_0 = 1$

$T_2 = x_1 x_0$

10

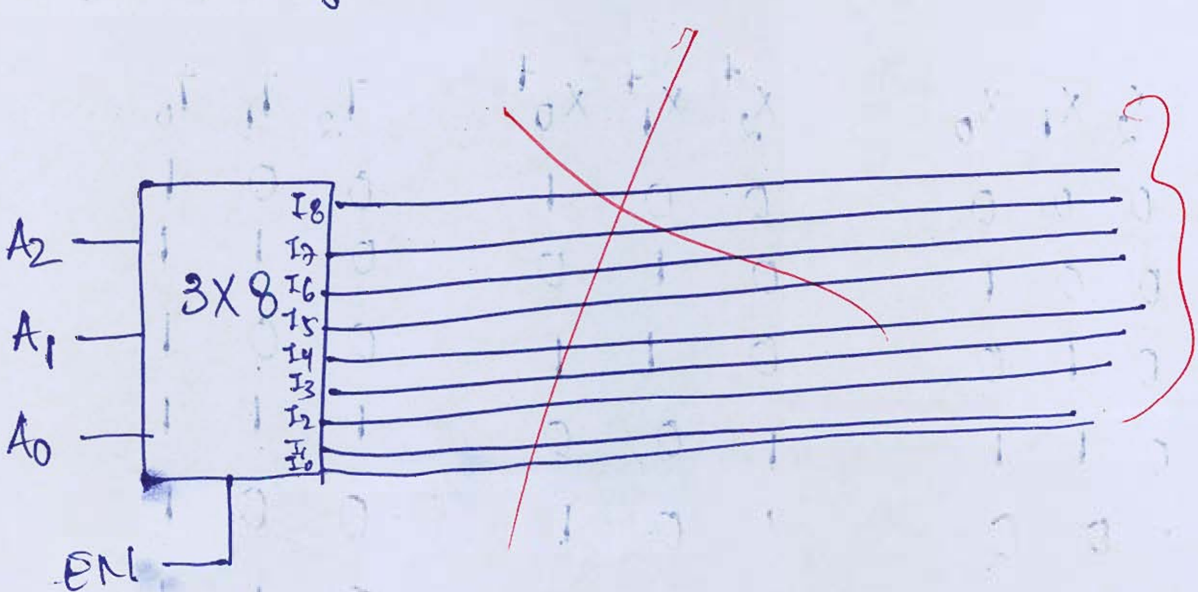
logic diagram.

Q.1 (b) (i) Draw the circuit for interfacing 512 bytes of memory to 8085 microprocessor using 3 × 8 decoder.

(ii) Write an assembly language program to move a block of Data of 16 bytes starting from address 2050H to another location starting from 2070H in 8085 microprocessor.

[7 + 5 marks]

Soln: i) 512 Bytes of memory $= 2^9$



(b) (ii)

```
MOV C, (16)H
MOV H, 20
MOV L, 50
INC H
INC L
DEC C
MOV D, H
MOV E, L
HLT
```

Starting

20	50
H	L

20	70
D	E

5

Do not write in this margin

Q.1 (c) (i) Draw the signal flow graph (Butterfly structure) for the computation of 8-point IDFT using inverse Radix-2 DIF-FFT.

(ii) State and prove Initial-value theorem of z-transform.

[8 + 4 marks]

Soln: Intial value theorem of z transform

$$x(n)\Big|_{n\to\infty} = \underset{z\to 0}{Lt}\ X(z)$$

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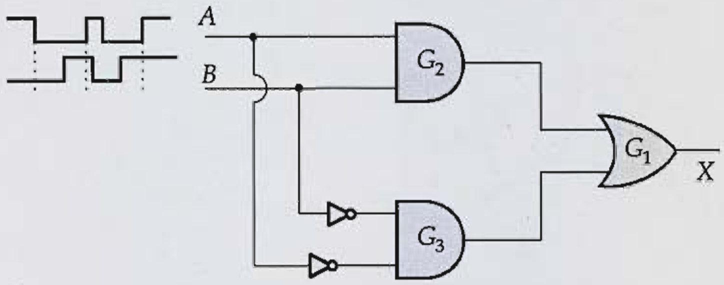
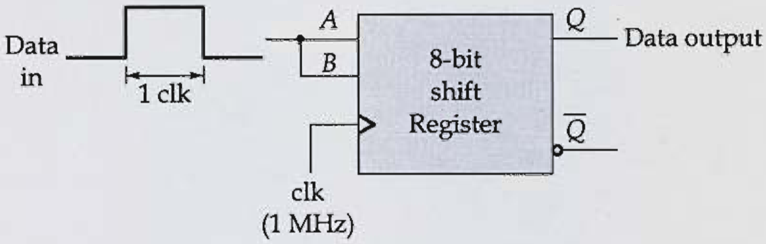
Q.1 (d) (i) Draw the timing diagram for the logic circuit in the figure shown with outputs of G_1, G_2 and G_3 with input waveform A and B as indicated.



(ii) Consider the serial in-serial out shift register which is used to provide time delay from input to output.



Draw and calculate the output and delay provided by the above shift register in clear steps.

[6 + 6 marks]

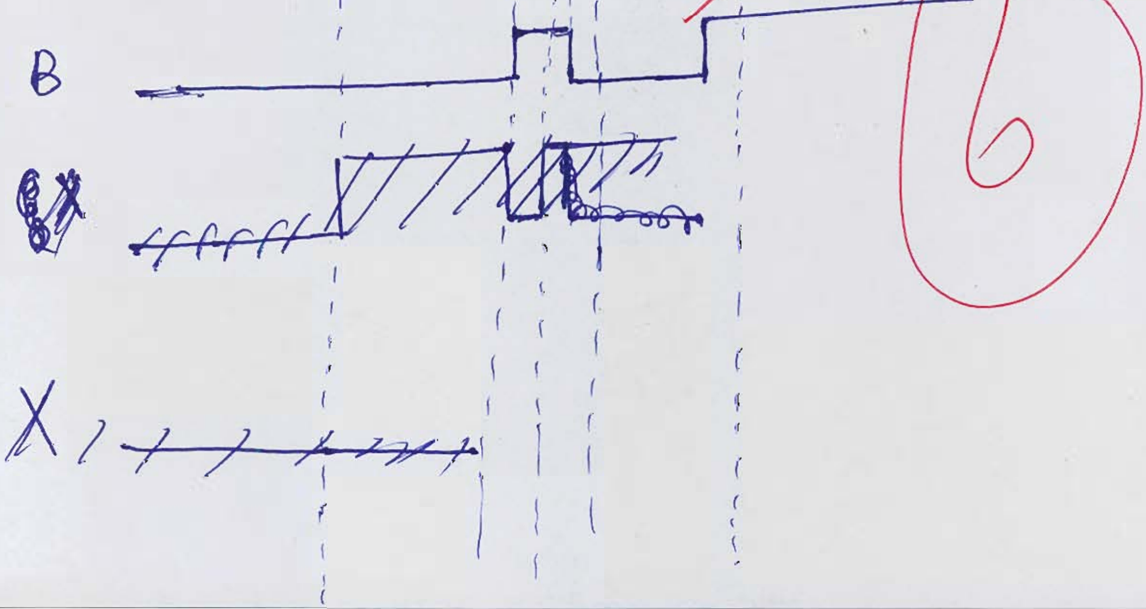
Soln: (i) (i)

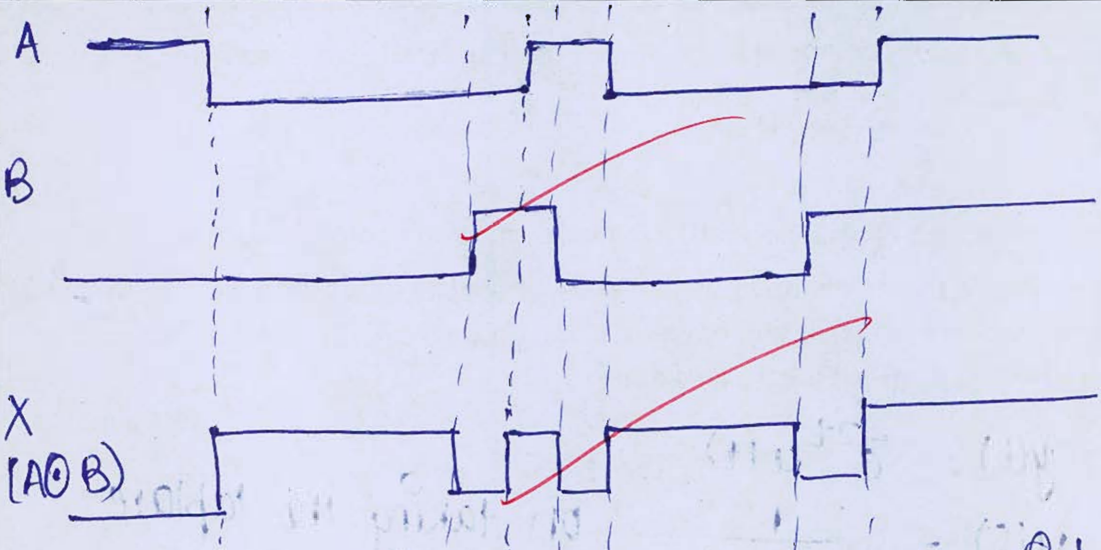
$G_2 = A \cdot B$

$G_3 = \bar{A}\bar{B}$

$G_1 = G_3 + G_2 = A \cdot B + \bar{A}\bar{B} = A \odot B = X$

$\therefore X = A \odot B$

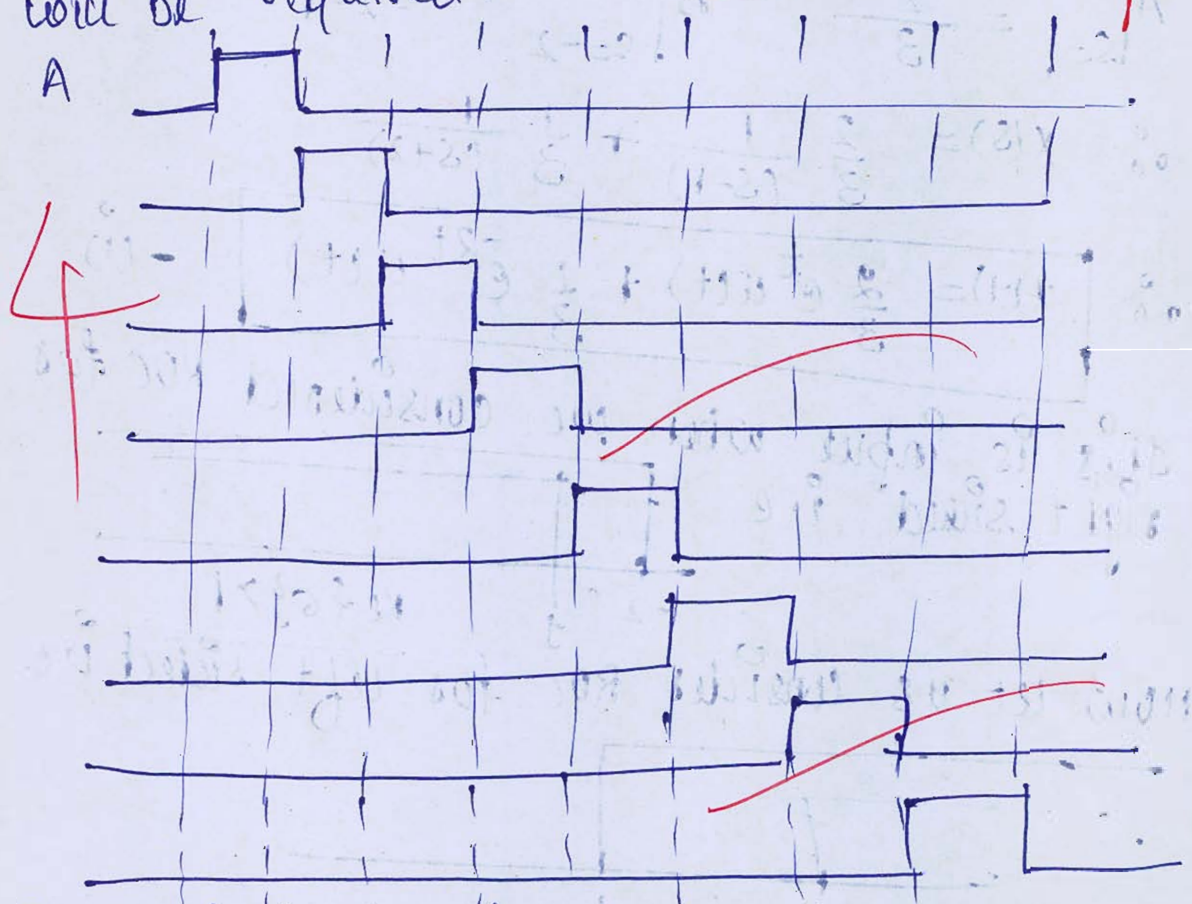




(d) (iii) For an 8 bit shift register, for input n number of clock pulses are required and at output (n-1) clock pulses are required.

∴ at input 8 clock pulses will be required and at output 7 clock pulses will be required.

8 clock pulse



Delay of 7 µsec will be there.

Q.1 (e) Consider the signal $y(t) = e^{-2t}u(t)$ is the output of a causal all-pass system for which the system function is

$$H(s) = \frac{s-1}{s+1}$$

(i) Find and sketch at least two possible inputs $x(t)$ that could produce $y(t)$.

(ii) From the solutions obtained in part (i), what is the input $x(t)$ if it known that a stable system exists that will have $x(t)$ as an output and $y(t)$ as the input? Find the impulse response $h(t)$ for this system.

[6 + 6 marks]

Solu:- (i)

$y(t) = e^{-2t}u(t)$

$Y(s) = \frac{1}{(s+2)}$ on taking the laplace transform.

$H(s) = \frac{s-1}{s+1}$

$Y(s) = X(s) \cdot H(s)$

$\frac{1}{s+2} = \frac{s-1}{s+1} \cdot X(s)$

$X(s) = \frac{s+1}{(s-1)(s+2)} = \frac{A}{(s-1)} + \frac{B}{s+2}$

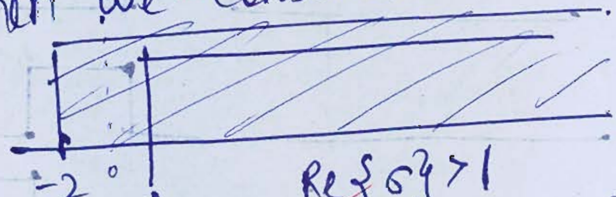
$A\Big|_{s=1} = \frac{2}{3}$ $\quad B\Big|_{s=-2} = \frac{-2+1}{-2-1} = \frac{-1}{-3} = \frac{1}{3}$

6

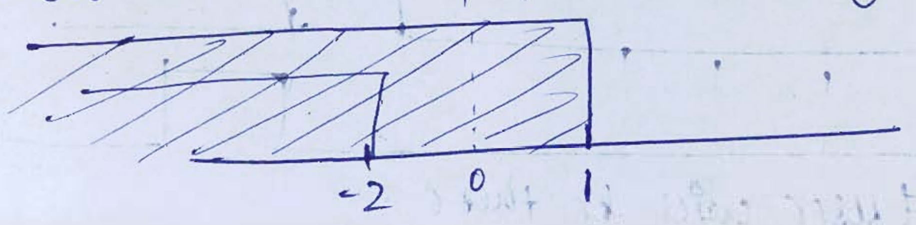
$\therefore X(s) = \frac{2}{3}\frac{1}{(s-1)} + \frac{1}{3}\frac{1}{(s+2)}$

$\therefore$ $x(t) = \frac{2}{3}e^{t}u(t) + \frac{1}{3}e^{-2t}u(t)$ — (1)

this is input when we considered ROC for right sided i.e



Now let us consider ROC for left sided i.e



$\therefore\ x(s) = \frac{2}{3}\frac{1}{(s-1)} + \frac{1}{3}\frac{1}{(s+2)}$

$\therefore\ \boxed{x(t) = -\frac{2}{3}e^{t}u(-t) + \frac{1}{3}(-1)e^{-2t}u(-t)}$ — (ii)

(i) & (ii) represents two possible input x(t) that could produce y(t).

(e)(ii) since we know for system to be stable it should have jω axis included. so in equation (i) & (ii) jω axis is considered.

we can choose any one solution.

let $\quad y(s) = \frac{s+1}{(s-1)(s+2)}$

& $\quad x(s) = \frac{1}{(s+2)}$

$\Rightarrow\quad y(s) = x(s)\cdot H(s)$

$\frac{s+1}{(s-1)(s+2)} = \frac{1}{(s+2)}\cdot H(s)$

$\therefore\ \frac{(s+1)(s+2)}{(s-1)(s+2)} = H(s)$

$\therefore\ H(s) = \left[\frac{s+1}{s-1}\right]$

$H(s) = \frac{s}{s-1} + \frac{1}{s-1} = \frac{2}{s-1} + 1$

$\therefore\ \boxed{h(t) = 2e^{t}u(t) + \delta(t)}$

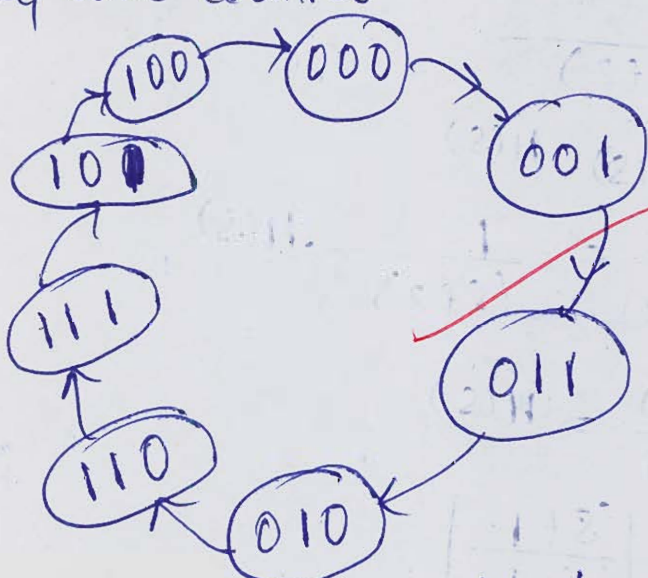
Q.2 (a) Implement the state diagram and sequential circuit diagram using JK flip-flops for 3-bit Gray code counter.

[20 marks]

Solu:- 3 bit Gray code counter:

	B_2	B_1	B_0	G_2	G_1	G_0
0	0	0	0	0	0	0
1	0	0	1	0	0	1
2	0	1	0	0	1	1
3	0	1	1	0	1	0
4	1	0	0	1	1	0
5	1	0	1	1	1	1
6	1	1	0	1	0	1
7	1	1	1	1	0	0

Gray code counter



Q	Q^+	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

	G_2	G_1	G_0	Q_2^+	Q_1^+	Q_0^+	J_2	K_2	J_1	K_1	J_0	K_0
0	0	0	0	0	0	1	0	X	0	X	1	X
1	0	0	1	0	1	1	0	X	1	X	X	0
3	0	1	1	0	1	0	0	X	X	0	X	1
2	0	1	0	1	1	0	1	X	X	0	0	X
6	1	1	0	1	1	1	X	0	X	0	1	X
7	1	1	1	1	0	1	X	0	X	1	X	0
5	1	0	1	1	0	0	X	0	0	X	X	1
4	1	0	0	0	0	0	X	1	0	X	0	X

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∴ J_2

	$\bar{Q}_1\bar{Q}_0$	$\bar{Q}_1 Q_0$	$Q_1 Q_0$	$Q_1\bar{Q}_0$
$\bar{Q}_2$	0	1	3	1 (2)
Q_2	X (4)	X (5)	X (7)	X (6)

$J_2 = Q_1\bar{Q}_0$

K_2

	X	X	X	X
	1			

$K_2 = \bar{Q}_1\bar{Q}_0$

J_1

		1	X	X
			X	X

$J_1 = \bar{Q}_2 Q_0$

K_1

	X	X		
	X	X		

$K_1 = Q_2 Q_0$

J_0

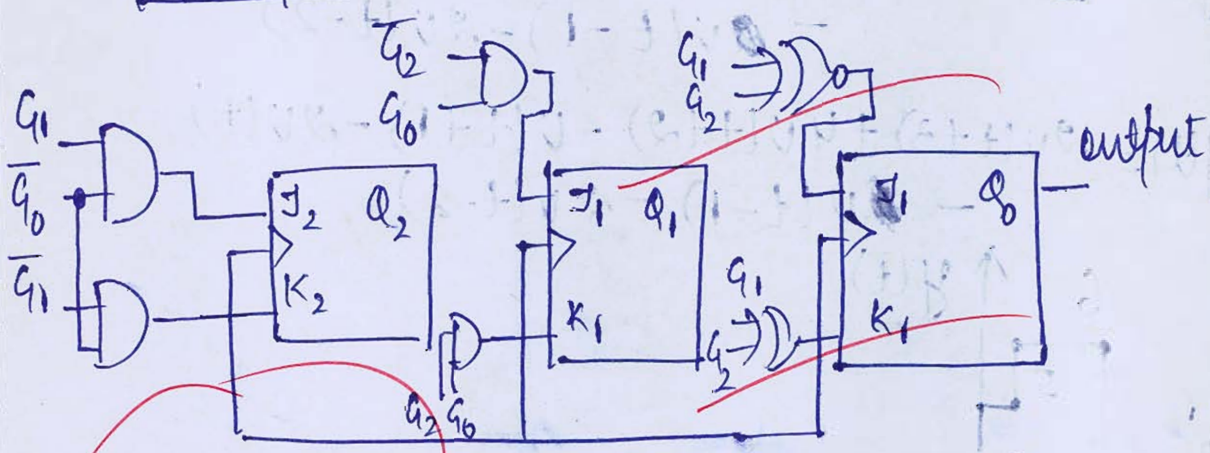
	1	X	X	
		X	X	1

$J_0 = \bar{Q}_2\bar{Q}_1 + Q_2 Q_1$

K_0

	X		1	X
	X	1		X

$K_0 = \bar{Q}_2 Q_1 + Q_2\bar{Q}_1$



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Q.2 (b) **(i)** Determine and sketch $y(t)$, the convolution of the two signals given below:

$$x(t) = \begin{cases} 2, & -1 \le t \le 1 \\ 1, & 1 < t \le 3 \\ 0, & \text{elsewhere} \end{cases}$$

and $h(t) = 2\delta(t+1) + \delta(t+2)$

(ii) The output $y(t)$ of a causal LTI system is related to the input $x(t)$ by the equation

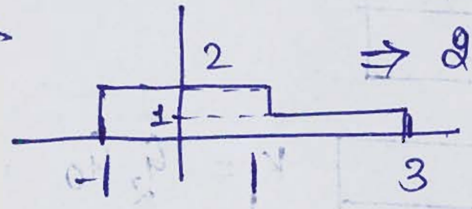
$$\frac{dy(t)}{dt} + 10y(t) = \int_{-\infty}^{\infty} x(\tau)z(t-\tau)d\tau - x(t)$$

where, $z(t) = e^{-t}u(t) + \delta(t)$

Determine the impulse response of the system.

[10 + 10 marks]

Soln. (i) $x(t) \leftrightarrow$



$\Rightarrow 2u(t+1) - u(t-1) - u(t-3)$

$h(t) \leftrightarrow 2\delta(t+1) + \delta(t+2)$

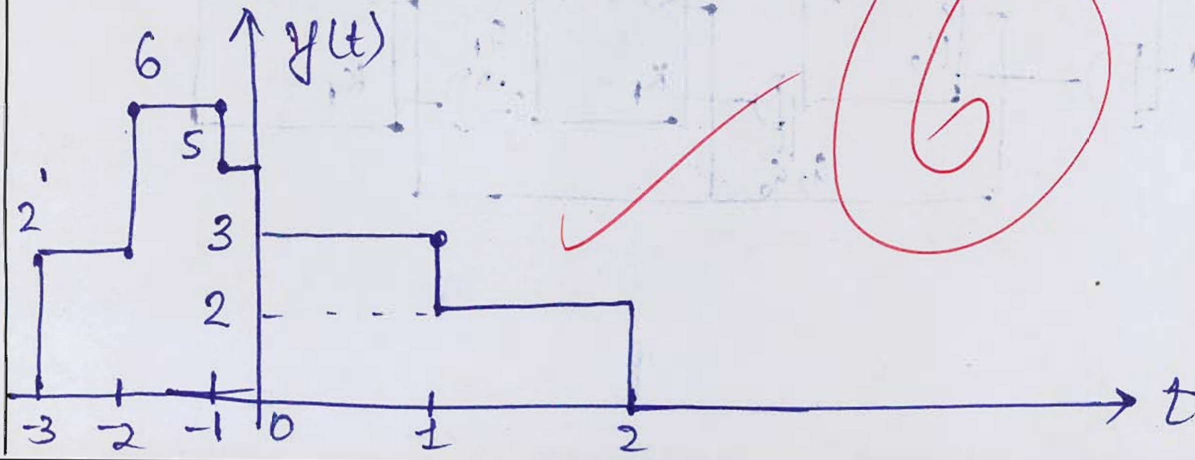
$\therefore y(t) = x(t) * h(t)$

$y(t) = [2u(t+1) - u(t-1) - u(t-3)] * [2\delta(t+1) + \delta(t+2)]$

$y(t) = 4u(t+2) + 2u(t+3) - 2u(t) - u(t+1) - 2u(t-2) - u(t-1)$

$y(t) = 2u(t+3) + 4u(t+2) - 2u(t) - u(t+1) - 2u(t-1) - 2u(t-2)$

$y(t) = 2u(t+3) + 4u(t+2) - u(t+1) - 2u(t) - 2u(t-1) - 2u(t-2)$



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(ii) $\frac{dy(t)}{dt} + 10y(t) = \int_{-\infty}^{\infty} x(\tau)\, x(t-\tau)\, d\tau - x(t)$

Soln:- $x(t) = e^{-t}u(t) + \delta(t)$

$h(t) = ?$

$\frac{dy(t)}{dt} + 10y(t) = x(t) * x(t) - x(t)$

on taking the laplace Transform, we get

$sY(s) + 10Y(s) = X(s) \cdot X(s) - X(s)$

$Y(s)[s+10] = X(s)[X(s) - 1]$

$\frac{Y(s)}{X(s)} = \frac{X(s) - 1}{(s+10)}$

$x(t) = e^{-t}u(t) + \delta(t)$

on taking laplace transform, we get

$X(s) = \frac{1}{(s+1)} + 1 = \frac{1 + (s+1)}{(s+1)} = \frac{s+2}{s+1}$

$\frac{Y(s)}{X(s)} = H(s) = \frac{\frac{s+2}{s+1} - 1}{(s+10)} = \frac{(s+2)-(s+1)}{(s+1)(s+10)}$

$H(s) = \frac{1}{(s+1)(s+10)} = \frac{A}{(s+1)} + \frac{B}{(s+10)}$

$A|_{s=-1} = \frac{1}{9}$ $\quad B|_{s=-10} = \frac{1}{-10+1} = \frac{-1}{9}$

$\therefore H(s) = \frac{1}{9}\frac{1}{(s+1)} - \frac{1}{9}\frac{1}{(s+10)}$

$h(t) = \frac{1}{9}e^{-t}u(t) - \frac{1}{9}e^{-10t}u(t)$ Ans.

10

Q.2 (c) (i) Interface 4 KB memory to 8085 with starting address A000H.
Design address decoding circuit using (i) 3 × 8 decoder and (ii) using only NAND gates.

(ii) Write an algorithm and assembly language program, to perform the multiplication of two 8 bit numbers using 8085.

[10 + 10 marks]

Soln: (i) $4KB = 2^2 \times 2^{10} = 2^{12}$

∴ There will be 12 address lines

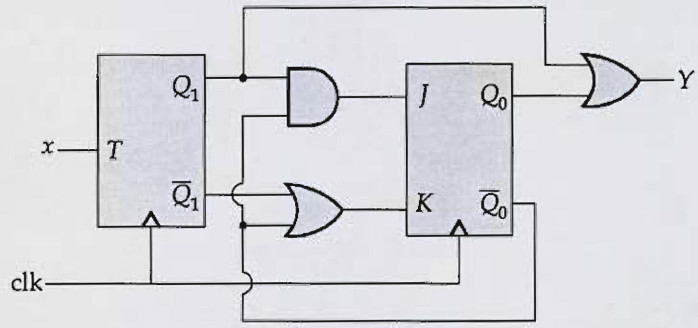
A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0
0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0
1	1	1	1	0	0	0	0	0	0	0	0	1	0	1	0

Starting Address + Ending Address − 1 = FFFF

Ending address = FFFF − A000H + 1

= 6000H

Q.3 (a) (i) Draw the state diagram of the sequential circuit shown in figure below:



(ii) Find the z-transform of the given signal $x[n]$ using scaling in the z-domain property.

$x[n] = a^n \sin(\omega_0 n)\, u[n]$.

[10 + 10 marks]

Q.3 (b) (i) Implement the following Boolean function using 3 × 4 × 2 PLA, also write the PLA programming table.

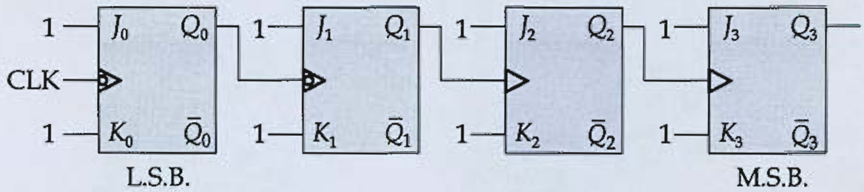
$F_1(A, B, C) = \Sigma m(0, 1, 2, 4)$

$F_2(A, B, C) = \Sigma m(0, 5, 6, 7)$

(ii) A 6-bit dual slope ADC uses a reference of 12 V and a fixed count of 010110. Convert the maximum input voltage accurately in digital form.

[15 + 5 marks]

Q.3 (c) Consider the sequential circuit given below:



(i) Find the count sequence of the circuit given above. Assume initial condition of flip-flop to be zero.

(ii) If clock frequency is 160 kHz. Find the frequencies of Q_0 and Q_2.

(iii) Sketch the waveforms of clock, Q_0, Q_1, Q_2 and Q_3.

[8 + 4 + 8 marks]

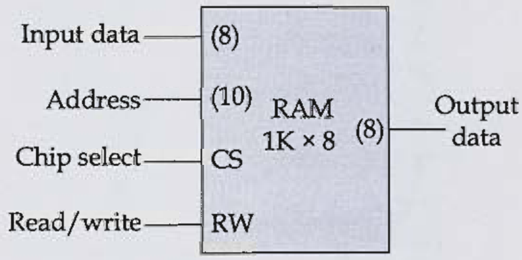
Q.4 (a) **(i)** Explain how linear convolution is performed using DFT. Find the linear convolution of $x[n] = \{1, 1, 1\}$ and $h[n] = \{1, 1\}$ using DFT.

(ii) Derive the relationship between discrete Fourier series coefficients (C_k) and discrete Fourier Transform $X(k)$ of a signal $x[n]$.

[15 + 5 marks]

Q.4 (b) **(i)** Implement the logic function $F(A, B, C, D) = \Sigma m(0, 1, 2, 3, 4, 7, 9, 10)$ using 4 : 1 MUX only. (Assume only inputs are available)

(ii) Construct a 4 K × 8 RAM with 1 K × 8 RAM chips. The 1 K × 8 RAM is as shown below:



[10 + 10 marks]

Q.4 (c) **(i)** Write an 8051 assembly language program for converting the packed BCD number stored at the location 9000H into its equivalent binary number and store the result at 9001H.

(ii) Write an 8086 assembly language program to find the sum $\sum_{i=1}^{10} i$ and store the result in accumulator.

[12 + 8 marks]

2

$6e^{-(t-10)}u(t)$

$6e^{-t}.e^{10}u(t)$

$6e^{10}.e^{-t}u(t)$

$\Downarrow \frac{6.e^{10}}{s+1}$

Section B : Digital Circuits + Signals and Systems + Microprocessors & Microcontroller

Q.5 (a) **(i)** Find the Laplace transform of the function

$f(t) = 2e^{-t}\cos 10t - t^4 + 6e^{-(t-10)}$ for $t > 0$

(ii) Find the Fourier transform for the following signal:

$$x(t) = \frac{\sin(2\pi t)}{\pi(t-1)}$$

[8 + 4 marks]

Soln: (i) $f(t) = 2e^{-t}\cos 10t - t^4 + 6e^{-(t-10)}$ $t > 0$

$$\cos 10t \longleftrightarrow \frac{s}{s^2+(10)^2}$$

$$e^{-t}\cos 10t \longleftrightarrow \frac{s+1}{(s+1)^2+(10)^2}$$

$$2e^{-t}\cos 10t \longleftrightarrow \frac{2(s+1)}{(s+1)^2+(10)^2}$$

$$t\,u(t) \longleftrightarrow -\frac{dX(s)}{ds} = \frac{n!}{s^{n+1}}$$

$$t^4 u(t) \longleftrightarrow (-1)^4 \frac{4!}{s^5} = \frac{24}{s^5}$$

$6e^{-t}u(t) \longleftrightarrow \frac{6}{[s+1]}$

$6e^{-(t-10)}u(t) \longleftrightarrow \frac{6 \cdot e^{-10s}}{(s+1)}$

$\therefore F(s) = \frac{s+1}{(s+1)^2+100} + \frac{24}{s^5} + \frac{6e^{-10s}}{(s+1)}$

5 (a) (iii) $x(t) = \frac{\sin(2\pi t)}{\pi(t-1)}$

Soln: $x(t) = \frac{\sin[2\pi(t-1+1)]}{\pi(t-1)}$

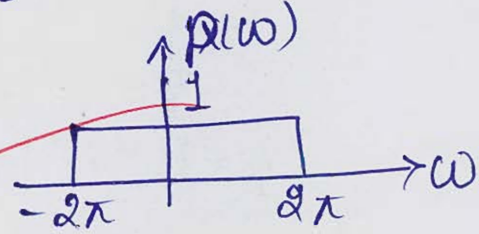
$x(t) = \frac{\sin[2\pi t - 2\pi + 2\pi]}{\pi(t-1)}$

$x(t) = \frac{\sin[2\pi(t-1)+2\pi]}{\pi(t-1)} = \frac{\sin 2\pi(t-1)}{\pi(t-1)}$

$\because \sin(2\pi+\theta) = \sin\theta$

Since we know

$p(t) = \frac{\sin(2\pi)t}{\pi t} \longleftrightarrow$



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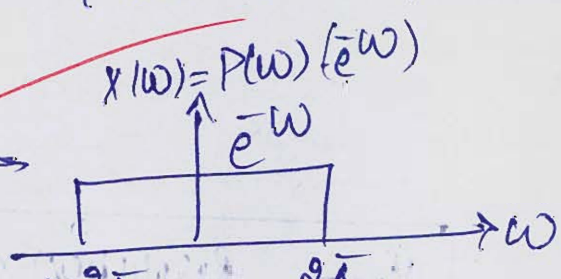
$p(t) \longleftrightarrow P(\omega)$

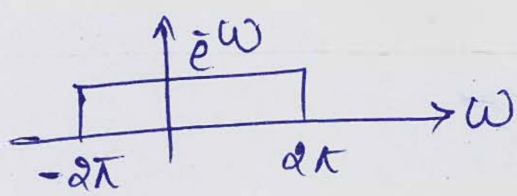
$\therefore p(t-1) \longleftrightarrow P(\omega) \cdot e^{-\omega \cdot \times 1} = P(\omega)e^{-\omega}$

$X(\omega) = P(\omega)(e^{-\omega})$

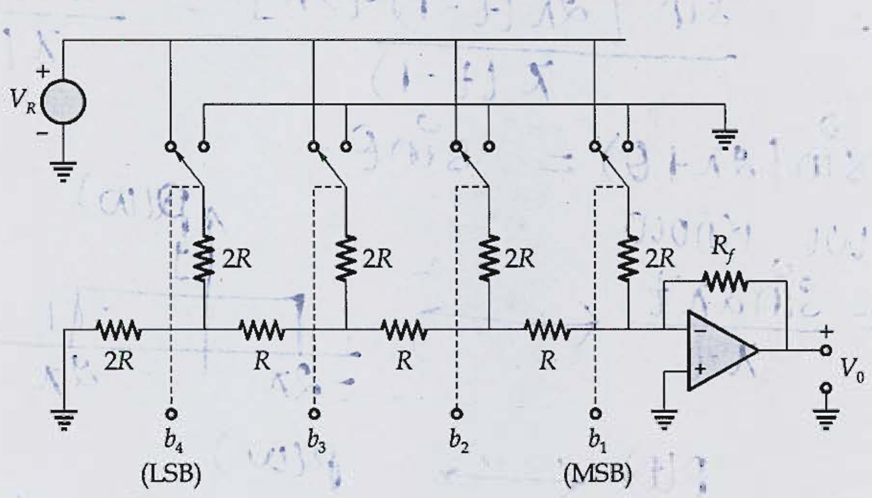
$\therefore X(\omega) \Rightarrow \frac{\sin 2\pi(t-1)}{\pi(t-1)} \longleftrightarrow$



$X(\omega) =$



Q.5 (b) Consider the *R*-2*R*, 4-bit converter shown below,



Assume the feedback resistance R_f of the op-amp is variable, the resistance $R = 5\ k\Omega$ and $V_R = 10$ V. Determine the value of R_f that should be connected to achieve the following output conditions:

(i) The value of 1 LSB at the output is 1 V.

(ii) An analog output of 8 V for a binary input of 1000.

(iii) The actual maximum output voltage of 10 V.

[12 marks]

Sol:

V_o = Resolution × |gain| × Decimal equivalent

(b) (i) $R = \frac{V_R}{2^n - 1} = \frac{10}{2^4 - 1} = 0.666$

$V_0 = R \times \left(\frac{R_f}{R}\right) \times 1$

$1 = 0.666 \times \frac{R_f}{5 \times 10^3} \times 1$

$\therefore R_f = \frac{5 \times 10^3}{0.666} \approx 7.50\ k\Omega$

(ii) for binary input of 1000 & $V_0 = 8V$

$\therefore$ Decimal equivalent is 8.

V_0 = resolution × gain × decimal equivalent

$8 = 0.666 \times \frac{R_f}{R} \times 8$

$\frac{5}{0.666} = R_f \Rightarrow R_f \approx 7.5075\ k\Omega$

(iii) The actual maximum output voltage of 10V. i.e $b_4 b_3 b_2 b_1 = 1111 = 15$

$V_0 = R \times g \times d$

$10 = 0.666 \times \frac{R_f}{R} \times 15$

$\frac{10 \times 5}{0.666 \times 15} = R_f$

$R_f = 5.0050\ k\Omega$

16

Q.5 (c) Compute and plot the convolution $y[n] = x[n] * h[n]$ using time domain approach where $x[n] = \left(\frac{1}{2}\right)^{(-n-1)} u[-n-1]$ and $h[n] = u[n-1]$.

[12 marks]

Sol:

$x(n) = \left(\frac{1}{2}\right)^{(-n-1)} u(-n-1)$; $h(n) = u(n-1)$

$$y(n) = \sum_{K=-\infty}^{\infty} x(K)\, h(n-K)$$

$$\therefore y(n) = \sum_{K=-\infty}^{\infty} \left(\frac{1}{2}\right)^{(-K-1)} u(-K-1) \cdot u[n-K-1]$$

or $$y(n) = \sum_{K=-\infty}^{\infty} \left(\frac{1}{2}\right)^{-K} \cdot \left(\frac{1}{2}\right)^{-1} u(-K-1)\, u[-K+n-1]$$

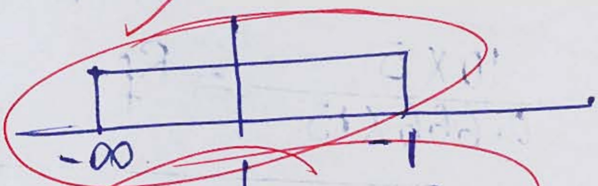
$$\therefore y(n) = 2\sum_{K=-\infty}^{\infty} \left[\left(\frac{1}{2}\right)^{-1}\right]^{K} u(-K-1)\, u(-K+n-1)$$

$$y(n) = 2\sum_{K=-\infty}^{\infty} 2^{K}\, u(-K-1)\, u(-K+n-1)$$

$u(-K-1) \Rightarrow -K-1 = 0$
$-K = 1$
$K = -1$; $\therefore -\infty < K < -1$

$u(-K+n-1) \Rightarrow -K+n-1 = 0$
$-K = -n+1$
$K = n-1$; $\therefore -\infty < K < n-1$

~~$y(n) < 2\ldots$~~



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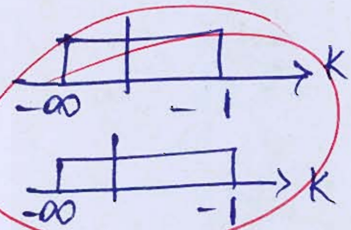
Now let us assume three conditions i.e.

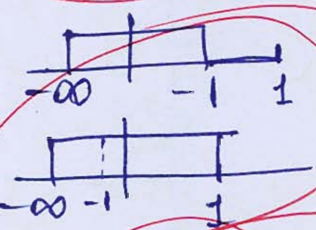
for $n=0$



$\therefore -\infty < K < -1$

for $n-1>0$

$n>1$

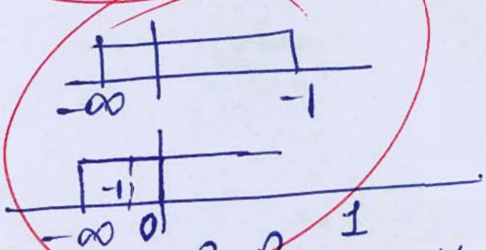


$\therefore -\infty < K < -1$

All are discrete signals.

for $n-1<0$

$n<1$



$-\infty < K < -1$

for three cases limit of $-\infty < K < -1$ is same.

$$\therefore \quad y(n) = 2 \sum_{K=-\infty}^{-1} 2^{K}$$

$$y(n) = 2\left[2^{-\infty} + \cdots + 2^{-2} + 2^{-1}\right]$$

$$y(n) = 2\left[\frac{a}{r-1}\right] = \frac{2(2^{-1})}{\left[2^{-1}-1\right]}$$

$$y(n) = \frac{2 \times \frac{1}{2}}{\left[\frac{1}{2}-1\right]} = \frac{1}{\left[\frac{-1}{2}\right]} = -2$$

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Q.5 (d) Explain the function of following pins of 8086 microprocessor:

1. $\overline{BHE}$/S7
2. MN/$\overline{MX}$
3. $\overline{TEST}$
4. READY
5. RESET
6. INTR

[12 marks]

Solu:- (2). MN | M$\overline{X}$

MN stands for minimum which is a active high signal.

M$\overline{X}$ stands for maximum which is a active low signal.

Both MN | M$\overline{X}$ works for different instructions seperately.

(3) $\overline{TEST}$: It is active low signal which is used for testing of the up at the input / output pins.

(4) READY: It is a active high signal, when the up is not ready then wait states are generated.

(5) RESET: It is signal which is used to reset the up.

(6) INTR: It is a interrupt signal which is used when another program interrupts the up ~~then~~ INTR (Interrupt Routine) is executed. which works as: up will save the current location of the instruction into the programm counter.

It will acknowledge the interrupt and all the data buses are transferred for servicing the interrupt.

6

Q.5 (e) Consider a three input Boolean function $f(a, b, c) = \Sigma m(0, 1, 2, 3, 7)$

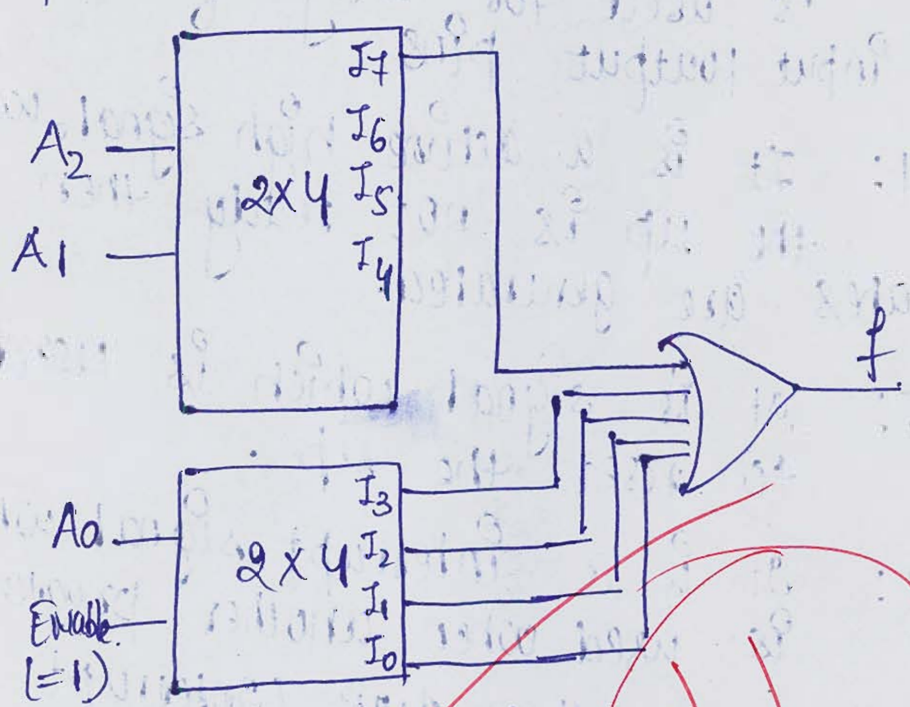
(i) Implement the function using a minimal network of 2 × 4 decoder and OR gates.

(ii) Implement the function using a minimal network of 4 × 1 multiplexers.

(iii) Implement the function using a minimal network of 2 × 1 multiplexers.

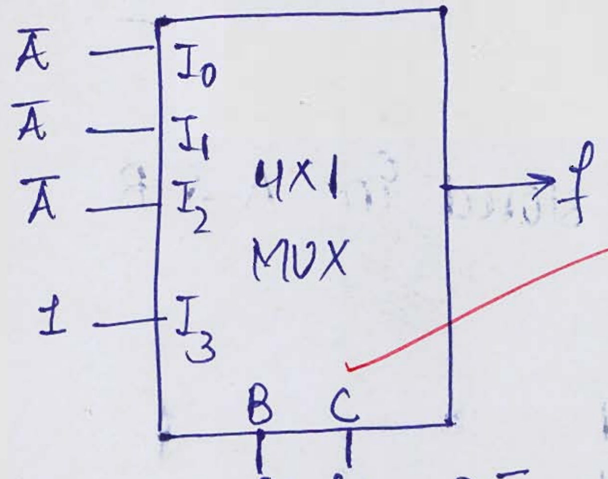
[4 + 4 + 4 marks]

Soln: (i) $f(a,b,c) = \Sigma m(0,1,2,3,7)$



1

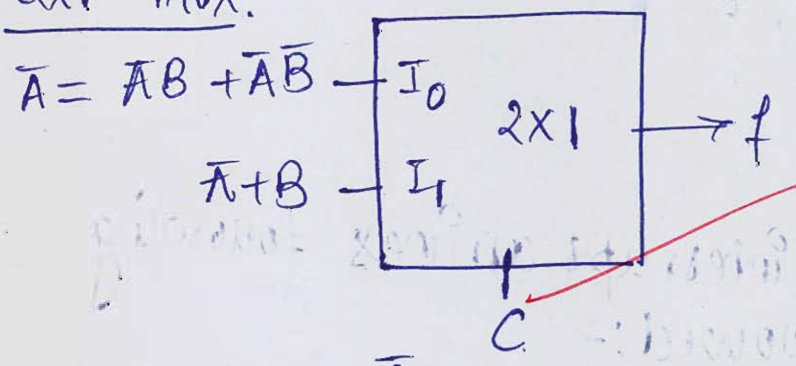
(ii) 4X1 MUX



for A is input and BC is select lines.

	$\bar{B}\bar{C}$	$\bar{B}C$	$B\bar{C}$	BC
$\bar{A}$	(0)	(1)	(2)	(3)
A	4	5	6	(7)
	I_0	I_1	I_2	I_3
	A	$\bar{A}$	$\bar{A}$	1

(iii) 2X1 MUX:



AB is input & C is slection line.

	$\bar{C}$	C
$\bar{A}\bar{B}$	(0)	(1)
$\bar{A}B$	(2)	(3)
AB	6	(7)
$A\bar{B}$	4	5

$I_0 = \bar{A}\bar{B} + \bar{A}B$ ⇓ ~~AB~~ $(\bar{A}+B)$

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Q.6 (a) (i) Write an 8086 assembly language program to add the two BCD data 29H and 98 H and store the result in BCD form in the memory locations 2000 H : 3000 H and 2000 H : 3001 H.

(ii) Explain the series of steps performed by 8086 microprocessor during processing of an interrupt request.

[10 + 10 marks]

Q.6 (a) (i) Let Data is stored in A & B

A ← 29H

B ← 98H

```
MOV A, 29H
MOV B, 98H
ADD A, B
ADD A,
MOV D, A
ADD D, 006H     if MSB > 9
ADD E, 006H     if LSB > 9
MOV 2000, D
MOV 300H, E
INC E
HLT
```

8

(ii) whenever the interrupt arrives following steps are followed:-

i) Microprocessor (μp) stores the current address into the programm counter or the next instruction which is to be executed.

ii) μp acknowledges the interrupt.

iii) through interrupt service routine μp gets the address of the interrupt. Then it gives its buses for the operation of the interrupt.

3

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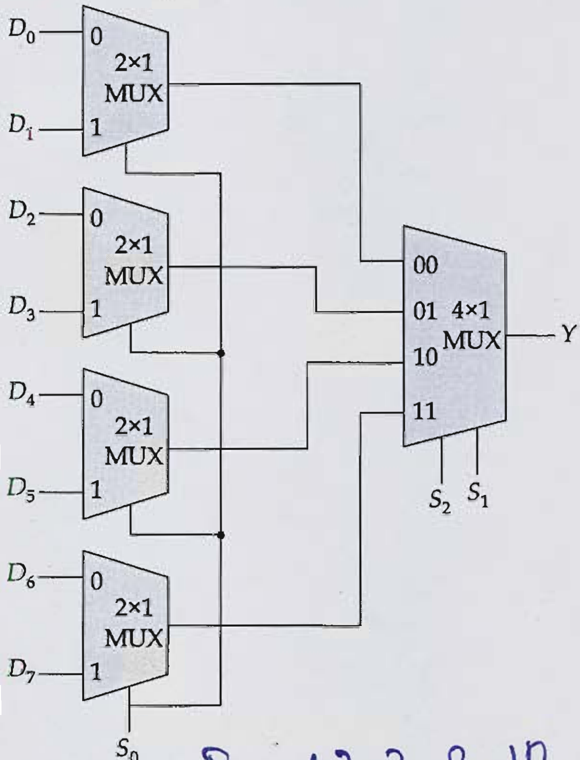
Q.6 (b) (i) Minimize the SOP terms given for a Boolean function,

$f(A, B, C, D) = \Sigma m(2, 3, 8, 10, 11, 12, 14, 15)$

Implement the minimized function using NAND gates alone.

(ii) Determine the logic equation for the output by constructing the truth table for the logic circuit shown in figure below:



[12 + 8 marks]

Q.6 (b) (i) $f(A,B,C,D) = \Sigma m(2,3,8,10,11,12,14,15)$

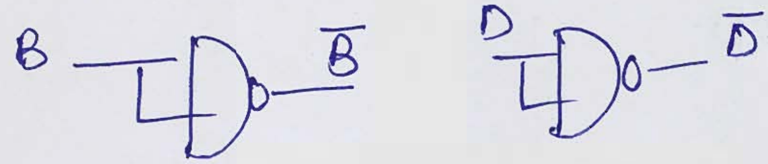
using K-MAP

	$\bar{C}\bar{D}$	$\bar{C}D$	CD	$C\bar{D}$
$\bar{A}\bar{B}$	0	1	1 3	1 2
$\bar{A}B$	4	5	7	6
AB	1 12	13	1 15	1 14
$A\bar{B}$	1 8	9	1 11	1 10

$f = \bar{B}C + AC + A\bar{D}$

$\bar{\bar{f}} = \overline{\overline{\bar{B}C + AC + A\bar{D}}} = \overline{\overline{\bar{B}C} \cdot \overline{AC} \cdot \overline{A\bar{D}}}$

$\therefore$



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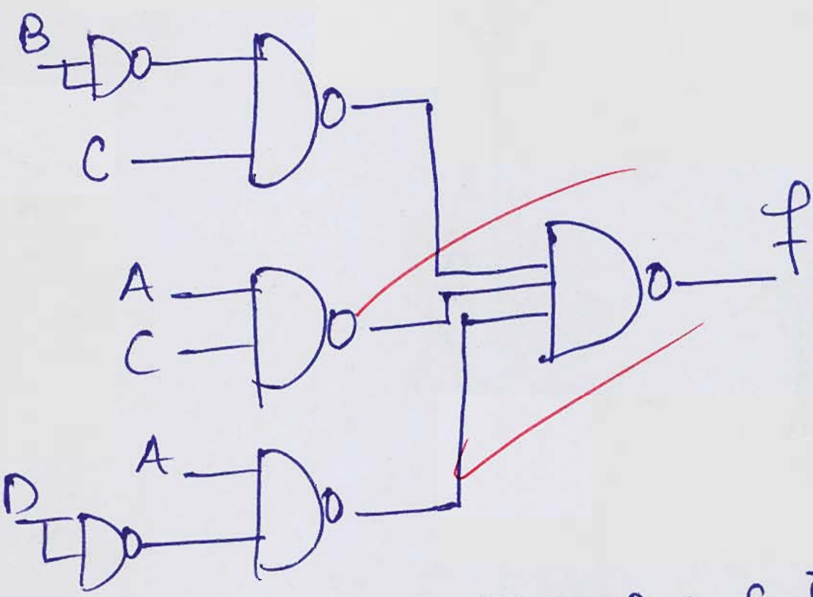


(b) (ii) $Y = \bar{S}_2 \bar{S}_1 A + \bar{S}_2 S_1 B + S_2 \bar{S}_1 C + S_2 S_1 D$

where, $A = \bar{S}_0 \cdot D_0 + S_0 \cdot D_1$

$B = \bar{S}_0 \cdot D_2 + S_0 \cdot D_3$

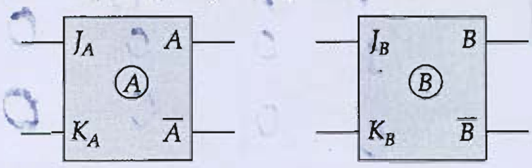
$C = \bar{S}_0 \cdot D_4 + S_0 \cdot D_5$

$D = \bar{S}_0 \cdot D_6 + S_0 D_7$

$Y = \bar{S}_2 \bar{S}_1 [\bar{S}_0 D_0 + S_0 D_1] + \bar{S}_2 S_1 [\bar{S}_0 D_2 + S_0 D_3] + S_2 \bar{S}_1 [\bar{S}_0 D_4 + S_0 D_5] + S_2 S_1 [\bar{S}_0 D_6 + S_0 D_7]$

6

6 (c) A sequential circuit has two J-K flip flops A and B as shown below, two inputs x and y, and one output Z. The flip flop input equations and circuit output equation are



$J_A = Bx + \bar{B}\bar{y}$; $K_A = \bar{B}x\bar{y}$

$J_B = \bar{A}x$; $K_B = A + x\bar{y}$

$Z = Ax\bar{y} + B\bar{x}\bar{y}$

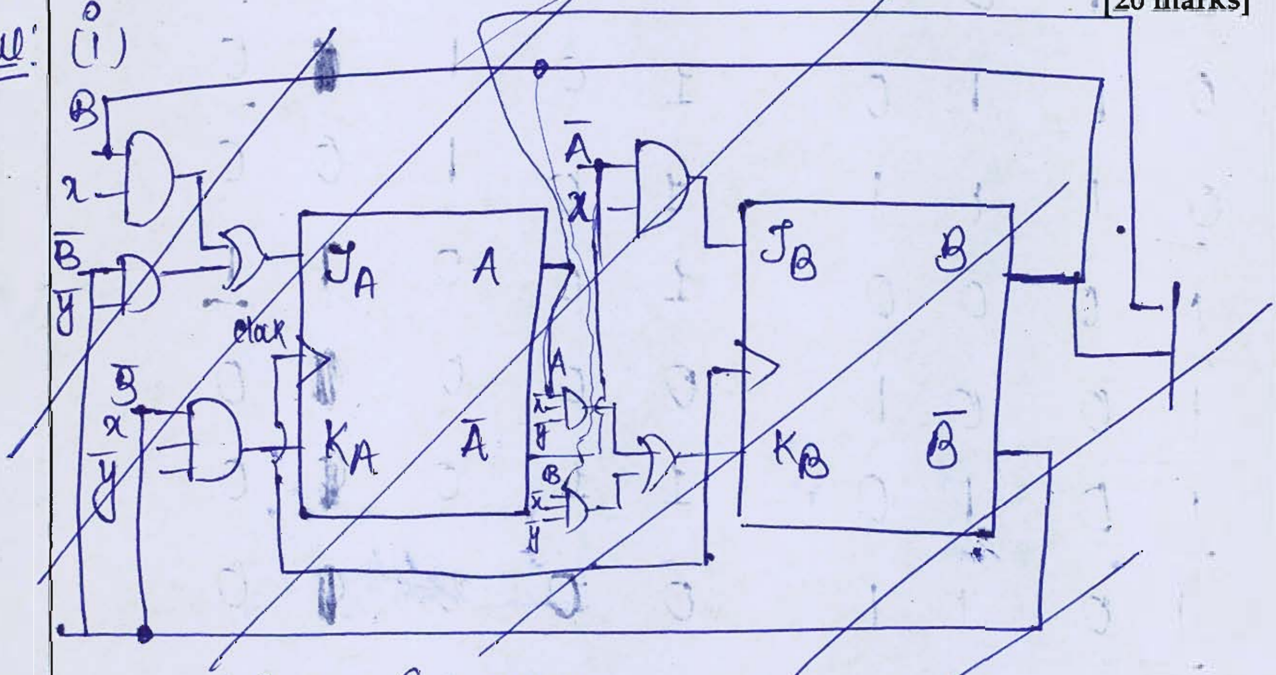
(i) Draw the logic diagram of the circuit.

(ii) Tabulate the state table.

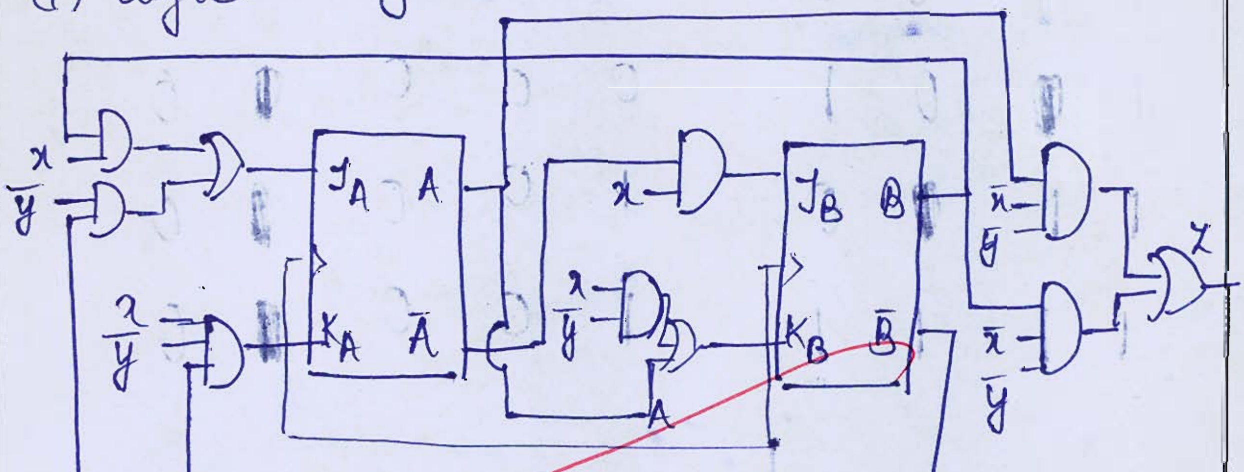
(iii) Derive the state equations for A and B.

[20 marks]

Sol: (i)



(i) logic diagram



(ii) State table

A	B	x	y	J_A	K_A	J_B	K_B	Z
0	0	0	0	1	0	0	0	0
0	0	0	1	0	0	0	0	0
0	0	1	0	1	1	1	1	0
0	0	1	1	0	0	1	0	0
0	1	0	0	0	0	0	0	0
0	1	0	1	0	0	0	0	0
0	1	1	0	1	0	1	[illegible]	0
0	1	1	1	1	0	1	0	0
1	0	0	0	1	0	0	1	1
1	0	0	1	0	0	0	[illegible]	0
1	0	1	0	1	1	0	[illegible]	0
1	0	1	1	0	0	0	[illegible]	0
1	1	0	0	0	0	0	1	1
1	[illegible]	0	1	0	0	0	[illegible]	0
1	1	[illegible]	0	1	0	0	[illegible]	0
1	1	1	1	1	0	0	[illegible]	0

iii) state equation for A & B.

A	B	Z
0	0	0
0	1	0
1	0	X
1	1	X

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Q.7 (a) **(i)** With a neat block diagram, explain the operation of counter type *ADC*. Give advantages and disadvantages of counter type *ADC*.

(ii) Define fan-out of a gate. A two-input NAND gate specifications are given as
$I_{OH(max)} = 0.4$ mA, $V_{OH(min)} = 2.7$ V, $V_{IH(min)} = 2$ V,
$V_{IL(max)} = 0.8$ V, $V_{OL(max)} = 0.4$ V, $I_{OL(max)} = 8$ mA,
$I_{IL(max)} = 0.4$ mA, $I_{IH(max)} = 25$ μA, $t_{PLH} = t_{PHL} = 15$ nsec
and supply voltage of 5 V. Determine

1. High state noise margin.
2. Low state noise margin.
3. Number of NAND gate inputs that can be driven from the output of a NAND gate of this type.

[12 + 8 marks]

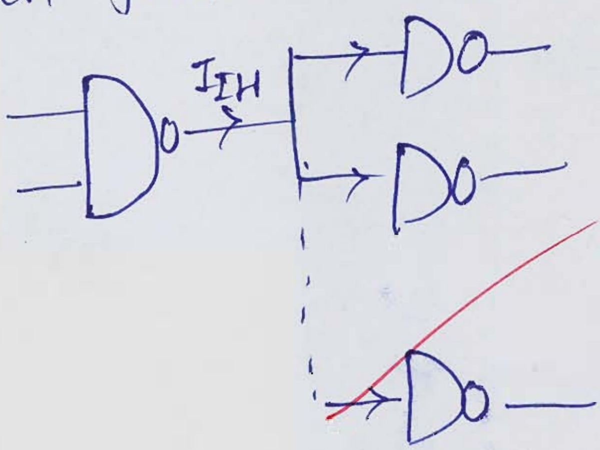
Solu: (ii) 1. High state Noise Margin.

$V_{OH} - V_{OL} = 2.7 - 2 = 0.7V$

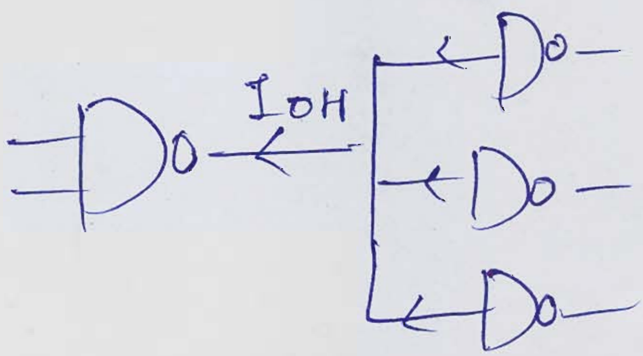
2. low state Noise margion

$V_{IL} - V_{OL} = 0.8 - 0.4 = 0.4V$

fan out: fanout represents that how many number of gates can be driven from the output of a gate.



sourcing



sinking

$$\text{fanout}\big|_{O/P} = \frac{I_{OH}}{I_{OL}} = \frac{0.4}{8} = 0.05$$

$$\text{fanout}\big|_{I/P} = \frac{I_{IL}}{I_{OL}} = \frac{0.4}{25} = 0.016$$

$$\text{fanout} = \min(0.05, 0.016) = 0.016$$

6

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Q.7 (b) Each of the following arithmetic operation is correct in atleast one number system. Determine the possible bases in each operation.

(i) 3441 + 4235 = 7676 (ii) $\frac{142}{7} = 16$

(iii) 23 + 44 + 14 + 32 = 223 (iv) 21 × 16 = 366

(v) $\frac{302}{20} = 12.1$ (vi) $\sqrt{51} = 6$

[20 marks]

Solu: (i) $(3441)_x + (4235)_x = (7676)_x$

for $x = 10$ where x is base of the system.

$3\times10^3 + 4\times10^2 + 4\times10^1 + 1\times10^0 + 4\times10^3 + 2\times10^2 + 3\times10^1 + 5\times10^0 = (7676)_{10}$

Hence, base of number system is 10.

(ii) $\frac{(142)_x}{(7)_x} = (16)_x$

$\frac{x^2+4x+2}{7} = x+6$

$x^2+4x+2 = 7x+42$

$x^2-3x-40=0$

on solving $x = 8$. So base is 8.

(iii) $(23)_x + (44)_x + (14)_x + (32)_x = (223)_x$

$2x+3+4x+4+x+4+3x+2 = 2x^2+2x+3$

$10x+13 = 2x^2+2x+3$

$2x^2+2x-10x-13+3=0$

$2x^2-8x-10=0$

$x^2-4x-5=0$ on solving $x=5$

20

v) $(21)_x \times (16)_x = (366)_x$

$[2x+x^0]\times[x+6] = 3x^2+6x+6$

$2x^2+13x+6 = 3x^2+6x+6$

$x^2-7x=0$

$x(x-7)=0 \Rightarrow \boxed{x=7}$

v) $\frac{(302)_x}{(20)_x} = (12.1)_x$

$\frac{3x^2+2}{2x} = x+2x^0+x^{-1} \Rightarrow 3x^2+2 = 2x^2+4x+\frac{2}{x}\times x$

$x^2-4x=0 \Rightarrow \boxed{x=4}$

vi) $\sqrt{51} = 6$ on whole squaring & solving

$(51)_x = (6\times6)_x$ base of the system is 7.

$5x+1 = 3x+6 \Rightarrow$ $2x=5$ $5x+1=6+6=12$

$x=\frac{5}{2}$ $\boxed{x=7}$ $x=\frac{11}{5}$

Q.7 (c) (i) Consider a discrete-time low-pass filter whose impulse response $h[n]$ is known to be real and whose frequency response magnitude in the region $-\pi \le \omega \le \pi$ is given as,

$$|H(e^{j\omega})| = \begin{cases} 1; & |\omega| \le \frac{\pi}{3} \\ 0; & \text{otherwise} \end{cases}$$

Determine the real-valued impulse response $h[n]$ for this filter when the corresponding group-delay function is $\tau_g(\omega) = \frac{3}{2}$.

(ii) Design a block level architecture of a 5 coefficient FIR filter by using appropriate number of multipliers, adders and registers. Assume that all the input operands are available in 4 bit, 2's complement fixed point representation. The architecture should give one output per clock cycle.

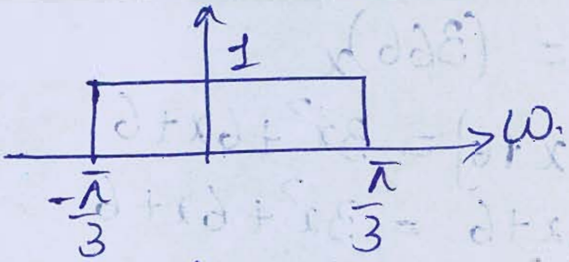
[10 + 10 marks]

Solu: (i) $\tau_g(\omega)$ is the group delay of the system.

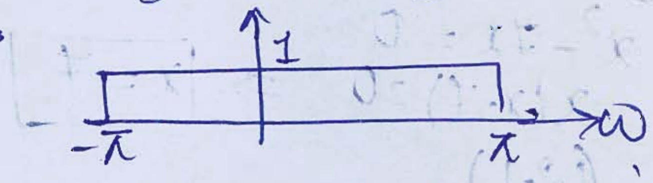
$$\tau_g = -\frac{d\phi(\omega)}{d\omega}$$

and $\tau_g(\omega) = \frac{3}{2}$

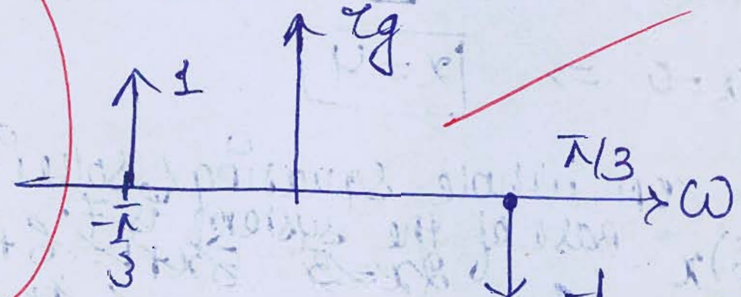
$|H(e^{j\omega})| \Rightarrow$



$h(n) \longleftrightarrow$

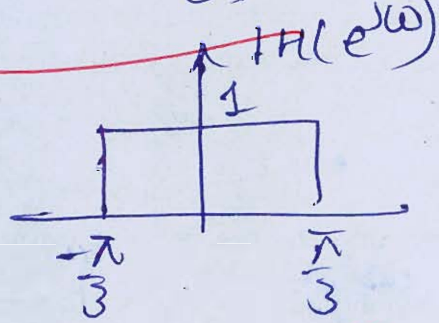


$\tau_g = -\frac{d|H(e^{j\omega})|}{d\omega}$ $\quad h(n) \longleftrightarrow |H(e^{j\omega})| \angle H(e^{j\omega})$



$\tau_g = 1\cdot\delta(n+\frac{\pi}{3}) - 1\,\delta(n-\frac{\pi}{3})$

$h(n) = \frac{\sin\frac{\pi n}{3}}{\pi n}$



Q.8 (a) (i) Draw the block diagram of programmable peripheral interface 8255A.

(ii) Explain BSR (Bit Set/Reset) mode of 8255A

(iii) Write a BSR control word subroutine to set bits PC_7 and PC_3 and reset them after some delay, using the below I/O port addresses.

$\overline{CS}$								Hexadecimal Address	Port
A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
1	0	0	0	0	0	0	0	= 80H	A
1	0	0	0	0	0	0	1	= 81H	B
1	0	0	0	0	0	1	0	= 82H	C
1	0	0	0	0	0	1	1	= 83H	Control Register

[20 marks]

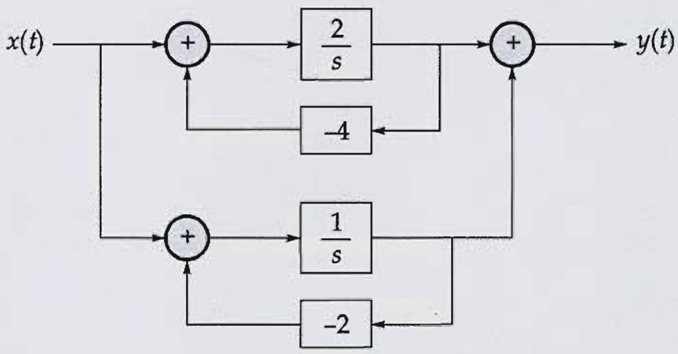
Do n
write
this m

3 (b) (i) Suppose we are given the following information about a continuous time periodic signal $x(t)$ with period 3 and Fourier series coefficients a_k:

1. $a_k = a_{k+2}$
2. $a_k = a_{-k}$
3. $\int_{-0.5}^{0.5} x(t)dt = 1$
4. $\int_{0.5}^{1.5} x(t)dt = 2$

Determine $x(t)$.

(ii) A causal LTI system 'S' has the block diagram representation as shown in figure below.



Determine a differential equation relating the input $x(t)$ to the output $y(t)$ of this system.

[10 + 10 marks]

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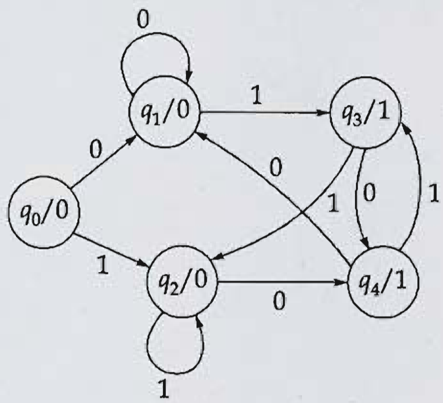
Q.8 (c) Consider the state diagram of Moore machine shown below:



Get the excitation equations and Boolean equations for output Z of Mealy machine. Also design the Mealy machine using J-K flip-flop.

[20 marks]

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Space for Rough Work

Space for Rough Work

Space for Rough Work

Space for Rough Work

Space for Rough Work

$(2x+1)(x+6)$

$2x^2+12x+x+6$

$2x^2+13x+6$

0, 1, 2, 3

$\bar{A}$ BC

A

$\sqrt{51}$

$(51)^{\frac{1}{2}}$

$x > 7$

$u(t) \leftrightarrow \frac{1}{s}$

$t\,u(t) \leftrightarrow \frac{1}{s^2} = \frac{1}{s^2}$

$t^n u(t) \leftrightarrow \frac{n!}{s^{n+1}}$

$x^2 - 3x - 40 = 0$ 4×1

$\sqrt{51} = 6$

$(51)^{\frac{1}{2}} = 6$

$(51) = (6)(6)$

$y(n) = \sum_{k=-\infty}^{\infty} x(k)\,h(n-k)$

29 / 98

16

D → 0006

E → 0006

$t - t_0 \leftrightarrow e^{-st_0}$

$\frac{\sin 2\pi(t-1+1)}{\pi(t-1)}$

$\frac{\sin[2\pi t - 2\pi + 2\pi]}{\pi(t-1)}$

$\frac{\sin[2\pi(t-1) + 2\pi]}{\pi(t-1)}$

$5x+1 = 6+6 = 12$

$5x = 11$

$x = \frac{11}{5}$

$x(t) * \delta(t) \Rightarrow x(t)|_{t=0}$

$x(t) * \delta(t-t_0)$

$x(t) * \delta(t-t_0)$

$x(t-t_0)$

$(s-1)(s+2)$

−2 t_0

gain

$\sin(360° + \theta) = \sin\theta$

(A)

$\frac{S-2}{S-1}$

$n = 2$

$V_0 = R \times D \times A$

$((2)^{-1})^{-1} = 2^1$

$\left(\frac{1}{2}\right)^{-1} \Rightarrow (2^{-1})^{-1}$

$\frac{2}{s-1} + 1$

$\frac{2+s-1}{s-1}$

$\frac{s+1}{s-1}$

$\frac{-1}{s-1} + 1$

$\frac{-1+s-1}{s-1}$

$\frac{-1+s-1}{s-1}$

$\frac{s-2}{s-1}$

A $\bar{A}$

15 ffff

10 A 000

5 fff

5 fff

+ 1

6000

$U(t+2-1)$

$U(t+1)$

$U(t-3)$

$U(t+2-3)$

$U(t-3)$

$U(t+1-3)$

$\bar{A}\bar{B} + \bar{A}B + AB$

$\bar{A}(1) + AB$

$(\bar{A}+A)(\bar{A}+B)$