ESE

Electronics & Telecom. Engineering

Preliminary Examination

(Previous Years Solved Papers 1999 to 2000)

Volume-I

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MADE EASY PUBLICATIONS

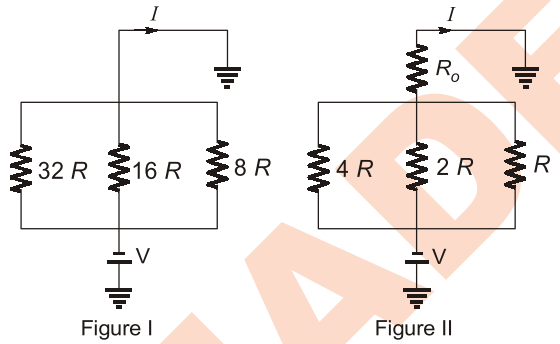
1 Network Theory

1. Basics of Network Analysis

1.1 An ideal constant voltage source is connected in series with an ideal constant current source. Considered together, the combination will be a
(a) constant voltage source
(b) constant current source
(c) constant voltage and a constant current source or a constant power source
(d) resistance

[ESE-1999]

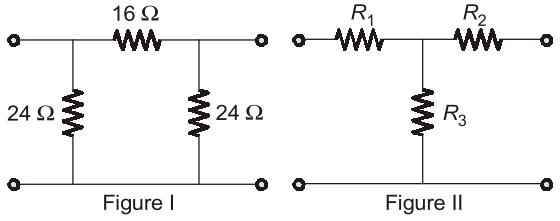
1.2 The circuit shown in Figure-I is replaced by that in Figure-II. If current 'I' remains the same, then R_0 then will be



(a) zero
(b) R
(c) $2R$
(d) $4R$

[ESE-1999]

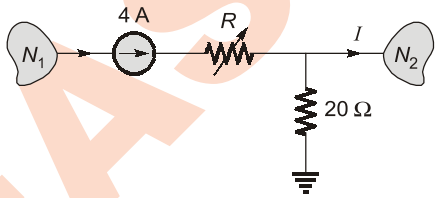
1.3 If the Π-network of Figure-I and T-network of Figure-II are equivalent, then the values of R_1, R_2 and R_3 will be respectively



(a) 9 Ω, 6 Ω and 6 Ω
(b) 6 Ω, 6 Ω and 9 Ω
(c) 9 Ω, 6 Ω and 9 Ω
(d) 6 Ω, 9 Ω and 6 Ω

[ESE-1999]

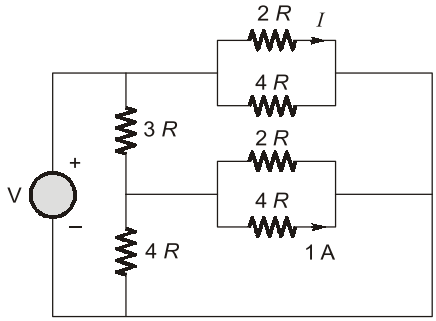
1.4 In the circuit shown in the figure, for $R = 20\ \Omega$ the current 'I' is 2 A. When R is 10 Ω, the current 'I' would be



(a) 1 A
(b) 2 A
(c) 2.5 A
(d) 3 A

[ESE-1999]

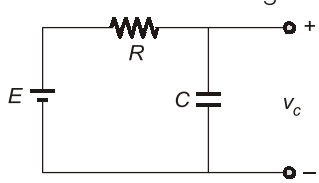
1.5 For the circuit shown in the figure, the current 'I' is



(a) indeterminable due to inadequate data
(b) zero
(c) 4 A
(d) 8 A

[ESE-1999]

1.6 Consider the following sets of values of E, R and C of the circuit shown in the figure



1. 2 V, 1 Ω and 1.25 F
2. 1.6 V, 0.8 Ω and 1 F
3. 1.6 V, 1 Ω and 0.8 F
4. 2 V, 1.25 Ω and 1 F

Which of these sets of E, R and C values will ensure that the state equation, $dv_c/dt = -1.25\ v_c + 2$ is valid?

(a) 1 and 4 (b) 1 and 2
(c) 3 and 4 (d) 2 and 3

[ESE-1999]

1.7 If a coil has diameter 'd', number of turns 'N' and form factor 'F' then the inductance of the coil is proportional to

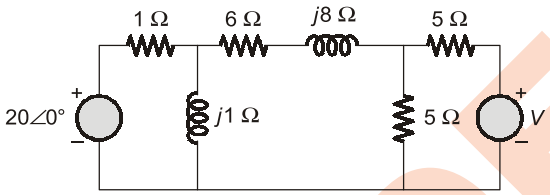
(a) N^2dF (b) Nd^2F
(c) N^2d^2/F (d) N^2d/F [ESE-2000]

1.8 A coil would behave as

(a) an inductor at high frequencies
(b) a capacitor at very low frequencies
(c) a capacitor at very high frequencies
(d) a resistor at high frequencies

[ESE-2000]

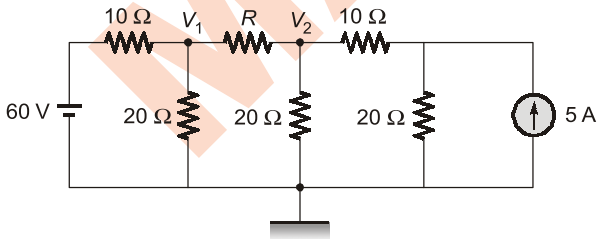
1.9 In the circuit shown below, if the power dissipated in the 6 Ω resistor is zero then V is



(a) $20\sqrt{2}\angle 45°$ (b) $20\angle 30°$
(c) $20\angle 45°$ (d) $20\sqrt{2}\angle 30°$

[ESE-2000]

1.10 In the circuit shown below, $V_1 = 40$ V when R is 10 Ω. When R is zero, the value of V_2 will be



(a) 40 V (b) 30 V
(c) 20 V (d) 10 V [ESE-2000]

1.11 A network contains only independent current sources and resistors. If the values of all resistors are doubled, the values of the node voltages

(a) will become half
(b) will remain unchanged
(c) will become double
(d) cannot be determined unless the circuit configuration and the values of the resistors are known

[ESE-2000]

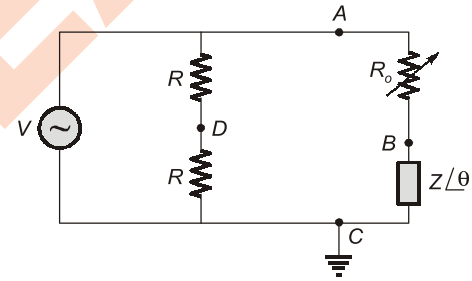
2. Steady State Sinusoidal Analysis & Resonance

2.1 A series resonant circuit has an inductive reactance of 1000 Ω, a capacitive reactance of 1000 Ω and a resistance of 0.1 Ω. If the resonant frequency is 10 MHz, then the bandwidth of the circuit will be

(a) 1 kHz (b) 10 kHz
(c) 1 MHz (d) 0.1 kHz

[ESE-1999]

2.2 In the circuit shown in the figure, if R_0 is adjusted such that $|V_{AB}| = |V_{BC}|$, then



(a) $\theta = 2\tan^{-1}\left(\frac{2|V_{BD}|}{|V|}\right)$

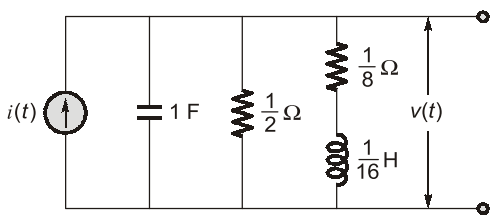
(b) $|V_{BC}| = |V_{DC}|$

(c) $|V_{AB}| = |V_{AD}|$

(d) $\theta = \tan^{-1}\left(\frac{|V_{BD}|}{|V|}\right)$

[ESE-1999]

2.3 In the circuit shown in the figure, $i(t)$ is a unit step current. The steady-state value of $v(t)$ is



(a) 2.5 V (b) 1 V
(c) 0.1 V (d) zero

[ESE-1999]

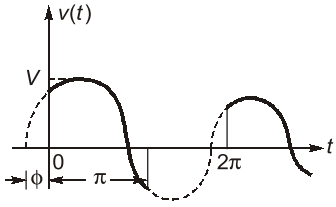
2.4 The average value of the periodic function $v(t)$ of the given figure is

(a) $\frac{V\cos\phi}{\pi}$

(b) $\frac{V\sin\phi}{\pi}$

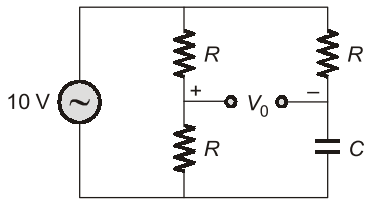
(c) $\frac{2V\cos\phi}{\pi}$

(d) $\frac{V}{\pi}$



[ESE-1999]

2.5 In the circuit shown in the figure, output $|V_0(j\omega)|$ is



(a) indeterminable as values of R and C are not given

(b) 2.5 V

(c) $5\sqrt{2}$ V

(d) 5 V

[ESE-1999]

2.6 A series LCR circuit with $R = 10\ \Omega$, $|X_L| = 20\ \Omega$ and $|X_C| = 20\ \Omega$ is connected across an AC supply of 200 V_{rms}. The rms voltage across the capacitor is

(a) $200 \angle -90°$ V (b) $200 \angle 90°$ V

(c) $400 \angle 90°$ V (d) $400 \angle -90°$ V

[ESE-2000]

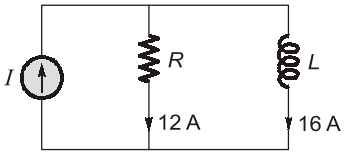
2.7 An inductor tunes at 200 kHz with 624 pF capacitor and at 600 kHz with 60.4 pF capacitor. The self-capacitance of the inductor would be

(a) 8.05 pF (b) 10.05 pF

(c) 16.10 pF (d) 20.10 pF

[ESE-2000]

2.8 In the circuit shown in the figure below, the current supplied by the sinusoidal current source I is



(a) 28 A

(b) 4 A

(c) 20 A

(d) not determinable from the data given

[ESE-2000]

2.9 A capacitor used for power factor correction in single-phase circuit decreases

(a) the power factor

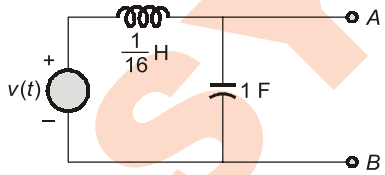
(b) the line current

(c) both the line current and the power factor

(d) the line current and increases power factor

[ESE-2000]

2.10 The circuit shown in the figure below, will act as an ideal current source with respect to terminals A and B, when frequency is



(a) zero (b) 1 rad/s

(c) 4 rad/s (d) 16 rad/s

[ESE-2000]

3. Network Theorems

3.1 **Assertion (A):** Tellegen's theorem is used in developing the sensitivity coefficient of a network from the concept of adjoint network.

Reason (R): Tellegen's theorem is applicable to any lumped network.

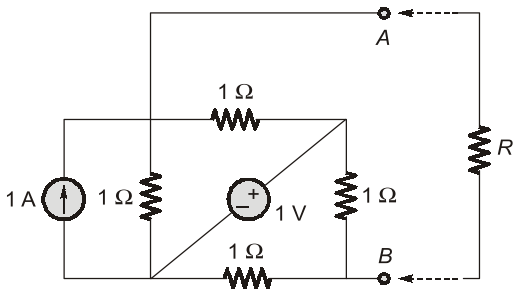
(a) Both A and R are true and R is the correct explanation of A

(b) Both A and R are true but R is NOT the correct explanation of A

(c) A is true but R is false

(d) A is false but R is true [ESE-1999]

3.2 If a resistance 'R' of 1 Ω is connected across the terminals AB as shown in the given figure, then the current flowing through R will be

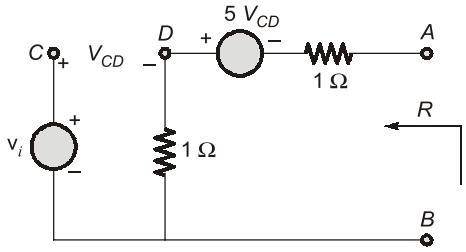


(a) 1 A (b) 0.5 A

(c) 0.25 A (d) 0.125 A

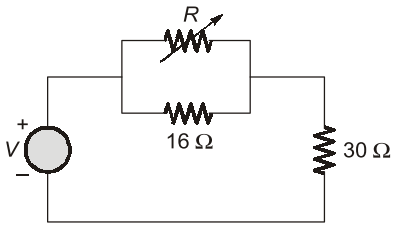
[ESE-1999]

3.3 The resistance '*R*' looking into the terminals *AB* in the circuit shown in the figure will be



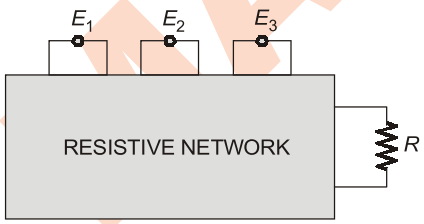
(a) 0.5 Ω (b) 2 Ω
(c) 3 Ω (d) 7 Ω **[ESE-1999]**

3.4 In the circuit shown in the figure, the power dissipated in 30 Ω resistor will be maximum if the value of *R* is



(a) 30 Ω (b) 16 Ω
(c) 9 Ω (d) zero **[ESE-1999]**

3.5 In the circuit shown in the figure below, the power consumed in the resistance *R* is measured when one source is acting at a time, these values are 18 W, 50 W and 98 W. When all the sources are acting simultaneously, the possible maximum and minimum values of power in *R* will be



(a) 98 W and 18 W (b) 166 W and 18 W
(c) 450 W and 2 W (d) 166 W and 2 W
[ESE-2000]

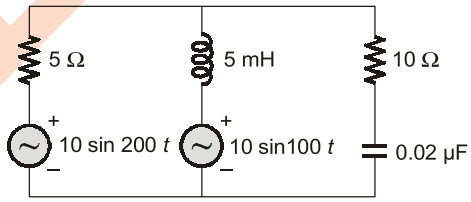
3.6 In a two-terminal network, the open-circuit voltage measured at the given terminals by an electronic voltmeter is 100 V. A short-circuit current measured at the same terminals by an ammeter of negligible resistance is 5 A. If a load resistor of 80 Ω is connected at the same terminals, then the current in the load resistor will be.

(a) 1 A (b) 1.25 A
(c) 6 A (d) 6.25 A
[ESE-2000]

3.7 Consider the following statements:
1. Tellegen's theorem is applicable to any lumped network.
2. The reciprocity theorem is applicable to linear bilateral networks.
3. Thevenin's theorem is applicable to two-terminal linear active networks
4. Norton's theorem is applicable to two-terminal linear active networks

Which of these statements are correct?
(a) 1, 2 and 3 (b) 1, 2, 3 and 4
(c) 1, 2 and 4 (d) 3 and 4
[ESE-2000]

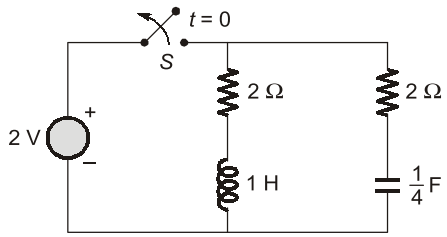
3.8 Which one of the following theorems can be conveniently used to calculate the power consumed by the 10 Ω resistor in the network shown in the figure below?



(a) Thevenin's theorem
(b) Maximum power transfer theorem
(c) Millman's theorem
(d) Superposition theorem **[ESE-2000]**

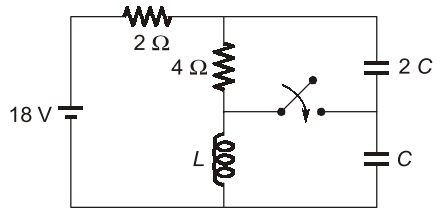
4. Transient State Analysis

4.1 On closing switch '*S*', the circuit in the given figure is in steady-state. The current in the inductor after opening the switch '*S*' will



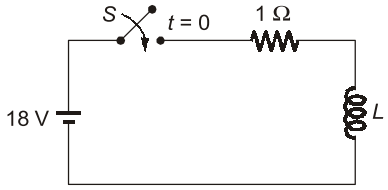
(a) decay exponentially with a time constant of 2s
(b) decay exponentially with a time constant of 0.5s
(c) consist of two decaying exponentials each with a time constant of 0.5s
(d) be oscillatory **[ESE-1999]**

4.2 In the circuit shown in the figure below, steady-state was reached when the switch S was open. The switch was closed at $t = 0$. The initial value of the current through the capacitor $2\,C$ is



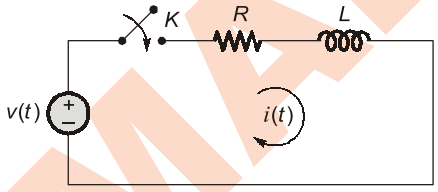
(a) zero (b) 1 A
(c) 2 A (d) 3 A [ESE-2000]

4.3 In the circuit shown below, S was initially open. At time $t = 0$, S is closed. When the current through the inductor is 6 A, the rate of change of current through the resistor is 6 A/s. The value of the inductor would be



(a) 1 H (b) 2 H
(c) 3 H (d) 4 H [ESE-2000]

4.4 In the circuit shown in the figure below, switch K is closed at $t = 0$. The circuit was initially relaxed. Which one of the following sources of $v(t)$ will produce maximum current at $t = 0^+$?



(a) Unit step
(b) Unit impulse
(c) Unit ramp
(d) Unit step plus unit ramp [ESE-2000]

5. Two Port Network Parameters

5.1 Consider the following statements for a 2-port network:

1. $Z_{11} = Z_{22}$ 2. $h_{12} = h_{21}$
3. $Y_{12} = -Y_{21}$ 4. $BC - AD = -1$

The network is reciprocal if and only if
(a) 1 and 2 are correct
(b) 2 and 3 are correct
(c) 3 and 4 are correct
(d) 4 alone is correct

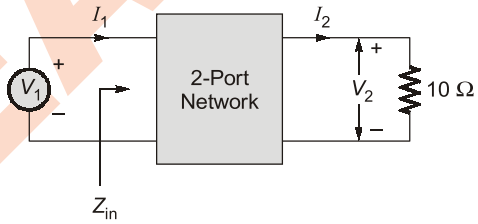
[ESE-1999]

5.2 For a two-port reciprocal network, the output open-circuit voltage divided by the input current is equal to

(a) B (b) Z_{12}
(c) $1/Y_{12}$ (d) h_{12}

[ESE-2000]

5.3 If the transmission parameters of the below network are $A = C = 1$, $B = 2$ and $D = 3$, then the value of Z_{in} is



(a) $\frac{12}{13}\,\Omega$ (b) $\frac{13}{12}\,\Omega$
(c) 3 Ω (d) 4 Ω [ESE-2000]

5.4 The impedance matrices of two, two-port networks are given by

$$\begin{bmatrix} 3 & 2 \\ 2 & 3 \end{bmatrix} \text{ and } \begin{bmatrix} 15 & 5 \\ 5 & 25 \end{bmatrix}$$

If these two networks are connected in series, the impedance matrix of the resulting two-port network will be

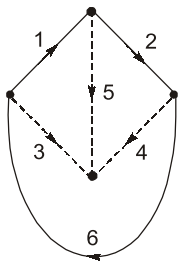
(a) $\begin{bmatrix} 3 & 5 \\ 2 & 25 \end{bmatrix}$ (b) $\begin{bmatrix} 18 & 7 \\ 7 & 28 \end{bmatrix}$

(c) $\begin{bmatrix} 15 & 2 \\ 5 & 3 \end{bmatrix}$ (d) indeterminate

[ESE-2000]

6. Graph Theory & Magnetically Coupled Circuits

6.1 Consider the graph and tree (dotted) of the given figure



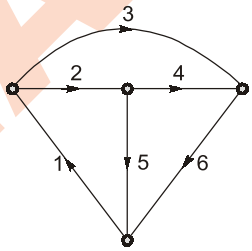
The fundamental loops include the set of lines
(a) (1, 5, 3), (5, 4, 2) and (3, 4, 6)
(b) (1, 2, 4, 3), (1, 2, 6), (3, 4, 6) and (1, 5, 4, 6)
(c) (1, 5, 3), (5, 4, 2), (3, 4, 6) and (2, 4, 3, 1)
(d) (1, 2, 4, 3) and (3, 4, 6)

[ESE-1999]

6.2 **Assertion (A):** The fundamental loop of a linear directed graph contains four twigs and two links corresponding to a given tree.
Reason (R): In a linear directed graph, a link forms a closed loop.
(a) Both A and R are true and R is the correct explanation of A
(b) Both A and R are true but R is NOT the correct explanation of A
(c) A is true but R is false
(d) A is false but R is true

[ESE-2000]

6.3 Which one of the following is a cut set of the graph shown in the figure below?



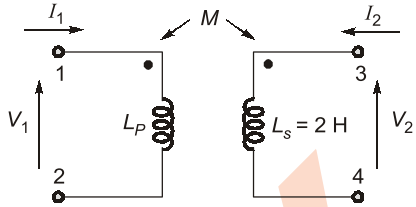
(a) 1, 2, 3 and 4
(b) 2, 3, 4 and 6
(c) 1, 4, 5 and 6
(d) 1, 3, 4 and 5

[ESE-2000]

6.4 Two coils have self-inductances of 0.09 H and 0.01 H and a mutual inductance of 0.015 H. The coefficient of coupling between the coils is
(a) 0.06 (b) 0.5
(c) 1.0 (d) 0.05

[ESE-2000]

6.5 In the transformer shown in the figure below, the inductance measured across the terminal 1 and 2 was 4 H with open terminals 3 and 4. It was 3 H when the terminal 3 and 4 were short circuited. The coefficient of coupling would be



(a) 1
(b) 0.707
(c) 0.5
(d) indeterminate due to insufficient data

[ESE-2000]

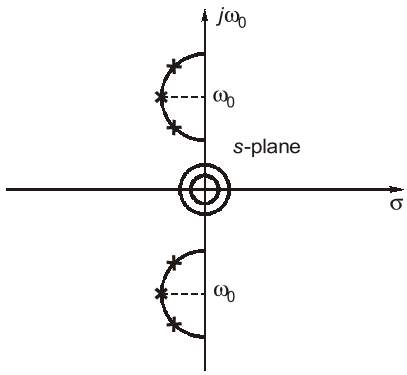
6.6 A network has 10 nodes and 17 branches. The number of different node pair voltages would be
(a) 7 (b) 9
(c) 10 (d) 45 **[ESE-2000]**

7. Network Synthesis and Filters

7.1 Voltage transfer function of a simple *RC* integrator has
(a) a finite zero and a pole at infinity
(b) a finite zero and a pole at the origin
(c) a zero at the origin and a finite pole
(d) a zero at infinity and a finite pole

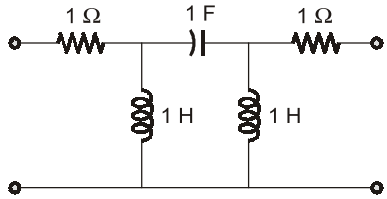
[ESE-1999]

7.2 The given figure shows the pole-zero pattern of a filter in the s-plane. The filter is a



(a) band elimination filter
(b) band-pass filter
(c) low-pass filter
(d) high-pass filter **[ESE-1999]**

7.3 Driving-point impedance of the network shown in the figure is



(a) $\frac{s^3+2s^2+s+1}{2s^2+1}$ (b) $\frac{s^3+s^2+s+1}{s^2+1}$

(c) $\frac{2s^2+1}{s^3+2s^2+s+1}$ (d) $\frac{s^3+2s^2+s+1}{s^2+1}$

[ESE-1999]

7.4 Match the **List-I** (Network) with **List-II** (Poles of driving-point impedance) and select the correct answer using the codes given below the lists:

List-I	List-II
A. *LC*	1. Negative real
B. *RC*	2. Imaginary
C. *RLC*	3. Either real or complex
D. *RL*	

Codes:

	A	B	C	D
(a)	1	2	3	1
(b)	1	2	1	3
(c)	2	1	1	3
(d)	2	1	3	1

[ESE-1999]

7.5 If two identical first order loss-pass filters are cascaded non-interactively, then the unit step response of the composite filter will be

(a) critically damped (b) underdamped

(c) overdamped (d) oscillatory

[ESE-1999]

7.6 Consider the following statements regarding the driving point admittance function.

$$Y(s) = \frac{s^2+2.5s+1}{s^2+4s+3}$$

1. It is an admittance of *RL* network.
2. Poles and zeroes alternate on the negative real axis of the s-plane.
3. The lowest critical frequency is a pole.
4. $Y(0) = 1/3$

Which of these statements are correct?

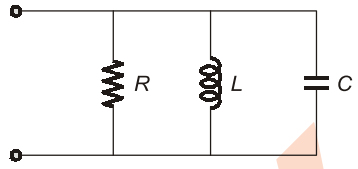
(a) 1, 2 and 3 (b) 2 and 4

(c) 1 and 3 (d) 1, 2, 3 and 4

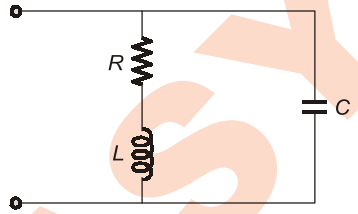
[ESE-1999]

7.7 An *R-L-C* circuit for the driving-point admittance function $\left(\frac{1/RLs}{\frac{1}{R}+\frac{1}{Ls}}+Cs\right)$ is

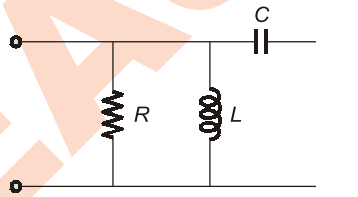
(a)



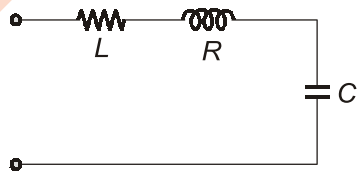
(b)



(c)



(d)



[ESE-1999]

7.8 Match **List-I** (Form) with **List-II** (Networks) and select the correct answer using the codes given below the lists:

List-I	List-II
A. Cauer I	1. L in series arms and *C* in shunt arms of a ladder
B. Cauer II	2. *C* in series arms and *L* in shunt arms of a ladder
C. Foster I	3. Series combination of *L* and *C* in parallel
D. Foster II	4. Parallel combination of *L* and *C* in series

Codes:

	A	B	C	D
(a)	1	2	3	4
(b)	1	2	4	3
(c)	2	1	4	3
(d)	2	1	3	4

[ESE-1999]

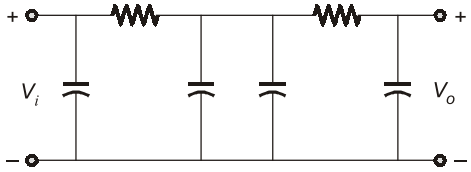
7.9 Poles and zeroes of a driving-point function of a network are simple and interlace on the $j\omega$ axis. The network consists of elements.

(a) R and C (b) L and C

(c) R and L (d) R, L and C

[ESE-1999]

7.10 For the circuit shown in the figure, the order of the differential equation relating V_0 and V_i will be



(a) 4 (b) 3

(c) 2 (d) 1 **[ESE-1999]**

7.11 **Assertion (A):** The functions given by

$$Z(s) = \frac{Ks(s^2+2)(s^2+10)}{(s^2+1)(s^2+6)}$$

represents an L-C driving point impedance function.

Reason (R): Poles and zeroes interlace on the imaginary axis of the complex s-plane.

(a) Both A and R are true and R is the correct explanation of A

(b) Both A and R are true but R is NOT the correct explanation of A

(c) A is true but R is false

(d) A is false but R is true **[ESE-2000]**

7.12 Consider the following statements:

If a network has an impedance of $(1-j)$ at a specific frequency, the circuit would consist of series

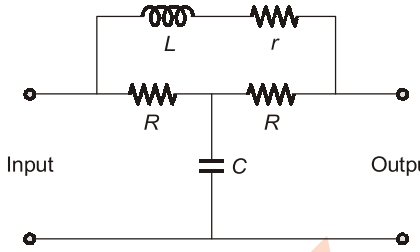
1. R and C 2. R and L 3. R, L and C

Which of these statements are correct?

(a) 1 and 2 (b) 1 and 3

(c) 1, 2 and 3 (d) 2 and 3 **[ESE-2000]**

7.13 The circuit shown in the figure below is a

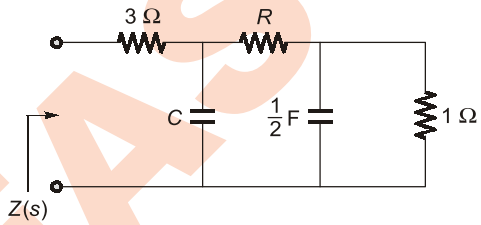


(a) low pass filter (b) high pass filter

(c) band pass filter (d) band stop filter

[ESE-2000]

7.14 $Z(s)$ for the network shown in the below figure is



$$\frac{3(s^2+6s+8)}{s^2+4s+3}$$

The value of C and R are, respectively

(a) 1/6 F and 4 Ω (b) 2/9 F and 9/2 Ω

(c) 2/3 F and 1/2 Ω (d) 1/2 F and 1 Ω

[ESE-2000]

■■■

Answers Network Theory

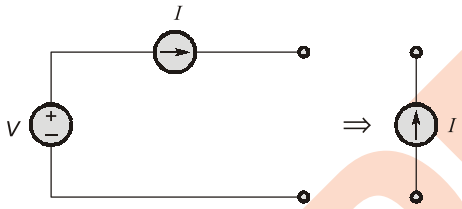
1.1	(b)	1.2	(d)	1.3	(b)	1.4	(b)	1.5	(d)	1.6	(d)	1.7	(c)	1.8	(c)	1.9	(a)
1.10	(a)	1.11	(c)	2.1	(a)	2.2	(a)	2.3	(c)	2.6	(d)	2.7	(b)	2.8	(c)	2.9	(d)
2.10	(c)	2.4	(a)	2.5	(d)	3.1	(d)	3.2	(c)	3.3	(d)	3.4	(d)	3.5	(c)	3.6	(a)
3.7	(b)	3.8	(d)	4.1	(b)	4.2	(c)	4.3	(b)	4.4	(b)	5.1	(d)	5.2	(b)	5.3	(a)
5.4	(b)	6.1	(a)	6.2	(d)	6.3	(d)	6.4	(b)	6.5	(c)	6.6	(d)	7.1	(d)	7.2	(b)
7.3	(a)	7.4	(d)	7.5	(a)	7.6	(b)	7.7	(b)	7.8	(a)	7.9	(b)	7.10	(b)	7.11	(a)
7.12	(b)	7.13	(a)	7.14	(a)												

Explanations Network Theory

1. Basics of Network Analysis

1.1 (b)

Ideal current-source in series with any element is redundant



1.2 (d)

From fig. I, $R'_{eq} = \dfrac{1}{\dfrac{1}{32R}+\dfrac{1}{16R}+\dfrac{1}{8R}} = \dfrac{32R}{7}$

From fig. II, $R''_{eq} = \dfrac{1}{\dfrac{1}{4R}+\dfrac{1}{2R}+\dfrac{1}{R}} = \dfrac{4R}{7}$

equating both

$$R'_{eq} = R''_{eq} + R_0$$

$$\Rightarrow \quad R_0 = \frac{32R}{7} - \frac{4R}{7} = \frac{28R}{7} = 4R$$

1.3 (b)

Equivalent *T*-network impedances are

$$R_1 = \frac{24\times16}{24+16+24} = \frac{24\times16}{64} = 6\ \Omega$$

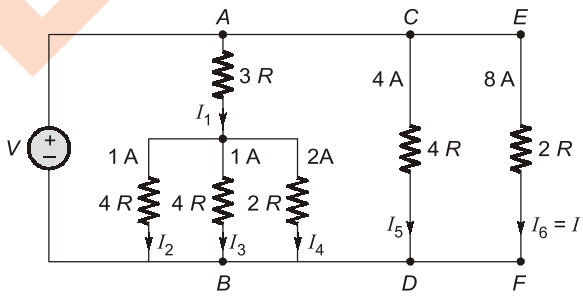
$$R_2 = \frac{24\times16}{24+16+24} = \frac{24\times16}{64} = 6\ \Omega$$

$$R_3 = \frac{24\times24}{24+16+24} = \frac{24\times24}{64} = 9\ \Omega$$

1.4 (b)

The current 'I' is independent of R. So, it will remain 2 A.

1.5 (d)



Given, $I_3 = 1$ A

then $I_2 = 1$ A

$I_4 = 2$ A

Using KCL, $I_1 = 1 + 1 + 2 = 4$ A

Equivalent resistance of branch AB

$R_{AB} = 3R + 4R \parallel 4R \parallel 2R$

$R_{AB} = 4R$

$I_5 = I_1 = 4$ A $\quad (\because R_{CD} = R_{AB})$

then $I_6 = 8$ A $= I$

1.6 (d)

Applying KVL,

$-E + Ri + v_c = 0$

But, $\quad i = C\dfrac{dv_c}{dt}$

So, $-E + RC\dfrac{dv_c}{dt} + v_c = 0$

$$\frac{dv_c}{dt} = \frac{E}{RC} - \frac{v_c}{RC}$$

Comparing with the given equation, i.e.

$$\frac{dv_c}{dt} = 1.25v_c + 2$$

$$\frac{1}{RC} = 1.25 \quad \text{... (i)}$$

$$\frac{E}{RC} = 2 \quad \text{... (ii)}$$

The values given in sets 2 & 3 satisfy the above equations.

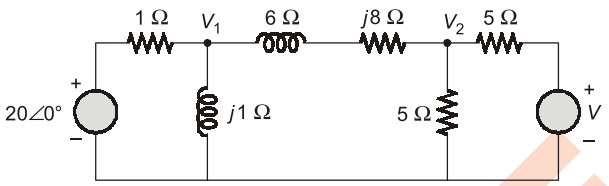
1.7 (c)

Inductance, $L \propto \frac{N^2A}{F}$

But $A = \pi d^2/4$

$\therefore \quad L \propto \frac{N^2d^2}{F}$

1.9 (a)



$$V_1 = \frac{j1}{1+j1} \cdot 20\angle 0°$$

$$\Rightarrow \quad V_1 = \frac{20}{\sqrt{2}}\angle 45°$$

Power dissipated in 6 Ω resistor is zero.

$\Rightarrow$ current through 6 Ω resistor is zero.

$$\Rightarrow \quad V_1 = V_2$$

$$V_2 = \frac{20}{\sqrt{2}}\angle 45° = \frac{5}{5+5} \cdot V = \frac{V}{2}$$

$$\Rightarrow \quad V = 20\sqrt{2}\angle 45°$$

1.10 (a)

V_1 is independent of R.

when $R = 0$, $V_1 = 40$ V

Since $R = 0$, so $V_1 = V_2$

$\Rightarrow \quad V_2 = 40$ V

1.11 (c)

Since the network contains only independent current sources, so changing all resistors in the same proportion the current through each branch will remain same but node voltages will change in the same proportion. Hence, doubling all resistors, node voltages will be doubled.

Note: If there are only independent voltage sources, then doubling all resistors, the node voltages will remain same but the current through each branch will be half.

2. Steady State Sinusoidal Analysis & Resonance

2.1 (a)

Inductive reactance,

$$\omega_0 L = 1000\ \Omega$$

Capacitive reactance,

$$\frac{1}{\omega_0 C} = 1000\ \Omega$$

Resistance, $R = 0.1\ \Omega$

Resonant frequency,

$$f_0 = 10\ \text{MHz}$$

$$\text{BW} = \frac{f_0}{Q} = \frac{f_0}{\omega_0 L/R} = \frac{Rf_0}{\omega_0 L}$$

Putting values,

$$\text{BW} = \frac{0.1 \times 10 \times 10^6}{10^3} = 10^3 = 1\ \text{kHz}$$

Other formula,

$$\text{BW} = \frac{f_0}{Q} = \frac{f_0}{1/\omega_0 CR}$$

$$= \frac{Rf_0}{1/\omega_0 C} = \frac{0.1 \times 10 \times 10^6}{10^3}$$

$$\text{BW} = 1\ \text{kHz}$$

2.2 (a)

From the figure,

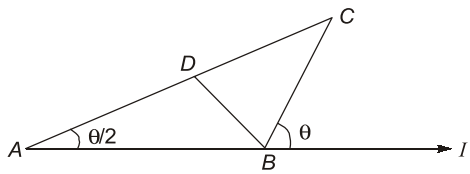
$$V_{AD} = V_{DC}$$

$$\Rightarrow \quad |V_{AD}| = |V_{DC}|$$

Given that

$$|V_{AB}| = |V_{BC}|$$

Drawing the phasor diagram of the given network,



In ΔADB & ΔCDB

$$AB = BC \because |V_{AB}| = |V_{BC}|$$

$$AD = DC \because |V_{AD}| = |V_{DC}|$$

$$\angle ADB = \angle CDB \text{ (i.e. } 90°\text{)}$$

So, ΔADB & ΔCDB are congruent triangles.

$\therefore \quad \angle ABD = \angle CBD$

But $\quad \angle ABC = 180° - \theta$

$\therefore \quad \angle ABD = (180° - \theta)/2$

$= 90° - \theta/2$

$\therefore \quad \angle BAD = \theta/2$

Now, in ΔABD,

$$\tan \theta/2 = \frac{BD}{AD}$$

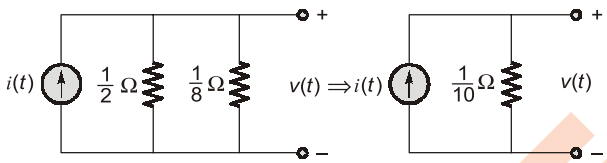
or $$\tan \theta/2 = \frac{|V_{BD}|}{|V|/2} = \frac{2|V_{BD}|}{|V|}$$

or $$\theta/2 = \tan^{-1}\left(\frac{2|V_{BD}|}{|V|}\right)$$

or $$\theta = 2\tan^{-1}\left(\frac{2|V_{BD}|}{|V|}\right)$$

2.3 (c)

The circuit in steady state will be



$$v(t) = 1 \times \frac{1}{10} = 0.1 \text{ V}$$

2.4 (a)

$$V_{avg} = \frac{\int_0^{\pi} V \sin(\omega t + \phi) d\omega t}{2\pi}$$

$$= \frac{V}{2\pi}\left[-\cos(\omega t + \phi)\Big|_0^{\pi}\right] = \frac{V}{2\pi} \cdot 2\cos\phi$$

$$V_{avg} = \frac{V}{\pi}\cos\phi$$

2.5 (d)

$$V_o = |V_R - V_C|$$

$$V_R = 10 \times \frac{R}{2R} = 5 \text{ V}$$

$$V_C = \frac{10 \times \frac{1}{j\omega C}}{R + \frac{1}{j\omega C}} = \frac{10}{j\omega CR + 1}$$

$$V_o = 5 - \frac{10}{j\omega CR + 1}$$

$$V_o = \frac{5j\omega CR + 5 - 10}{j\omega RC + 1}$$

$$V_o = \frac{5(j\omega CR - 1)}{j\omega CR + 1}$$

$$|V_o| = \frac{5\sqrt{1^2 + \omega^2 C^2 R^2}}{\sqrt{1^2 + \omega^2 C^2 R^2}} = 5 \text{ V}$$

2.6 (d)

Quality factor

$$Q = \frac{|X_L|}{R} = \frac{|X_C|}{R}$$

So, $$Q = \frac{20}{10} = 2$$

rms voltage across capacitor,

$$V_{c_{rms}} = QV \angle -90°$$

$$V_{c_{rms}} = 2 \times 200 \angle -90°$$

$$V_{c_{rms}} = 400 \angle -90° \text{V}$$

2.7 (b)

Let the self capacitance of the inductor be C_S.

$$f = \frac{1}{2\pi\sqrt{L(C + C_s)}}$$

$$200 \times 10^3 = \frac{1}{2\pi\sqrt{L(624 + C_s)}} \quad \text{... (i)}$$

$$600 \times 10^3 = \frac{1}{2\pi\sqrt{L(60.4 + C_s)}} \quad \text{... (ii)}$$

Dividing equation (ii) by equation (i)

$$3 = \sqrt{\frac{624 + C_s}{60.4 + C_s}}$$

$$\Rightarrow \quad 9 = \frac{624 + C_s}{60.4 + C_s}$$

$$\Rightarrow 543.6 + 9C_s = 624 + C_s$$

$$\Rightarrow \quad 8C_s = 80.4$$

$$\Rightarrow \quad C_s = 10.05 \text{ pF}$$

Alternate solution:

$$\text{Self capacitance } (C_d) = \frac{C_1 - n^2 C_2}{n^2 - 1}$$

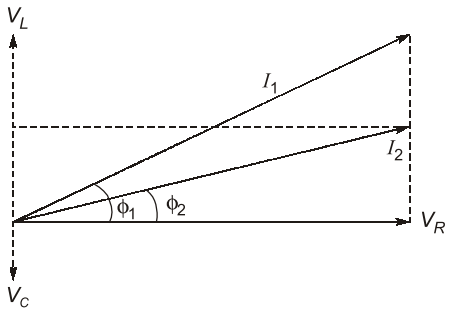
where $$f_2 = nf_1 \Rightarrow n = \frac{600}{200} = 3$$

$$C_d = \frac{624 - (a \times 60.4)}{8} = 10.05 \text{ pF}$$

2.8 (c)

$$I = \sqrt{(12)^2 + (16)^2} = \sqrt{144 + 256} = \sqrt{400} = 20 \text{ A}$$

2.9 (d)



I_1 and cos ϕ_1 are old line current and power factor respectively.

Using capacitor for power factor correction, ϕ_1 will decrease to ϕ_2. So, the resultant line current will decrease but power factor will increase.

2.10 (c)

Internal impedance of the circuit is

$$Z = \frac{Ls \cdot 1/Cs}{Ls + 1/Cs}$$

The internal impedance of an ideal current source is infinite. In other words, the internal admittance of an ideal current source is zero.

$$Y = 0 \Rightarrow \quad Ls + \frac{1}{Cs} = 0$$

$$\Rightarrow \quad \frac{1}{16}\omega = \frac{1}{\omega}$$

$$\Rightarrow \quad \omega^2 = 16$$

$$\Rightarrow \quad \omega = 4 \text{ rad/s}$$

3. Network Theorems

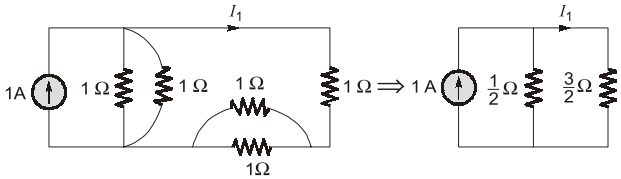
3.1 (d)

Tellegen's theorem states that the sum of power delivered to each branch of any electric network is zero. It is applicable for any lumped network having elements which are linear or non-linear, active or passive, time-varying or time-invariant.

3.2 (c)

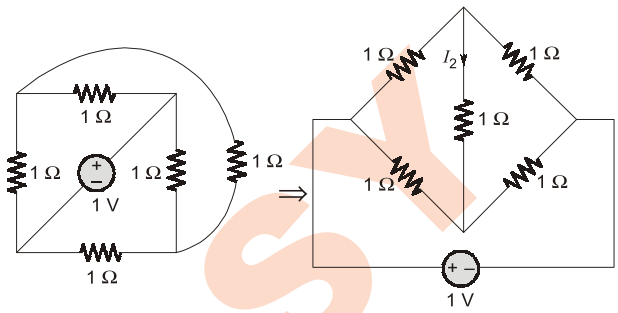
Apply superposition theorem.

First, consider only current source.



$$I_1 = \frac{\frac{1}{2}}{\frac{1}{2}+\frac{3}{2}} \cdot 1 = \frac{1}{4} = 0.25 \text{ A}$$

Now consider only voltage source.



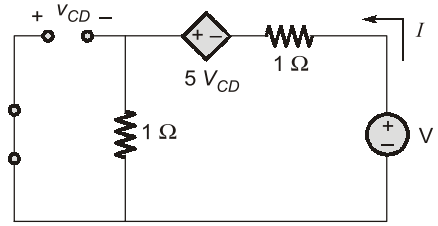
The above circuit is a balanced Wheatstone's bridge. So $I_2 = 0$.

Current flowing through R is $I = I_1 + I_2$

$= 0.25$ A

3.3 (d)

Use $\frac{V}{I} = R_{AB}$



$$V = 1\,I - 5\,V_{CD} + 1\,I \qquad \text{...(i)}$$

$$-1\,I = V_{CD} \qquad \text{...(ii)}$$

$$V = 1\,I + 5\,I + 1\,I$$

$$\frac{V}{I} = 7\ \Omega = R_{AB}$$

3.4 (d)

The power dissipated in 30 Ω resistor will be maximum when maximum current will pass through 30 Ω resistor.

For i to be i_{max}, R should be short – circuited, i.e. $R = 0$.

3.5 (c)

Maximum power,

$$P_{max} = \left(\sqrt{18} + \sqrt{50} + \sqrt{98}\right)^2$$

$\Rightarrow \quad P_{max} = 450\ W$

Minimum Power,

$$P_{min} = \left(\sqrt{98} - \sqrt{50} - \sqrt{18}\right)^2$$

$\Rightarrow \quad P_{min} = 2\ W$

3.6 (a)

$$V_{Th} = V_{OC} = 100\ V$$
$$I_{SC} = 5\ A$$
$$Z_{Th} = \frac{V_{OC}}{I_{SC}} = \frac{100}{5} = 20\ \Omega$$
$$R_L = 80\ \Omega$$
$$V_{Th} = (R_{Th} + R_L) \cdot I$$
$$\Rightarrow \quad I = \frac{V_{Th}}{R_{Th} + R_L} = \frac{100}{20 + 80} = \frac{100}{100}$$
$$\Rightarrow \quad I = 1\ A$$

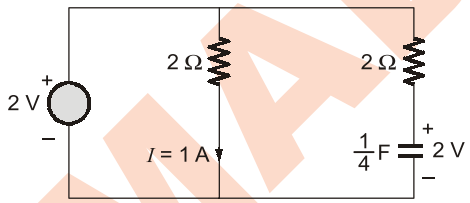
3.8 (d)

Reactive elements with sources operating at different frequencies, only superposition theorem is useful to find the response in the circuit.

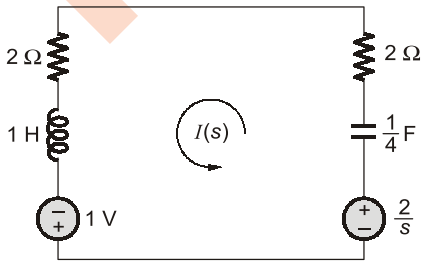
4. Transient State Analysis

4.1 (b)

When the switch '*S*' is closed and the circuit is in steady state, the circuit will be as shown below:



Now on opening the switch, the circuit in s-domain will be as shown below:



Applying KVL

$$\frac{4}{s} \cdot I(s) - \frac{2}{s} + 2 \cdot I(s) + 2 \cdot I(s) + s \cdot I(s) - 1 = 0$$

$$\Rightarrow I(s)\left[s + 4 + \frac{4}{s}\right] = 1 + \frac{2}{s}$$

$$\Rightarrow I(s)\left[\frac{s^2 + 4s + 4}{s}\right] = \frac{s + 2}{s}$$

$$\Rightarrow \quad I(s) = \frac{1}{s + 2}$$

$$\Rightarrow \quad i(t) = e^{-2t}\ A$$

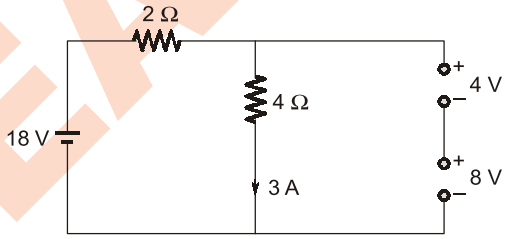
Comparing with $e^{-t/\tau}$,

$$\tau = \frac{1}{2} = 0.5\ s.$$

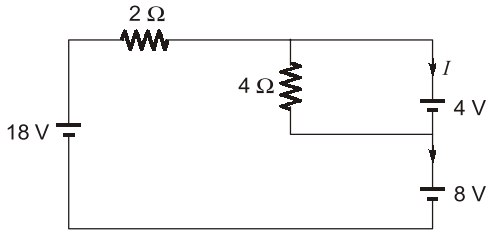
So, the current in the inductor will decay exponentially with a time constant of 0.5 s.

4.2 (c)

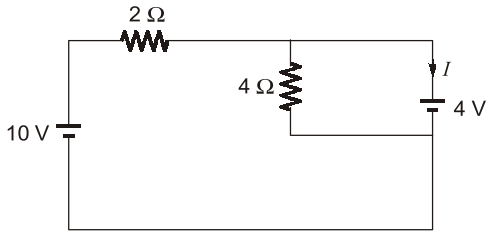
The circuit at steady state when the switch was open, is shown below:



The circuit at $t = 0$ when the switch is closed, is shown below:



The equivalent circuit of the above circuit is shown below:



$$I = \frac{10 - 4}{2} - \frac{4}{4} = 3 - 1 = 2\ A$$

4.3 (b)

$$V_L = \frac{L di}{dt}$$
$$V_R = iR = 6 \times 1 = 6\ V$$
$$V_L + V_R = 18\ V$$

$$V_L = 18 - 6 = 12\ \text{V}$$
$$12 = L \times 6$$
$$\Rightarrow \quad L = 2\ \text{H}$$

4.4 (b)

$$I(s) = \frac{V(s)}{R + sL}$$

Initial value of current

$$= i(t)\big|_{t=0^+} = \lim_{s\to\infty} sI(s) = \lim_{s\to\infty} \frac{sV(s)}{R + sL}$$

For current to be maximum, $V(s) = 1$

$\Rightarrow \quad v(t) = \delta(t)$

$\Rightarrow v(t)$ should be unit impulse for maximum current.

5. Two Port Network Parameters

5.1 (d)

The condition of reciprocity for various parameters is as follows:

Z para $\Rightarrow Z_{12} = Z_{21}$

Y para $\Rightarrow Y_{12} = Y_{21}$

h para $\Rightarrow h_{12} = -h_{21}$

g para $\Rightarrow g_{12} = -g_{21}$

$ABCD$ para $\Rightarrow AD - BC = 1$

$A'\ B'\ C'\ D'$ para $\Rightarrow A'D' - B'C' = 1$

5.2 (b)

$$\left.\frac{V_2}{I_1}\right|_{I_2 = 0} = Z_{21}$$

Since network is reciprocal, so

$$Z_{12} = Z_{21}$$

5.3 (a)

$$V_1 = AV_2 - BI_2 \Rightarrow V_1 = V_2 - 2I_2$$
$$I_1 = CV_2 - DI_2 \Rightarrow I_1 = V_2 - 3I_2$$

But $\quad V_2 = -10\, I_2$ (given)

$$Z_{in} = \frac{V_1}{I_1} = \frac{-10\ I_2 - 2I_2}{-10\ I_2 - 3I_2} = \frac{12}{13}$$

5.4 (b)

For series connection of two port network

$$[Z] = [Z_A] + [Z_B]$$
$$= \begin{bmatrix} 3 & 2 \\ 2 & 3 \end{bmatrix} + \begin{bmatrix} 15 & 5 \\ 5 & 25 \end{bmatrix}$$
$$= \begin{bmatrix} 18 & 7 \\ 7 & 28 \end{bmatrix}$$

6. Graph Theory & Magnetically Coupled Circuits

6.1 (a)

The number of fundamental loops = $b - n + 1$

Here, $\quad b = 6$ and $n = 4$.

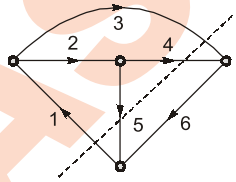
So number of fundamental loops = 6 – 4 + 1 = 3

6.2 (d)

(i) In a linear directed graph, a link forms a closed loop.

(ii) The fundamental loop of a linear directed graph contains only one link and a number of twigs.

6.3 (d)



The cut set of the graph shown is (1, 3, 4, 5).

6.4 (b)

$$M = K\sqrt{L_1 L_2}$$
$$\Rightarrow \quad 0.015 = K\sqrt{0.09 \times 0.01}$$
$$\Rightarrow \quad K = \frac{0.015}{0.3 \times 0.1} = 0.5$$

6.5 (c)

When terminals 3 & 4 are open, then

$$V_1 = \omega L_P \cdot I_1 \Rightarrow L_P = 4\ \text{H}$$

When terminal 3 and 4 are short circuited, then

$$V_1 = \omega L_P I_1 + \omega M I_2$$

and $\quad 0 = \omega L_S I_2 + \omega M I_1$

$$\Rightarrow \quad I_2 = \frac{-M}{L_S} I_1$$

So, $\quad V_1 = 4\omega I_1 + \omega M\left(\frac{-M}{L_S}\right) I_1$

Given, $\quad L_s = 2\ \text{H}$

$$\Rightarrow \quad 4 - \frac{M^2}{2} = 3$$
$$\Rightarrow \quad \frac{M^2}{2} = 1 \Rightarrow M^2 = 2$$
$$\Rightarrow \quad M = \sqrt{2}$$

Now, $\quad M = K\sqrt{L_P L_S}$

$$\Rightarrow \quad \sqrt{2} = K\sqrt{4 \times 2} = 2\sqrt{2}K$$
$$\Rightarrow \quad K = 0.5$$

6.6 (d)

Nodes, $n = 10$

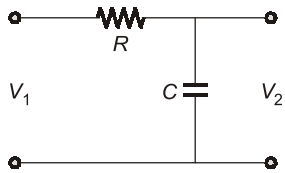
Node pair voltages

$= {}^{n}C_2 = {}^{10}C_2 = 45$

7. Network Synthesis and Filters

7.1 (d)

Simple *RC* integrator circuit is



$$\frac{V_2}{V_1} = \frac{1/Cs}{R + \frac{1}{Cs}} = \frac{1}{1 + RCs}$$

It is clear from the above expression that voltage transfer function of a simple *RC* integrator has a finite pole and a zero at infinity.

7.3 (a)

Driving-point impedance of the network is

$$Z(s) = 1 + \frac{s\left(\frac{1}{s} + s\right)}{s + \frac{1}{s} + s} = \frac{1 + s\frac{(s^2+1)}{s}}{\frac{2s^2+1}{s}}$$

$$\Rightarrow \quad Z(s) = 1 + \frac{s^3 + s}{2s^2 + 1}$$

$$= \frac{2s^2 + 1 + s^3 + s}{2s^2 + 1}$$

$$\Rightarrow \quad Z(s) = \frac{s^3 + 2s^2 + s + 1}{2s^2 + 1}$$

7.4 (d)

(i) Form of *LC* driving point impedance function is

$\frac{(s^2 + a)(s^2 + c)}{s(s^2 + b)(s^2 + d)}$ where $0 < a < b < c < d$.

It is clear that the poles are at imaginary axis.

(ii) The form of *RC* driving point impedance function is $\frac{(s + b)(s + d)}{(s + a)(s + c)}$ where $0 < a < b < c < d$.

It is clear that the poles are at negative real axis.

(iii) The form of *RL* driving point impedance function is $\frac{(s + a)(s + c)}{(s + b)(s + d)}$ where $0 < a < b < c < d$.

It is clear that the poles are at negative real axis.

7.5 (a)

Let the first order response of LPF be $1/(s + \tau)$. Since two identical LPF are cascaded non-interactively, so the unit step response of composite filter will be $1/(s + \tau)^2$, which is critically damped response.

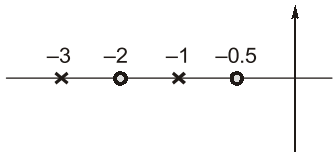
7.6 (b)

$$Y(s) = \frac{s^2 + 2.5s + 1}{s^2 + 4s + 3}$$

$$Y(0) = \frac{1}{3}$$

$$Y(s) = \frac{(s + 0.5)(s + 2)}{(s + 1)(s + 3)}$$

Pole zero plot



⇒ Since, there is a zero nearer to origin, hence lower critical frequency is zero.

So it is *RC* admittance function.

7.7 (b)

Driving point admittance function

$$Y(s) = \frac{1/RLs}{\frac{1}{R} + \frac{1}{Ls}} + Cs$$

$$= \frac{1/RLs}{\frac{Ls + R}{RLs}} + Cs = \frac{1}{Ls + R} + Cs$$

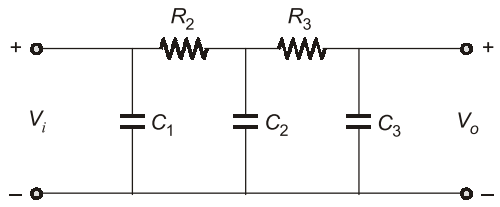
7.9 (b)

Poles and zeros of the *LC* functions always lie on $j\omega$-axis.

Poles and zeros of *RC* or *RL* functions always lie on negative real axis.

7.10 (b)

The equivalent circuit of the given circuit is shown below:



$$\frac{V_0}{V_i} = \cfrac{\cfrac{1}{C_3 s}}{C_1 s + \cfrac{1}{R_2 + \cfrac{1}{C_2 s + \cfrac{1}{R_3 + \cfrac{1}{C_3 s}}}}}$$

$$\frac{V_0}{V_i} = \cfrac{\cfrac{1}{C_3 s}}{C_1 s + \cfrac{1}{R_2 + \cfrac{1}{C_2 s + \cfrac{C_3 s}{R_3 C_3 s + 1}}}}$$

$$= \cfrac{\cfrac{1}{C_3 s}}{C_1 s + \cfrac{1}{R_2 + \cfrac{R_3 C_3 s + 1}{C_2 s(R_3 C_3 s + 1) + C_3 s}}}$$

$$= \cfrac{\cfrac{1}{C_3 s}}{\cfrac{1}{C_1 s} + \cfrac{C_2 s(R_3 C_3 s + 1) + C_3 s}{R_2\{C_2 s(R_3 C_3 s + 1) + C_3 s\} + R_3 C_3 s + 1}}$$

$$= \cfrac{\cfrac{1}{C_3 s}}{\cfrac{R_2\{C_2 s(R_3 C_3 s + 1) + C_3 s\} + R_3 C_3 s + 1 + C_1 s\{C_2 s(R_3 C_3 s + 1) + C_3 s\}}{C_1 s[R_2\{C_2 s(R_3 C_3 s + 1) + C_3 s\} + R_3 C_3 s + 1]}}$$

$= \frac{As^2 + ...}{Bs^3 + ...}$ where A and B are constants.

So, the differential equation will be of order of 3.

Note: It can directly be claimed that the order of the differential equation is equal to the number of capacitors in equivalent circuit. In fact, it can be generalized for such type of network.

7.11 (a)

In an *L*-*C* function,

(i) Poles and zeros are alternate on $j\omega$-axis.

(ii) There is either a pole or a zero at origin and infinity.

(iii) The highest and lowest powers of s in numerator and denominator can differ at the most by 1.

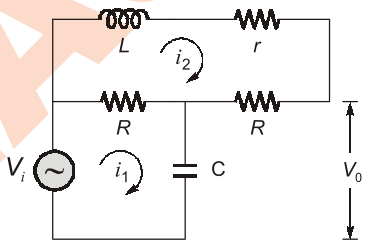
7.12 (b)

$$Z(s) = 1 - j$$

Since the impedance is capacitive, the circuit will consist of either *R* and *C* or *R*, *L* and *C* but it cannot consist only *R* and *L*.

Note: If the impedance is inductive, the circuit will consist of either *R* and *L* or *R*, *L* and *C*.

7.13 (a)



Applying KVL in loop 1 and 2,

$$V_i(s) = R[I_1(s) - I_2(s)] + \frac{1}{Cs} I_1$$

$$(sL + r)\, I_2(s) + R(2I_2(s)) - I_1(s)) = 0$$

$$V_0(s) = RI_2(s) + \frac{1}{Cs}[I_1(s) - I_2(s)]$$

$$\Rightarrow V_0(s) = \left(R - \frac{1}{Cs}\right) I_2(s) + \frac{1}{Cs}\frac{(sL + r + 2R)}{R} \cdot I_2(s)$$

$$\Rightarrow V_i(s) = \frac{\left\{\left(R + \frac{1}{Cs}\right)\frac{(sL + r + 2R)}{R} - R\right\}}{\left(R - \frac{1}{Cs}\right)\left\{\frac{sL + r + 2R}{sCR}\right\}}$$

$$\Rightarrow \frac{V_0(s)}{V_i(s)} = \frac{(sCR - 1)(sL + r + 2R)/sCR}{sC\{(sCR + 1)(sL + r + 2R) - sCR^2\}/sCR}$$

$$\Rightarrow \frac{V_0(s)}{V_i(s)} = \frac{(sCR - 1)(sL + r + 2R)}{sC\{(sCR + 1)(sL + r + 2R) - sCR^2\}}$$

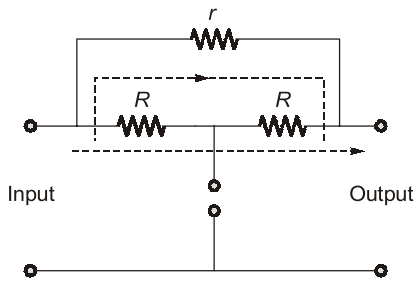
$$s \to 0 \Rightarrow \frac{V_0(s)}{V_i(s)} \to \infty$$

$$s \to \infty \Rightarrow \frac{V_0(s)}{V_i(s)} \to 0$$

Therefore, the circuit shown in the above figure is a low pass filter.

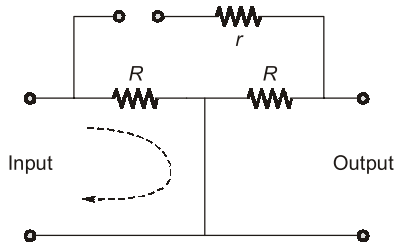
Alternate solution:

At $\omega = 0$, equivalent network is



Input reaches output.

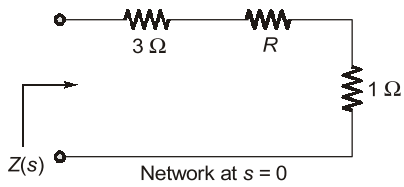
At $\omega = \infty$, equivalent network is



Input do not reach at output.

$\therefore$ Circuit shown is low pass filter.

7.14 (a)



At zero frequency i.e. at $s = 0$,

$$Z(s)\big|_{s=0} = 8$$

$$\Rightarrow 3 + R + 1 = 8$$

$$\Rightarrow R = 4\ \Omega$$

At $s = 1$,

$$Z(s) = \frac{3(1+6+8)}{1+4+3} = \frac{45}{8}$$

At $s = 1$,

$$Z(s) = 3 + \frac{14}{14C + 3}$$

$$\Rightarrow \frac{45}{8} = 3 + \frac{14}{14C + 3}$$

$$\Rightarrow \frac{14}{14C + 3} = \frac{21}{8}$$

$$\Rightarrow 16 = 42C + 9$$

$$\Rightarrow 42C = 7$$

$$\Rightarrow C = \frac{1}{6}\text{F}$$

■■■

2 Electronic Devices and Circuits

1. Semiconductor Physics

1.1 The Ohm's law for conduction in metals is

(a) $J = \sigma E$ (b) $J = E/\sigma$

(c) $J \propto \sigma E$ (d) $J \propto E/\sigma$ **[ESE-1999]**

1.2 **Assertion (A):** In a graded semiconductor, a built-in electric field exists.

Reason (R) : The built-in electric field gives improved performance to a graded base transistor as compared to a uniform base transistor.

(a) Both A and R are true and R is the correct explanation of A

(b) Both A and R are true but R is NOT the correct explanation of A

(c) A is true but R is false

(d) A is false but R is true

[ESE-1999]

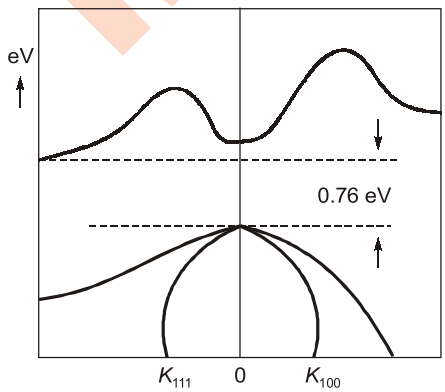
1.3 Quantum effects have to be taken into account in determining the properties of materials if

(a) $E_F = 3/2\ kT$ (b) $E_F < 3/2\ kT$

(c) $E_F > 3/2\ kT$ (d) $E_F >> 3/2\ kT$

[ESE-1999]

1.4# The band structure shown in the given figure is that of



(a) Gallium Arsenide (Ga As)

(b) Silicon (Si)

(c) Copper (Cu)

(d) Germanium (Ge) **[ESE-1999]**

1.5 Which one of the following pairs of semiconductors and current carriers is correctly matched?

(a) Intrinsic : number of electrons = number of holes

(b) *p*-type : number of electrons > number of holes

(c) *n*-type : number of electrons < number of holes

(d) Bulk : Neither electrons nor holes

[ESE-1999]

1.6 For the n-type semiconductor with $n = N_D$ and $p = n_i^2/N_D$, the hole concentration will fall below the intrinsic value because some of the holes

(a) drop back to acceptor impurity states

(b) drop to donor impurity states

(c) virtually leave the crystal

(d) recombine with the electrons

[ESE-2000]

1.7 Match **List-I** with **List-II** and select the correct answer using the codes given below the lists:

List-I

A. Drift current

B. Einstein's equation

C. Diffusion current

D. Continuity equation

List-II

1. Law of conservation of charge

2. Electric field

3. Thermal voltage

4. Concentration gradient

Codes:

	A	B	C	D
(a)	2	1	4	3
(b)	4	3	2	1
(c)	4	1	2	3
(d)	2	3	4	1

[ESE-2000]

1.8 Consider the following statements:
If an electric field is applied to an n-type semiconductor bar, the electrons and holes move in opposite directions due to their opposite charges. The net current is
1. due to both electrons and holes with electrons as majority carriers
2. the sum of electron and hole currents.
3. the difference between electron and hole current.

Which of these statements is/are correct?
(a) 1 alone (b) 1 and 2
(c) 2 alone (d) 3 alone

[ESE-2000]

1.9 **Assertion (A):** Hall crystal can be used as a multiplier of two signals.
Reason (R): Hall voltage is proportional to the currents or voltages applied in perpendicular directions across the Hall crystal.
(a) Both A and R are true and R is the correct explanation of A
(b) Both A and R are true but R is NOT the correct explanation of A
(c) A is true but R is false
(d) A is false but R is true

[ESE-2000]

2. PN-Junction Diodes

2.1 A p-n junction diode's dynamic conductance is directly proportional to
(a) the applied voltage
(b) the temperature
(c) its current
(d) the thermal voltage [ESE-1999]

2.2 The AC resistance of a forward-biased p-n junction diode operating at a bias voltage 'V' and carrying current 'I' is
(a) zero
(b) a constant value independent of V and I
(c) V/I
(d) $\Delta V/\Delta I$

[ESE-2000]

2.3 Match **List-I** (Devices) with **List-II** (Property) and select the correct answer using the codes given below the lists:

List-I
A. Silicon diode
B. Germanium diode
C. LED
D. PIN diode

List-II
1. High frequency applications
2. Very low reverse bias saturation current
3. Low forward bias voltage drop
4. Cut-off wavelength

Codes:

	A	B	C	D
(a)	1	3	4	2
(b)	2	4	3	1
(c)	1	4	3	2
(d)	2	3	4	1

[ESE-2000]

2.4 The depletion layer across a p^+ –n junction lies
(a) mostly in the p^+ – region
(b) mostly in the n – region
(c) equally in both the p^+ and n – regions
(d) entirely in the p^+ – regions [ESE-2000]

3. Bipolar Junction Transistors

3.1 A transistor with emitter base voltage (V_{EB}) of 20 mV has a collector current (I_C) of 5 mA. For V_{EB} of 30 mV, I_C is 30 mA. If V_{EB} is 40 mV, then the I_C will be
(a) 55 mA (b) 160 mA
(c) 180 mA (d) 270 mA

[ESE-1999]

3.2 Match **List-I** (Devices) with **List-II** (Characteristics) and select the correct answer using the codes given below the lists:

List-I	List-II
A. BJT	1. Voltage controlled –ve resistance
B. MOSFET	2. High current gain
C. Tunnel diode	3. Voltage regulation
D. Zener diode	4. High input impedance

Codes:

	A	B	C	D
(a)	1	4	2	3
(b)	2	4	1	3
(c)	2	3	1	4
(d)	1	3	2	4

[ESE-1999]

3.3 In a junction transistor, the collector cutoff current 'I_{CBO}' reduces considerably by doping the
(a) emitter with high level of impurity
(b) emitter with low level of impurity
(c) collector with high level of impurity
(d) collector with low level of impurity
[ESE-1999]

3.4 In a junction transistor biased for operation at emitter current 'I_E' and collector current 'I_C', the transconductance 'g_m' is
(a) kT/qI_E (b) $qI_E/\bar{k}T$
(c) I_C/I_E (d) I_E/I_C
[ESE-1999]

3.5 A transistor has a current gain of 0.99 in the CB mode. Its current gain in the CC mode is
(a) 100 (b) 99
(c) 1.01 (d) 0.99 **[ESE-2000]**

3.6 Match **List-I** (Biasing of the junctions) with **List-II** (Functions) and select the correct answer using the codes given below the lists:

List-I
A. E-B junction forward bias and C-B junction reverse bias
B. Both E-B and C-B junctions forward bias
C. E-B junction reverse bias and C-B junction forward bias
D. Both E-B and C-B junctions reverse bias

List-II
1. Very low gain amplifier
2. Saturation condition
3. High gain amplifier
4. Cut-off condition

Codes:

	A	B	C	D
(a)	2	3	1	4
(b)	3	2	1	4
(c)	3	2	4	1
(d)	2	3	4	1

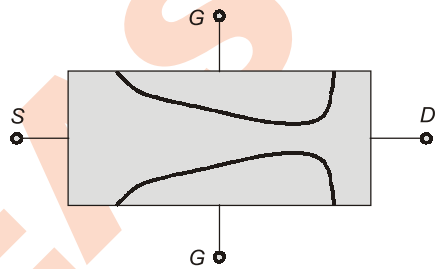
[ESE-2000]

4. Field Effect Transistors

4.1 The transconductance 'g_m' of a JFET is equal to
(a) $-\frac{2I_{DSS}}{V_P}$ (b) $\frac{2}{|V_P|}\sqrt{I_{DSS}I_{DS}}$
(c) $-\frac{2I_{DS}}{V_P}$ (d) $\frac{I_{DSS}}{V_P}\left(1-\frac{V_{GS}}{V_P}\right)$
[ESE-1999]

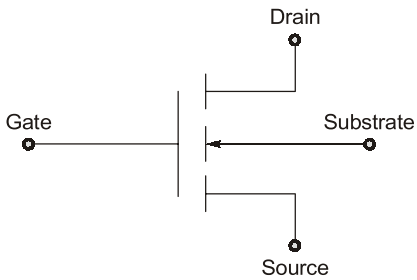
4.2 **Assertion (A):** FETs are more suitable at the input stages of millivoltmeter and CROs than BJTs.
Reason (R): A FET has lower output impedance than a BJT.
(a) Both A and R are true and R is the correct explanation of A
(b) Both A and R are true but R is NOT the correct explanation of A
(c) A is true but R is false
(d) A is false but R is true
[ESE-1999]

4.3 In a biased JFET, the shape of the channel is as shown in the given figure



because
(a) it is the property of the material used
(b) the drain end is more reverse biased than source end
(c) the drain end is more forward biased than source end
(d) the impurity profile varies with the distance from source
[ESE-1999]

4.4



The above figure shows the circuit symbol of
(a) FET (b) *P*-MOSFET
(c) CMOSFET (d) *N*-MOSFET
[ESE-2000]

4.5 Match **List-I** (Structures/characteristics) with **List-II** (Reasons) in respect of JFET and select the correct answer using the codes given below the lists:

List-I
A. *n*-channel JFET is better than p-channel JFET
B. Channel is wedge shaped

C. Channel is not completely closed at pinch-off
D. Input impedance is high

List-II

1. Reverse bias increases along the channel
2. High electric field near the drain and directed towards source
3. Low leakage current at the gate terminal
4. Better frequency performance since $\mu_n >> \mu_p$

Codes:

	A	B	C	D
(a)	4	1	2	3
(b)	4	2	1	3
(c)	3	1	2	4
(d)	3	2	1	4

[ESE-2000]

5. Special Diodes and Optoelectronic Devices

5.1 Consider the following statements:
He-Ne LASER
1. gives continuous output
2. emits red light
3. requires a DC magnet
4. can be voice modulated by using a Kerr cell

Which of these statements are correct?
(a) 1, 2 and 3 (b) 1, 3 and 4
(c) 1, 2, and 4 (d) 2, 3 and 4

[ESE-1999]

5.2 **Assertion (A):** When light falls at the junction of a p-n photo diode, its P side becomes positive and N side becomes negative.
Reason (R): When a photo diode is short-circuit, the current in the external circuit flows from the *P*-side to the *N*-side.
(a) Both A and R are true and R is the correct explanation of A
(b) Both A and R are true but R is NOT the correct explanation of A
(c) A is true but R is false
(d) A is false but R is true [ESE-2000]

5.3 Match **List-I** (Optical devices) with **List-II** (Electrical/optical characteristics) and select the correct answer using the codes given below the lists:

List-I

A. LASER
B. Solar cell
C. Photo diode
D. LED

List-II

1. Emits monochromatic light of low intensity
2. Consumes electrical power due to the incident light
3. Delivers power to a load
4. Emits monochromatic light of high intensity

Codes:

	A	B	C	D
(a)	4	3	1	2
(b)	3	4	2	1
(c)	4	3	2	1
(d)	3	4	1	2

[ESE-2000]

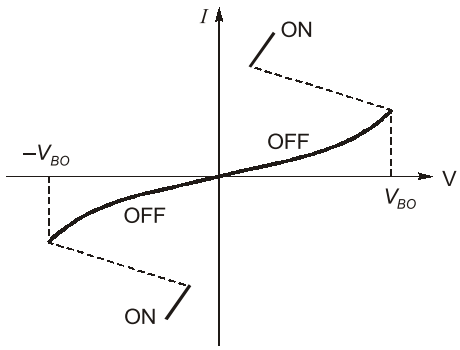
6. Power Switching Devices

6.1 Which one of the following devices is NOT used as the controller in a stabilizer?
(a) Diac (b) Triac
(c) SCR (d) Power transistor

[ESE-1999]

6.2 SCR turns OFF from conducting state to blocking state on
(a) reducing gate current
(b) reversing gate voltage
(c) reducing anode current below holding current value
(d) applying a.c. to the gate [ESE-1999]

6.3



The above graph depicts
(a) drain characteristic of a MOSFET
(b) drain characteristic of an IGBT
(c) volt-ampere characteristic of a triac
(d) volt-ampere characteristic of an SCR

[ESE-2000]

6.4 **Assertion (A):** Thyristors are preferred over power diodes in variable power rectifiers.
Reason (R): Thyristors provide controlled rectification even though they have more power loss in comparison to power diodes.
(a) Both A and R are true and R is the correct explanation of A
(b) Both A and R are true but R is NOT the correct explanation of A
(c) A is true but R is false
(d) A is false but R is true **[ESE-2000]**

6.5 Consider the following statements:
A four-layer *PNPN* device having two gate leads can be turned on by applying a
1. positive current pulse to the cathode gate
2. positive current pulse to the anode gate
3. negative current pulse to the anode gate
4. negative current pulse to the cathode gate
Which of these statements is/are correct?
(a) 1 alone (b) 1 and 3
(c) 2 alone (d) 2 and 4
[ESE-2000]

■■■

Answers Electronic Devices and Circuits

1.1	(a)	1.2	(b)	1.3	(d)	1.4	(a)	1.5	(a)	1.6	(d)	1.7	(d)	1.8	(b)	1.9	(c)		
2.1	(c)	2.2	(d)	2.3	(d)	2.4	(b)	3.1	(c)	3.2	(b)	3.3	(a)	3.4	(b)	3.5	(a)		
3.6	(b)	4.1	(b)	4.2	(a)	4.3	(b)	4.4	(d)	4.5	(a)	5.1	(c)	5.2	(b)	5.3	(c)		
6.1	(a)	6.2	(c)	6.3	(c)	6.4	(a)	6.5	(d)										

Explanations Electronic Devices and Circuits

1. Semiconductor Physics

1.1 (a)

The Ohm's law for conduction in metals is

$$J = \sigma E$$

We have $I = J \cdot A$

$$= \sigma E \cdot A$$

$$= \left(\sigma \frac{V}{l}\right) A = \frac{V}{R} \quad \text{where} \left(R = \frac{l}{\sigma A}\right)$$

where, $l \rightarrow$ length of the conductor

$A \rightarrow$ area of cross-section

$V \rightarrow$ voltage applied

1.2 (b)

In a graded semiconductor, as a result of the non-uniform doping, an electric field is generated within the semiconductor.

1.4 (a)

The band structure shown is of a material having direct bandgap energy and GaAs is a direct bandgap material.

1.5 (a)

In intrinsic semiconductor,
number of electrons = number of holes

1.7 (d)

(i) Drift current is due to electric field.

(ii) Diffusion current is due to concentration gradient.

(iii) Einstein's equation is

$$\frac{D_p}{\mu_p} = \frac{D_n}{\mu_n} = V_T$$

where V_T = thermal voltage

(iv) Continuity equation is also called the law of conservation of charge.

1.8 (b)

In a semiconductor, the net current is the sum of electron current and hole current.

2. PN-Junction Diodes

2.1 (c)

p-n junction diode's dynamic conductance

$$g_m \approx \frac{I}{\eta V_T} \text{ or } g_m \propto I.$$

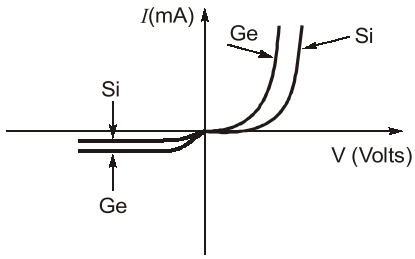
2.2 (d)

AC resistance or dynamic resistance

$$r = \Delta V / \Delta I$$

2.3 (d)

(i) The V-I characteristics of a silicon diode and germanium diode are shown below:



(ii) LED works in forward bias.

(iii) PIN diode is used in high frequency applications.

2.4 (b)

Doping ↑ → depletion layer ↓. Therefore, the depletion layer across a $p^+ - n$ junction lies mostly in the n-region.

3. Bipolar Junction Transistors

3.1 (c)

We know that $I_c = I_0 e^{+\frac{V_{EB}}{V_T}}$

$$5 = I_0 e^{\frac{20}{V_T}} \quad \text{...(i)}$$

and, $$30 = I_0 e^{\frac{30}{V_T}} \quad \text{...(ii)}$$

from equations (i) & (ii)

$$e^{\frac{10}{V_T}} = 6$$

So, $$I_0 = \frac{5}{36}\text{mA}$$ from equation (i)

So, $$I_c = I_0 e^{\frac{40}{V_T}} = \frac{5}{36}\cdot 6^4 = 180 \text{ mA}$$

3.2 (b)

(i) Zener diode is used for voltage regulation.
(ii) MOSFET has very high input impedance.
(iii) The tunnel diode exhibits a negative-resistance characteristic between the peak current I_P and the minimum value, I_V, called the valley current.

3.3 (a)

By doping the emitter with high level of impurity, the large-signal current gain of a common-base transistor, α increases. But

$$\alpha = \frac{I_C - I_{CBO}}{I_E}$$

Therefore, I_{CBO} reduces on increasing α.

3.4 (b)

$$g_m = \frac{\alpha_0}{r_e}$$

where, $\alpha_0 \rightarrow$ large-signal current gain of a common-base transistor

$r_e \rightarrow$ emitter diode resistance

$$r_e = \frac{V_T}{I_E} \text{ where } V_T = \frac{kT}{q}$$

$$\therefore \quad g_m = \frac{\alpha_0 I_E q}{kT} \qquad \because \ \alpha_0 \approx 1$$

$$\therefore \quad g_m \approx \frac{q I_E}{kT}$$

3.4 (b)

$$g_m = \frac{\alpha_0}{r_e}$$

where, $\alpha_0 \rightarrow$ large-signal current gain of a common-base transistor

$r_e \rightarrow$ emitter diode resistance

$$r_e = \frac{V_T}{I_E} \text{ where } V_T = \frac{kT}{q}$$

$$\therefore \quad g_m = \frac{\alpha_0 I_E q}{kT}$$

$$\because \quad \alpha_0 \approx 1$$

$$\therefore \quad g_m \approx \frac{q I_E}{kT}$$

3.5 (a)

$\alpha = 0.99$

$$\beta = \frac{\alpha}{1-\alpha} = \frac{0.99}{1-0.99} = 99$$

The current gain in CC mode = $\beta + 1 = 99 + 1 = 100$

4. Field Effect Transistors

4.1 (b)

The transconductance of a JFET,

$$g_m = g_{m_0}\left(1 - \frac{V_{GS}}{V_P}\right)$$

where g_{m_0} is the value of g_m for $V_{GS} = 0$, and is given by

$$g_{m_0} = \frac{-2 I_{DSS}}{V_P}$$

Also, $$I_{DS} = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

$$\Rightarrow \left(1 - \frac{V_{GS}}{V_P}\right) = \sqrt{\frac{I_{DS}}{I_{DSS}}}$$

So, $$g_m = \frac{-2 I_{DSS}}{V_P}\cdot\sqrt{\frac{I_{DS}}{I_{DSS}}}$$

or $$g_m = \frac{2}{|V_P|}\sqrt{I_{DSS} I_{DS}}$$

6. Power Switching Devices

6.1 (a)

Diac does not have a controlling signal.

6.2 (c)

The holding current may be defined as the minimum value of anode current below which it must fall for turning off the SCR.

■■■

3 Analog Circuits

1. Diodes Circuits

1.1 The ratio of available power from the DC component of a full-wave rectified sinusoid to the available power of the rectified sinusoid is

(a) $8/\pi$ (b) 2

(c) $4/\pi$ (d) $8/\pi^2$ **[ESE-1999]**

1.2 Consider the following statements in relation to a large value of capacitor filter used in a full-wave rectifier:

It gives the

1. low conduction period for the diode rectifier.
2. increased peak current rating of the diode.
3. large peak inverse voltage rating of the diode.

Which of these statements are correct?

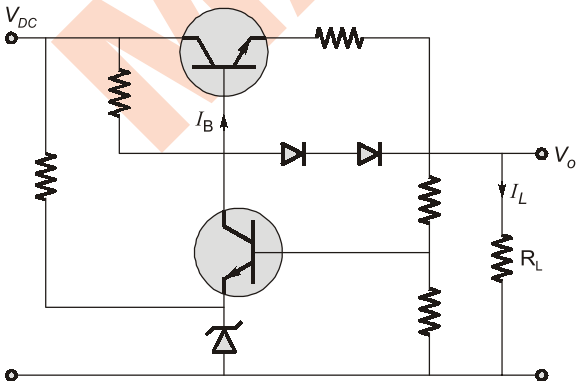
(a) 1, 2 and 3 (b) 2 and 3

(c) 1 and 2 (d) 1 and 3 **[ESE-2000]**

2. BJT Circuits

2.1 **Assertion (A):** In the circuit shown in the figure, a prescribed value of load current I_L, V_0 will gradually fall.

Reason (R): Above the prescribed value, as load current I_L increases, I_B decreases.



(a) Both A and R are true and R is the correct explanation of A

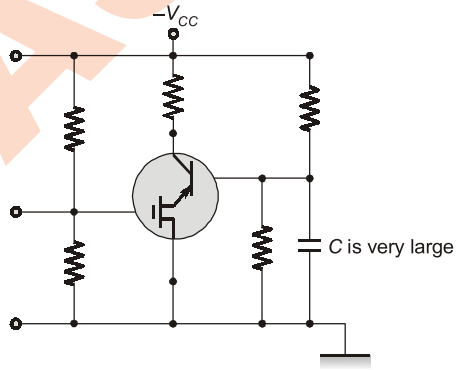
(b) Both A and R are true but R is NOT the correct explanation of A

(c) A is true but R is false

(d) A is false but R is true

[ESE-1999]

2.2 The given figure shows a composite transistor consisting of a MOSFET and a bipolar transistor in cascode



The MOSFET has a transconductance g_m of 2 mA/V and the bipolar transistor has $\beta(\triangleq h_{fe})$ of 99. The overall transconductance of the composite transistor is

(a) 198 mA/V (b) 19.8 mA/V

(c) 1.98 A/V (d) 1.98 mA/V

[ESE-1999]

2.3 The input resistance of a common emitter stage can be increased by

1. unbypassing emitter resistance
2. bootstrapping
3. biasing it at low quiescent current
4. using compounded BJTs

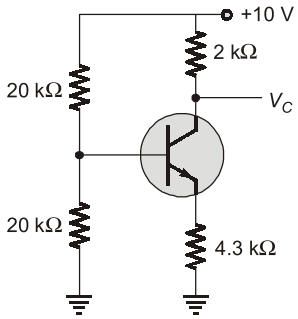
The correct sequence in descending order of the effectiveness of these methods is

(a) 2, 4, 1, 3 (b) 4, 3, 2, 1

(c) 2, 4, 3, 1 (d) 4, 2, 3, 1

[ESE-1999]

2.4 The collector voltage V_C of the circuit shown in the given figure is approximately

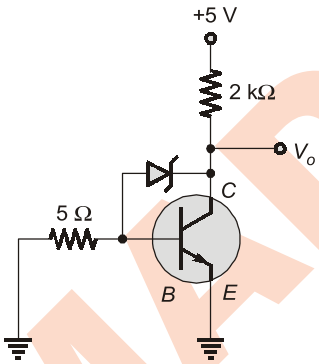


(a) 2 V (b) 4.6 V
(c) 8 V (d) 8.6 V **[ESE-1999]**

2.5 Consider the following devices:
1. BJT in CB mode
2. BJT in CE mode
3. JFET
4. MOSFET

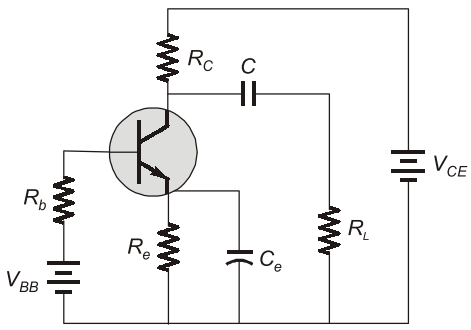
The correct sequence of these devices in increasing order of their input impedance is
(a) 1, 2, 3, 4 (b) 2, 1, 3, 4
(c) 2, 1, 4, 3 (d) 1, 3, 2, 4 **[ESE-1999]**

2.6 The voltage V_0 of the circuit shown in the given figure is



(a) 5 V (b) 3.1 V
(c) 2.5 V (d) zero **[ESE-1999]**

2.7 A common emitter amplifier circuit is shown in the given figure



The slope of AC load line is

(a) $-\left(\frac{1}{R_L}+\frac{1}{R_C}\right)$ (b) $-\left(\frac{1}{R_L+R_C}\right)$

(c) $-\frac{1}{R_L}$ (d) $-\frac{1}{R_C}$

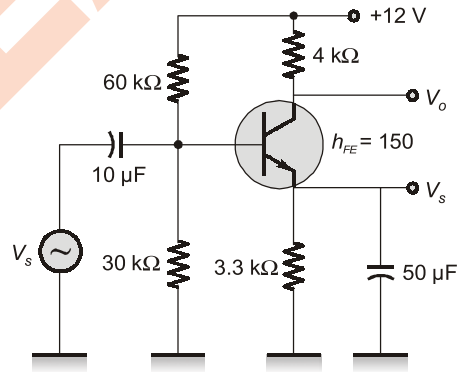
[ESE-2000]

2.8 Consider the following circuit configurations:
1. Common emitter
2. Common base
3. Emitter follower
4. Emitter follower using Darlington pair

The correct sequence in increasing order of the input resistances of these configurations is
(a) 2, 1, 4, 3 (b) 1, 2, 4, 3
(c) 2, 1, 3, 4 (d) 1, 2, 3, 4

[ESE-2000]

2.9 An amplifier circuit is shown in the given figure:



The voltage gain (V_0 / V_s) is
(a) 4/3.33 (b) 100
(c) 150 (d) 160

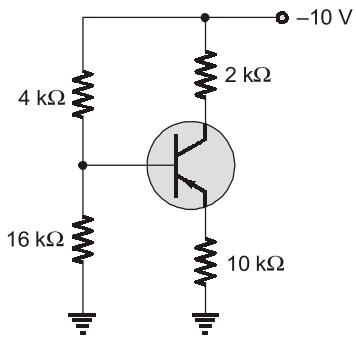
[ESE-2000]

2.10 Consider the following statements regarding the bootstrap biasing arrangement for a BJT emitter follower:
1. The input impedance is very high.
2. The voltage gain is exactly equal to one.
3. The output impedance is equal to zero.

Which of these statements is correct?
(a) None (b) 2 alone
(c) 3 alone (d) 1 alone

[ESE-2000]

2.11 In the circuit shown in the given figure, the approximate voltages at the transistor



(a) base and emitter respectively are –8 V and –7.3 V
(b) base and collector respectively are –8 V and –5 V
(c) collector and emitter respectively are –8 V and –7.3 V
(d) base, emitter and collector respectively are –8 V, –7.3 V and –5 V

[ESE-2000]

2.12 If a common emitter amplifier with an emitter resistance R_e has an overall transconductance gain of –1 mA/V, a voltage gain of –4 and desensitivity of 50, then the value of the emitter resistance R_e would be
(a) 50 kΩ (b) 0.98 kΩ
(c) 50 MΩ (d) 0.98 MΩ

[ESE-2000]

2.13 *CE* configuration is the most preferred transistor configuration when used as a switch because it
(a) requires only one power supply
(b) requires low voltage or current
(c) is easily understood by every one
(d) has small I_{CEO} [ESE-2000]

3. FET and MOSFET Circuits

3.1 An FET is a better chopper than a BJT because it has
(a) lower offset voltage
(b) higher series ON resistance
(c) lower input current
(d) higher input impedance [ESE-2000]

4. Frequency Response of Amplifiers & Filters

4.1 A second-order band-pass active filter can be obtained by cascading a low-pass second-order section having cut-off frequency f_{OH} with a high-pass second-order section having cut-off frequency f_{OL}, provided
(a) $f_{OH} > f_{OL}$ (b) $f_{OH} < f_{OL}$
(c) $f_{OH} = f_{OL}$ (d) $f_{OH} \leq 1/2\ f_{OL}$

[ESE-1999]

4.2 Consider the following statements:
The lower cut-off frequencies for an *RC* coupled *CE* amplifier depend on
1. input and output coupling capacitors
2. emitter bypass capacitor
3. junction capacitors

Which of these statements is/are correct?
(a) 1 alone (b) 2 alone
(c) 1 and 2 (d) 2 and 3 [ESE-2000]

4.3 An amplifier network is unconditionally stable if
(a) real part of Z_{in} and Z_{out} are greater than zero for some positive real impedances of the source and load.
(b) real part of Z_{in} and Z_{out} are greater than zero for all positive real impedances of the source and load
(c) Z_{in} and Z_{out} are complex conjugates of each other for some positive real impedances of the source and load
(d) Z_{in} and Z_{out} are complex conjugates of each other for all positive real impedances of the source and load

[ESE-2000]

4.4 If the *Q* of a single-stage single-tuned amplifier is doubled, then its bandwidth will
(a) remain same (b) become half
(c) become double (d) become four times

[ESE-2000]

4.5 An amplifier using BJT has two identical stages each having a lower cut-off (3 dB) frequency of 64Hz due to coupling capacitor. The emitter bypass capacitor also provides a lower cut-off (3 dB) frequency due to emitter degeneration alone of 64 Hz. The lower (3 dB) frequency of the overall amplifier is nearly
(a) 100 Hz (b) 128 Hz
(c) 156 Hz (d) 244 Hz

[ESE-2000]

4.6 **Assertion (A):** The hybrid π-model of a transistor can be reduced to its h-parameter model and vice-versa.

Reason (R): Hybrid π and *h*-parameter models are inter-related as both of them describe the same transistor.

(a) Both A and R are true and R is the correct explanation of A
(b) Both A and R are true but R is NOT the correct explanation of A
(c) A is true but R is false
(d) A is false but R is true

[ESE-2000]

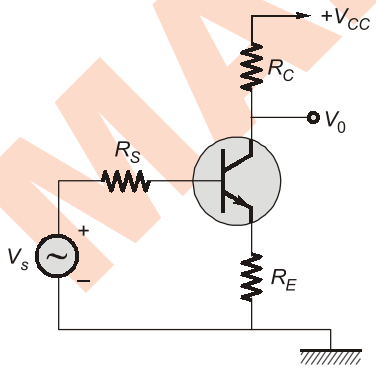
5. Feedback Amplifiers

5.1 **Assertion (A):** A large negative feedback is deliberately introduced in an amplifier to make its gain independent of the variation of parameters of the active device and other circuit components.
Reason (R): A large negative feedback results in a high value of return difference compared to unity, which makes the feedback gain inversely proportional to the feedback factor.

(a) Both A and R are true and R is the correct explanation of A
(b) Both A and R are true but R is NOT the correct explanation of A
(c) A is true but R is false
(d) A is false but R is true

[ESE-1999]

5.2 The given circuit has a feedback factor of



(a) $-R_C/R_S$ (b) $-R_E/R_C$
(c) $-R_E/R_S$ (d) $-R_C/R_E$

[ESE-1999]

5.3 The voltage gain of an amplifier without feedback and with negative feedback respectively are 100 and 20. The percentage of negative feedback (β) would be

(a) 4% (b) 5%
(c) 20% (d) 80%

[ESE-2000]

5.4 **Assertion (A):** For equal outputs, the harmonic distortion is reduced in CE amplifier with the introduction of negative feedback.
Reason (R): Nonlinear distortion usually arises due to signals traversing the large part of the dynamic characteristic of the transistor at the output stage.

(a) Both A and R are true and R is the correct explanation of A
(b) Both A and R are true but R is NOT the correct explanation of A
(c) A is true but R is false
(d) A is false but R is true [ESE-2000]

6. Oscillators

6.1 **Assertion (A):** Miller sweep circuit producing sawtooth waveform is a relaxation oscillator.
Reason (R): The active device alternately supplies power to the load and relaxes when it is cut-off.

(a) Both A and R are true and R is the correct explanation of A
(b) Both A and R are true but R is NOT the correct explanation of A
(c) A is true but R is false
(d) A is false but R is true

[ESE-1999]

6.2 A Hartley oscillator is used for generating

(a) very low frequency oscillation
(b) radio-frequency oscillation
(c) microwave oscillation
(d) audio-frequency oscillation

[ESE-1999]

6.3 In every practical oscillator, the loop gain is slightly larger than unity and the amplitude of the oscillations is limited by the

(a) magnitude of the loop gain
(b) onset of non-linearity
(c) magnitude of the gain of the amplifier
(d) feedback transmission factor

[ESE-2000]

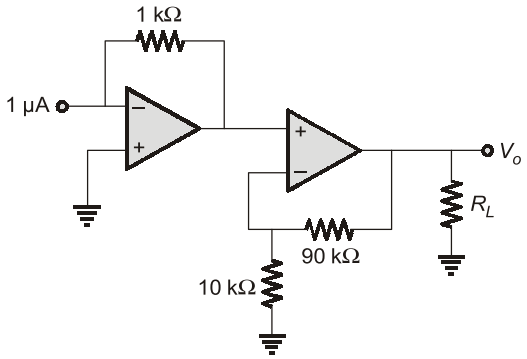
7. Operational Amplifiers

7.1 In a single-stage differential amplifier, the output offset voltage is basically dependent on the mismatch of

(a) V_{BE}, I_B and β (b) V_{BE} and I_B
(c) I_B and β (d) V_{BE} and β

[ESE-1999]

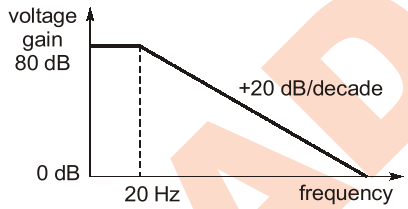
7.2 The output voltage V_0 of the given circuit



(a) –100 V (b) –100 mV
(c) 10 V (d) –10 mV

[ESE-1999]

7.3 The voltage gain versus frequency curve of an Op-Amp is shown in the given figure

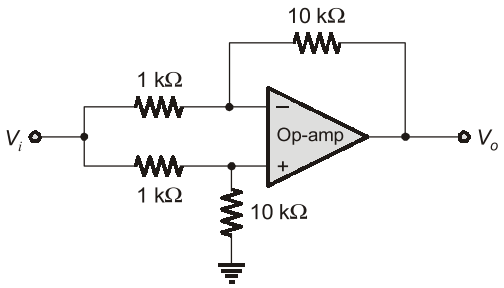


The gain-bandwidth product of the Op-Amp is

(a) 200 Hz (b) 200 MHz
(c) 200 kHz (d) 2 MHz

[ESE-1999]

7.4 The V_0 of the Op-Amp circuit shown in the given figure is



(a) 11 V_i (b) 10 V_i
(c) V_i (d) zero [ESE-1999]

7.5 **Assertion (A):** Op-amps with FET input stages have less gain than those with BJT.
Reason (R): BJT has higher transconductance than FET.

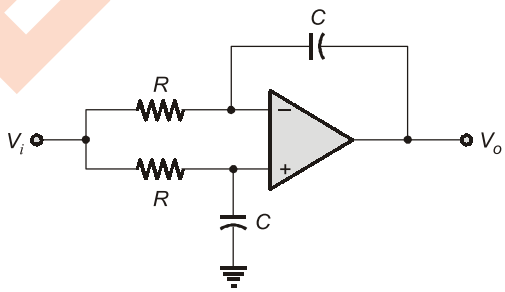
(a) Both A and R are true and R is the correct explanation of A
(b) Both A and R are true but R is NOT the correct explanation of A
(c) A is true but R is false
(d) A is false but R is true [ESE-2000]

7.6 Consider the following statements:
A totem pole configuration used in the output stage of an op-amp has the advantage of using
1. only n-p-n BJTs
2. complementary symmetrical pair of transistors.
3. only one transistor

Which of these statements is/are correct?

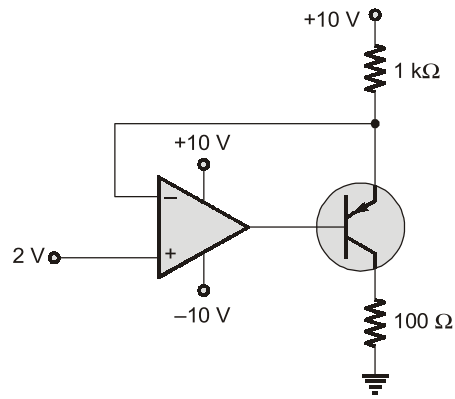
(a) 1 alone (b) 2 alone
(c) 3 alone (d) 1 and 3 [ESE-2000]

7.7 The op-amp circuit shown in the given figure is



(a) a high-pass circuit
(b) a low-pass circuit
(c) a band-pass circuit
(d) an all-pass circuit [ESE-2000]

7.8 In the circuit shown below, the current flowing through resistance of 100 Ω would be



(a) 8 mA (b) 10 mA
(c) 20 mA (d) 100 mA

[ESE-2000]

8. Power Amplifiers and Regulators

8.1 If a class *C* power amplifier has an input signal with frequency of 200 kHz and the width of collector current pulses of 0.1 μs, then the duty cycle of the amplifier will be
(a) 1 % (b) 2 %
(c) 10 % (d) 20 %
[ESE-1999]

8.2 Thermal runaway will take place if the quiescent point is such that
(a) $V_{CE} > 1/2\ V_{CC}$ (b) $V_{CE} < V_{CC}$
(c) $V_{CE} < 2\ V_{CC}$ (d) $V_{CE} < 1/2\ V_{CC}$
[ESE-1999]

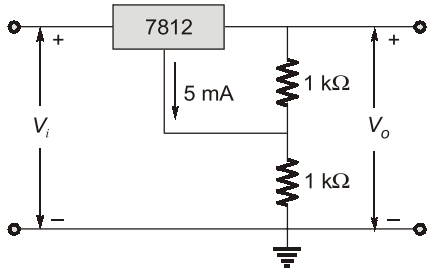
8.3 To avoid thermal runway in the design of an analog circuit, the operating point of the BJT should be such that it satisfies the condition
(a) $V_{CE} = V_{CE}/2$ (b) $V_{CE} \le V_{CE}/2$
(c) $V_{CE} > V_{CE}/2$ (d) $V_{CE} \le 0.78\ V_{CE}$
[ESE-1999]

8.4 The unit of a thermal resistance of a semiconductor device is
(a) Ohms (b) Ohms/°C
(c) °C/Ohm (d) °C/Watt
[ESE-1999]

8.5 In a feedback series regulator circuit, the output voltage is regulated by controlling the
(a) magnitude of the input voltage
(b) gain of the feedback transistor
(c) reference voltage
(d) voltage drop across the series pass transistor
[ESE-1999]

8.6 A three-terminal monolithic IC regulator can be used as
(a) an adjustable output voltage regulator alone
(b) an adjustable output voltage regulator and a current regulator
(c) a current regulator and a power switch
(d) a current regulator alone
[ESE-1999]

8.7 A 12 V monolithic regulator is adjusted to obtain a higher output voltage as shown in the given figure



The V_0 will be
(a) 12 V (b) 17 V
(c) 24 V (d) 29 V **[ESE-1999]**

8.8 The input voltage of Zener regulator varies from 20 V to 30 V. The load current varies from 10 mA to 15 mA. If the Zener voltage is 5 V, the value of series resistor will be
(a) 1 kΩ (b) 1.5 kΩ
(c) 1.66 kΩ (d) 2.5 kΩ
[ESE-2000]

8.9 The thermal run-away in a CE transistor amplifier can be prevented by biasing the transistor in such a manner that
(a) $V_{CE} > \frac{V_{CC}}{2}$ (b) $V_{CE} < \frac{V_{CC}}{2}$
(c) $V_{CE} = \frac{V_{CC}}{2}$ (d) $V_{CE} = 0$
[ESE-2000]

8.10 Consider the following statements:
Sziklai pair
1. is also called complementary Darlington.
2. acts like a single p-n-p transistor with a very high current gain.
3. can be used in class *B* push-pull power amplifier.

Which of these statements are correct?
(a) 1 and 2 (b) 1 and 3
(c) 2 and 3 (d) 1, 2 and 3
[ESE-2000]

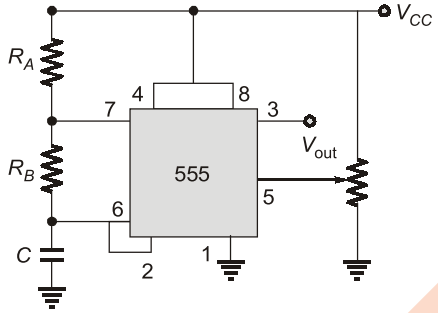
8.11 Which one of the following power amplifiers has the maximum efficiency?
(a) Class *A* (b) Class *B*
(c) Class *AB* (d) Class *C* **[ESE-2000]**

8.12 Thermal runaway is not possible in FET because as the temperature of FET increases
(a) the mobility decreases
(b) the transconductance increases
(c) the drain current increases
(d) the mobility increases **[ESE-2001]**

9. Multivibrators and Timers

9.1 **Assertion (A):** A monostable multivibrator can be used to alter the pulse width of a repetitive pulse train.
Reason (R): Monostable multivibrator has a single stable state.
(a) Both A and R are true and R is the correct explanation of A
(b) Both A and R are true but R is NOT the correct explanation of A
(c) A is true but R is false
(d) A is false but R is true **[ESE-1999]**

9.2 Circuit shown in the given figure represents



(a) an astable multivibrator
(b) a monostable multivibrator
(c) voltage-controlled oscillator
(d) ramp generator **[ESE-1999]**

9.3 A 1 ms pulse can be stretched to 1 s pulse by using
(a) an astable multivibrator
(b) a monostable multivibrator
(c) a bistable multivibrator
(d) a Schmitt trigger circuit **[ESE-2000]**

9.4 Which one of the following sets of circuits can be obtained by using a 555 timer?
(a) Pulse modulator and amplitude demodulator
(b) Pulse modulator and astable multivibrator
(c) Amplitude demodulator and AC to DC converter
(d) AC to DC converter and astable multivibrator **[ESE-2000]**

■■■

Answers Analog Circuits

1.1	(d)	1.2	(c)	2.1	(c)	2.2	(d)	2.3	(d)	2.4	(c)	2.5	(a)	2.6	(*)	2.7	(a)		
2.8	(c)	2.9	(d)	2.10	(d)	2.11	(a)	2.12	(b)	2.13	(b)	3.1	(a)	4.1	(a)	4.2	(c)		
4.3	(d)	4.4	(b)	4.5	(c)	4.6	(a)	5.1	(a)	5.2	(b)	5.3	(a)	5.4	(b)	6.1	(d)		
6.2	(b)	6.3	(b)	7.1	(c)	7.2	(d)	7.3	(c)	7.4	(d)	7.5	(a)	7.6	(a)	7.7	(*)		
7.8	(a)	8.1	(b)	8.2	(a)	8.3	(b)	8.4	(d)	8.5	(d)	8.6	(a)	8.7	(d)	8.8	(a)		
8.9	(b)	8.10	(b)	8.11	(d)	8.12	(a)	9.1	(b)	9.2	(c)	9.3	(b)	9.4	(b)				

Explanations Analog Circuits

1. Diodes Circuits

1.1 (d)

For full wave rectifier,

$$I_{dc} = \frac{2I_m}{\pi}$$

$$I_{rms} = \frac{I_m}{\sqrt{2}}$$

$$\frac{P_{dc}}{P} = \frac{(I_{dc})^2 R}{(I_{rms})^2 R} = \frac{\left(\frac{2I_m}{\pi}\right)^2}{\left(\frac{I_m}{\sqrt{2}}\right)^2} = \frac{8}{\pi^2}$$

1.2 (c)

$$\tau = R_L C = T_{OFF}$$
$$T = T_{ON} + T_{OFF}$$

- when C increases, T_{OFF} increases and T_{ON} decreases. Hence Conduction period decreases.
- Larger value of capacitor requires larger current to charge it.

2. BJT Circuits

2.2 (d)

$$g_m = \frac{I_D}{V_i}$$

In the figure, $I_E = I_D$ and $I_C = \alpha I_E$

$$g_{m_{overall}} = \frac{I_c}{V_i} = \frac{\alpha I_E}{V_i} = \frac{\alpha I_D}{V_i} = \alpha g_m$$

$$\Rightarrow \quad g_{m_{overall}} = \frac{\beta}{\beta+1} \cdot g_m = \frac{99}{99+1} \times 2$$

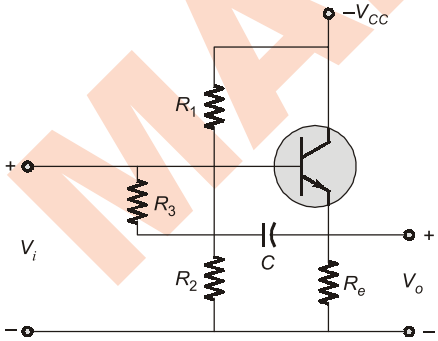
$$= 1.98 \text{ mA/V}$$

2.3 (d)

In bootstrapping, $A_v \to 1$, and effective input resistance becomes extremely large as

$$R_{eff} = \frac{R_3}{1 - A_v}$$

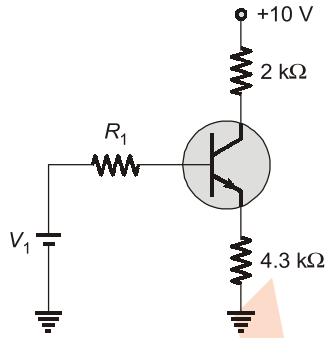
Thus the most effective way to increase the input resistance is through bootstrapping and the least effective way is to reduce the bias current.



2.4 (c)

$$V_1 = \frac{20}{20+20} \times 10 = 5 \text{ V}$$

$$R_1 = \frac{20 \times 20}{20+20} = 10 \text{ k}\Omega$$



KVL:

$$V_1 = R_1 I_B + V_{BE} + 4.3 I_E$$

Let $\beta > 1$. So $I_B \approx 0$ & $I_E \approx I_C$

$$V_1 = V_{BE} + 4.3 I_C$$

$$\Rightarrow \quad 5 - 0.7 = 4.3 I_C$$

$$\Rightarrow \quad I_C = 1 \text{ mA}$$

$$V_C = 10 - 2 \times 1$$

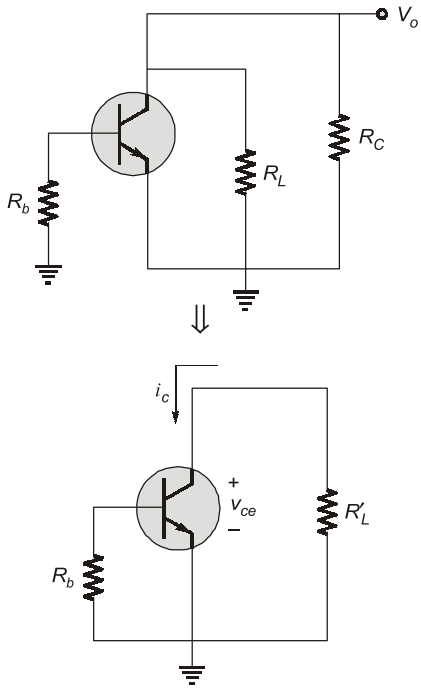
$$\Rightarrow \quad V_C = 8 \text{ V}$$

2.5 (a)

The increasing order of impedance is given below:
BJT (CB) < BJT (CE) < JFET < MOSFET.

2.7 (a)

AC equivalent of the circuit is



KVL in collector loop

$$i_c = -\frac{1}{R_L'} v_{CE}$$

$$= -\frac{1}{R_L'}(v_{CE} - v_{CEQ})$$

(Total, DC)

$$\text{Slope} = -\frac{1}{R_L'} = -\left[\frac{1}{R_L} + \frac{1}{R_C}\right]$$

2.9 (a)

$$V_{Th} = \frac{12 \times 30}{90} = 4\text{ V}$$

$$I_C \simeq \frac{V_{Th} - V_{BE}}{R_E} = \frac{4 - 0.7}{3.3\text{ k}\Omega} = 1\text{mA}$$

$$g_m = \frac{I_C}{V_T} = 40\text{ m}\mho$$

$$= g_m R_C = 40 \times 4 = 160$$

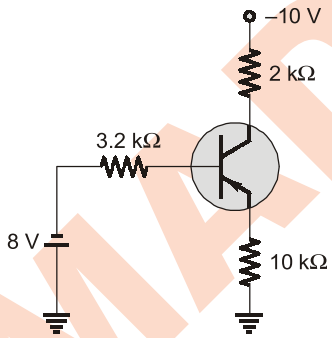
2.10 (d)

In the bootstrap biasing arrangement, voltage gain $A_v \to 1$ but not exactly equal to 1 that's why the input impedance is very high and the output impedances is not equal to zero.

(Since β is not given, we assume β to be very large).

2.11 (a)

Equivalent circuit is shown below:



Hence by approximate analysis we get,

Let $I_B \approx 0$

$V_B = -8$ V

$V_E = V_{EB} + V_B$

$\Rightarrow V_E = 0.7 + (-8)$

$\Rightarrow V_E = -7.3$ V

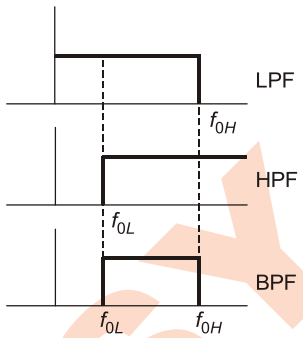
3. FET and MOSFET Circuits

3.1 (a)

FET exhibits no offset voltage at zero drain current, and hence makes an excellent signal chopper.

4. Frequency Response of Amplifiers & Filters

4.1 (a)



It is clear from the diagram that to make a bandpass filter $f_{0H} > f_{0L}$

4.2 (c)

For the RC–coupled amplifier, the drop at low frequencies is due to the increasing reactance of the coupling capacitors i.e. C_C, C_E, or C_S while its upper frequency limit is determined by either the parasitic capacitive elements of the network and frequency dependence of the gain of the active device.

4.4 (b)

$$Q = \frac{f_0}{\text{BW}} \Rightarrow \text{BW} \propto \frac{1}{Q}$$

5. Feedback Amplifiers

5.1 (a)

$$A_{v_f} = \frac{A_v}{1 + A_v\beta}$$

when $\beta >> 1$, $A_{v_f} \cong \frac{A_v}{A_v\beta} = \frac{1}{\beta}$

Thus, gain A_{v_f} is independent of A_v.

Note: Return difference, $D = 1 + A_v\beta$.

5.2 (b)

$$\beta = \frac{V_f}{V_0} = \frac{-I_C R_E}{I_C R_C} = \frac{-R_E}{R_C}$$

5.3 (a)

$A = 100$

$A_f = 20$

$$A_f = \frac{A}{1 + A\beta}$$

$$20 = \frac{100}{1+100\beta}$$

$$\Rightarrow \quad 1 + 100\beta = 5$$

$$\Rightarrow \quad \beta = \frac{4}{100} \times 100 = 4\ \%$$

6. Oscillators

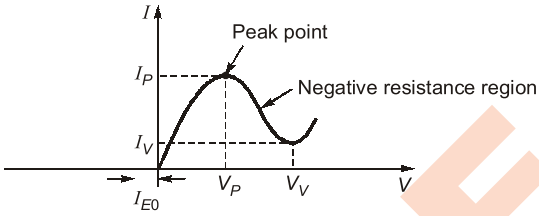
6.2 (b)

RF oscillators ($f > 20$ kHz) — Hartley, Colpitt, Clapp, Crystal

AF oscillators ($f < 20$ kHz) — RC phase shift, Wein bridge

6.4 (a)

UJT characteristic curve:



7. Operational Amplifiers

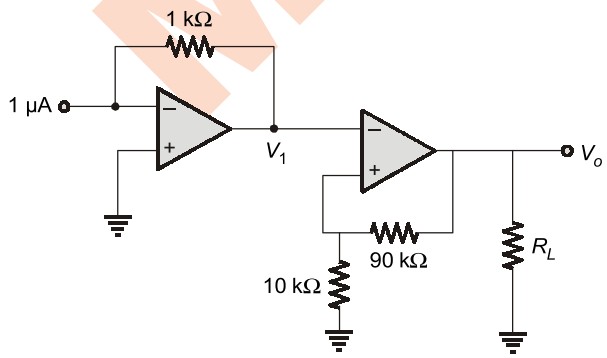
7.1 (c)

The output offset voltage

$$V_{OOV} = (A_{OO})V_{iO} + R_F I_B$$

where A_{OO} depends on β and I_B.

7.2 (d)



$$V_1 = \frac{10}{10+90} \cdot V_0$$

$$\Rightarrow \quad V_1 = \frac{V_0}{10}$$

$$V_1 = -1 \times 10^3 \times 1 \times 10^{-6}$$

$$\Rightarrow \quad \frac{V_0}{10} = -10^{-3}$$

$$\Rightarrow \quad V_0 = -10\ \text{mV}$$

7.3 (c)

$$80\ \text{dB} = 20 \log A_v$$

$$\Rightarrow \quad A_v = 10^4$$

GBW product $= 10^4 \times 20 = 200$ kHz

7.4 (d)

$$V_0 = -\frac{10}{1} \cdot V_i + V_i\left(\frac{10}{10+1}\right)\left(1+\frac{10}{1}\right)$$

$$\Rightarrow \quad V_0 = -10V_i + 10V_i\left(\frac{10}{11}\right)(11)$$

$$\Rightarrow \quad V_0 = -10\ V_i + 10\ V_i = 0$$

7.5 (a)

$\therefore$ Gain $\propto$ transconductance. Device having low transconductance will have low value of gain.

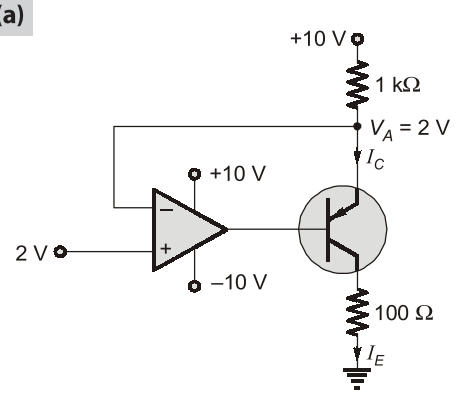
7.7 (*)

$$V_o(s) = \frac{-\frac{1}{Cs}}{R}V_i(s) + \frac{\frac{1}{Cs}}{R+\frac{1}{Cs}}\left(1+\frac{\frac{1}{Cs}}{R}\right)V_i(s)$$

$$\frac{V_o(s)}{V_i(s)} = -\frac{1}{RCs} + \left(\frac{1}{1+RCs}\right)\left(\frac{RCs+1}{RCs}\right) = 0$$

Hence the given circuit will not pass any signal at any frequency.

7.8 (a)



Using virtual ground $V_A = 2$ V

Current flowing through 1 kΩ resistor

$$= \frac{10-2}{1k} = 8\ \text{mA}$$

Since no current flows through op-amp

$$I_E \simeq I_C \simeq 8\ \text{mA}$$

8. Power Amplifiers and Regulators

8.1 (b)

Time period,

$$T = \frac{1}{f} = \frac{1}{200 \times 10^3} = 5 \times 10^{-6} = 5\,\mu\text{sec}$$

Pulse width $\tau = 0.1\ \mu$ sec

$$\text{Duty cycle} = \frac{\tau}{T} \times 100 = \frac{0.1}{5} \times 100 = 2\%$$

8.2 (a)

To avoid thermal runway,

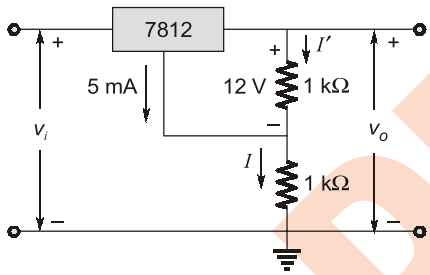
$$V_{CE} < \frac{V_{CC}}{2}$$

8.3 (b)

To avoid thermal runaway,

$$V_{CE} < V_{CC}/2$$

8.7 (d)



Output of IC 7812 is + 12 V.

$$I' = \frac{12}{1\text{k}\Omega} = 12\,\text{mA}$$

Using KCL

$\therefore \quad I = 5 + I' = 17$ mA

So $\quad V_o = 12 + 1 \times 17 = 29$ V

8.8 (a)

Zener diode should have minimum current, i.e., $I_Z(\text{min}) = 0$

$$R = \frac{V_i(\text{min}) - V_z}{I_z(\text{min}) + I_L(\text{max})} = \frac{20 - 5}{(0 + 15)10^{-3}}$$

$R = 1\ \text{k}\Omega$

8.9 (b)

To prevent thermal runway,

$$V_{CE} < \frac{V_{CC}}{2}$$

8.11 (d)

Increasing order of efficiency:
Class A < Class AB < Class B < Class C

8.12 (a)

In FET, there are only majority charge carriers. On increasing temperature, their mobility decreases. So speed decreases and further increase in temperature does not occur due to the collision of charge carriers.

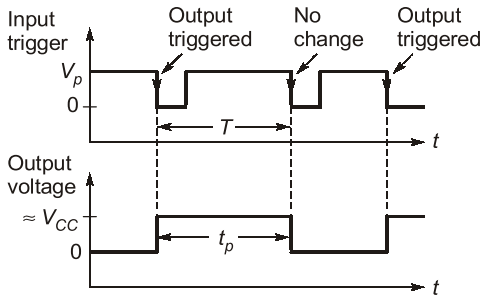
9. Multivibrators and Timers

9.1 (b)

Monostable multivibrator is used as pulse stretcher.

9.3 (b)

The output pulse width of the monostable multivibrator can be viewed as a stretched version of the narrow input pulse, hence the name pulse stretcher.



4 Digital Circuits

1. Number Systems

1.1 The minimum decimal equivalent of the number 11*C*.0 is

(a) 183 (b) 194

(c) 268 (d) 269 **[ESE-2000]**

2. Boolean Algebra

2.1 The Boolean theorem $AB + \bar{A}C + BC = AB + \bar{A}C$ corresponds to

(a) $(A + B).(\bar{A} + C).(B + C) = (A + B).(\bar{A} + C)$

(b) $AB + \bar{A}C + BC = AB + BC$

(c) $AB + \bar{A}C + BC = (A + B)(\bar{A} + C)(B + C)$

(d) $(A + B)(\bar{A} + C)(B + C) = AB + \bar{A}C$

[ESE-1999]

2.2 Karnaugh map is used to

(a) minimise the number of flip-flops in a digital circuit

(b) minimise the number of gates only in a digital circuit

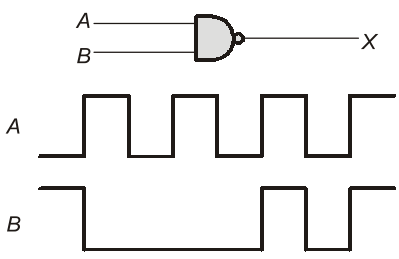
(c) minimise the number of gates and fan-in of a digital circuit

(d) design gates

[ESE-2000]

3. Logic Gates

3.1 The given figure shows a NAND gate with input waveforms *A* and *B*



The correct output waveform *X* of the gate is

(a)

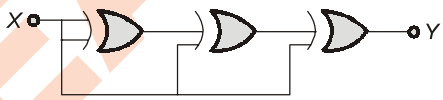
(b)

(c)

(d)

[ESE-1999]

3.2 The output *Y* of the given circuit is



(a) 1 (b) zero

(c) *X* (d) $\bar{X}$ **[ESE-1999]**

3.3 $Y = f(A, B) = \Pi M\ (0, 1, 2, 3)$ represents (*M* is Maxterm)

(a) NOR gate

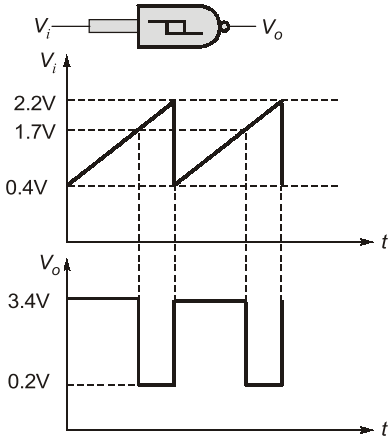
(b) NAND gate

(c) OR gate

(d) a situation where output is independent of input

[ESE-1999]

3.4 The input waveform V_i and the output wave-form V_0 of a Schmitt NAND are shown in the given figures. The duty cycle of the output waveform will be

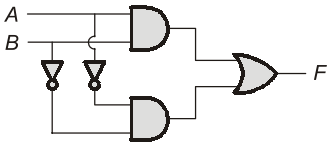


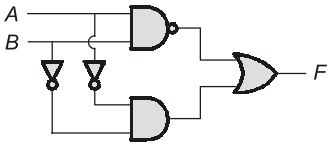
(a) 100% (b) 85.5%

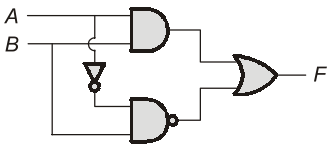
(c) 72.2% (d) 25% **[ESE-1999]**

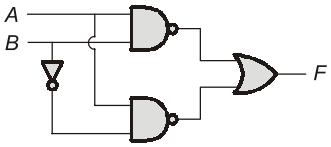
3.5 $(FE35)_{16}$ XOR $(CB15)_{16}$ is equal to
(a) $(3320)_{16}$ (b) $(FF35)_{16}$
(c) $(FF50)_{16}$ (d) $(3520)_{16}$ **[ESE-2000]**

3.6 Which one of the following figures represents the coincidence logic?

(a) 

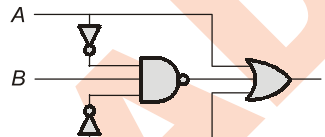
(b) 

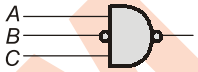
(c) 

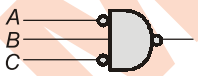
(d) 

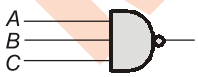
[ESE-2000]

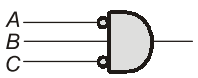
3.7 Which one of the following circuits is the minimised logic circuit for the circuit shown in figure below?



(a) 

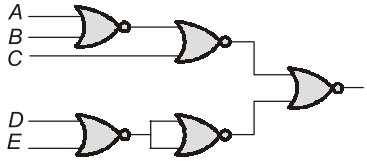
(b) 

(c) 

(d) 

[ESE-2000]

3.8 The circuit shown in the given figure realizes the function



(a) $(\overline{A+B}+C)(\bar{D}\bar{E})$ (b) $(\overline{A+B}+C)(D\bar{E})$
(c) $(A+\overline{B+C})(\bar{D}E)$ (d) $(A+B+\bar{C})(\bar{D}\bar{E})$
[ESE-2000]

3.9 The logic operations of two combinational circuits given in Figure-I and Figure-II are

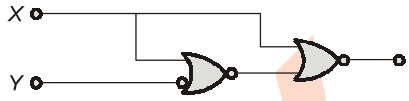


Figure I

Figure II

(a) entirely different (b) identical
(c) complementary (d) dual **[ESE-2000]**

4. Combinational Circuits

4.1 **Assertion (A):** A demultiplexer can be used as a decoder.
Reason (R): A demultiplexer is built by using AND gates only.
(a) Both A and R are true and R is the correct explanation of A
(b) Both A and R are true but R is NOT the correct explanation of A
(c) A is true but R is false
(d) A is false but R is true **[ESE-1999]**

4.2 Match **List-I** (Circuits) with **List-II** (Types of integration level) and select the correct answer using the codes given below the lists:

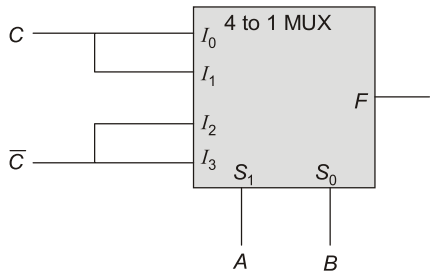
List-I	List-II
A. Full adder	**1.** VLSI
B. Magnitude comparator	**2.** SSI
C. Programmable logic array	**3.** MSI

Codes:

	A	B	C
(a)	2	3	1
(b)	3	2	1
(c)	1	3	2
(d)	2	1	3

[ESE-1999]

4.3 The logic circuit realized by the circuit shown in the given figure will be



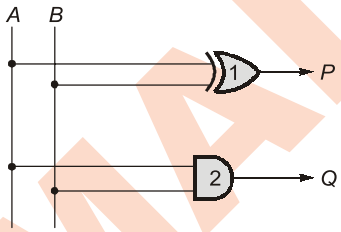
(a) $B \odot C$ (b) $F = B \oplus C$
(c) $A \odot C$ (d) $F = A \oplus C$

[ESE-1999]

4.4 Which one of the following statements correctly defines the full-adder?
An adder circuit
(a) having two inputs used to add two binary digits. It produces their sum and carry as output.
(b) having three inputs used to add two binary digits plus a carry. It produces their sum and carry as outputs.
(c) used in the least significant position when adding two binary digits with no carry-in to consider. It produces their sum and carry as outputs.
(d) having two inputs and two outputs.

[ESE-2000]

4.5 The half-adder circuit in the given figure has inputs $AB = 11$



The logic level of P and Q outputs will be
(a) $P = 0$ and $Q = 0$ (b) $P = 0$ and $Q = 1$
(c) $P = 1$ and $Q = 0$ (d) $P = 1$ and $Q = 1$

[ESE-2000]

4.6 Which one of the following can be used as parallel to series converter?
(a) Decoder (b) Digital counter
(c) Multiplexer (d) Demultiplexer

[ESE-2000]

4.7 Consider the following statements:
A multiplexer
1. selects one of the several inputs and transmits it to a single output
2. routes the data from a single input to one of many output
3. converts parallel data into serial data
4. is a combinational circuit

Which of these statements are correct?
(a) 1, 2 and 4 (b) 2, 3, and 4
(c) 1, 3 and 4 (d) 1, 2 and 3

[ESE-2000]

5. Sequential Circuits

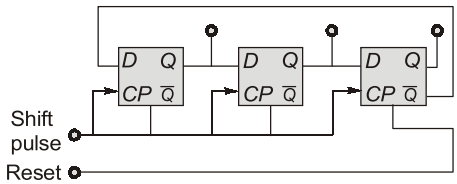
5.1 In a negative edge triggered *J-K* flip-flop, in order to have the output Q state 0, 0 and 1 in the next three successive clock pulses, the *J-K* input states required would be respectively
(a) 00, 00 and 10 (b) 00, 01 and 11
(c) 00, 10 and 11 (d) 01, 10 and 11

[ESE-1999]

5.2 The initial state of *MOD*-16 down counter is 0110. After 37 clock pulses, the state of the counter will be
(a) 1011 (b) 0110
(c) 0101 (d) 0001

[ESE-1999]

5.3 A three-bit shift register is shown in the given figure



To have the content '000' again, the number of clock pulses required would be
(a) 3 (b) 6
(c) 8 (d) 16 **[ESE-1999]**

5.4 Symmetrical square wave of time period 100 μs can be obtained from square wave of time period 10 μs by using a
(a) divide by-5 circuit
(b) divide by-2 circuit
(c) divide by-5 circuit followed by a divide by-2 circuit
(d) *BCD* counter **[ESE-1999]**

5.5 A 1 μs pulse can be converted into a 1ms pulse by using
(a) a monostable multivibrator
(b) an astable multivibrator
(c) a bistable multivibrator
(d) a *J-K* flip-flop **[ESE-1999]**

5.6 **Assertion (A):** Synchronous counter has higher speed of operation than ripple counter.
Reason (R): Synchronous counter uses high speed flip-flops.
(a) Both A and R are true and R is the correct explanation of A
(b) Both A and R are true but R is NOT the correct explanation of A
(c) A is true but R is false
(d) A is false but R is true **[ESE-2000]**

5.7 **Assertion (A):** A ring counter is preferred over a binary sequential counter.
Reason (R): The decoding logic is simple for a ring counter.
(a) Both A and R are true and R is the correct explanation of A
(b) Both A and R are true but R is NOT the correct explanation of A
(c) A is true but R is false
(d) A is false but R is true
[ESE-2000]

5.8 A *T*-flip-flop function is obtained from a *JK* flip-flop. If the flip-flop belongs to a *TTL* family, the connection needed at the input must be
(a) $J = K = 1$ (b) $J = K = 0$
(c) $J = 1$ and $K = 0$ (d) $J = 0$ and $K = 1$
[ESE-2000]

5.9 Consider the following statements:
1. Race around condition occurs in a *JK* flip-flop when both the inputs are one
2. A flip-flop is used to store one bit of information
3. A transparent latch consists of a *D*-type flip-flop
4. Master-slave configuration is used in flip-flops to store two bits of information

Which of these statements are correct?
(a) 1, 2 and 3 (b) 1, 3 and 4
(c) 1, 2 and 4 (d) 2, 3 and 4
[ESE-2000]

5.10 A ring counter consisting of five flip-flops will have
(a) 5 states (b) 10 states
(c) 32 states (d) infinite states
[ESE-2000]

5.11 A crystal oscillator is frequently used in digital circuits for timing purposes because of its
(a) low cost
(b) high frequency stability
(c) simple circuitry
(d) ability to set the frequency at the desired value
[ESE-2000]

6. Memories and Programmable Logic Devices

6.1 For a particular type of memory, the access time and the cycle time are respectively 200 ns and 200 ns. The maximum rate at which the data can be accessed, is
(a) 2.5×10^6 /s (b) 5×10^6 /s
(c) 0.2×10^6 /s (d) 10^6 /s
[ESE-1999]

6.2 Which one of the following statements is correct?
(a) RAM is a non-volatile memory whereas ROM is a volatile memory
(b) RAM is a volatile memory whereas ROM is a non-volatile memory
(c) Both RAM and ROM are volatile memories but in ROM data is not lost when power is switched off
(d) Both RAM and ROM are non-volatile memories but in RAM data is lost when power is switched off
[ESE-2000]

6.3 Match **List-I** (Memory elements) with **List-II** (Properties) and select the correct answer using the codes given below the lists:

List-I
A. Semiconductor memory
B. Ferrite core memory
C. Magnetic tape memory

List-II
1. Destructive read out
2. Combinational logic
3. Volatile

Codes:

	A	B	C
(a)	2	1	3
(b)	1	3	2
(c)	3	2	1
(d)	3	1	2

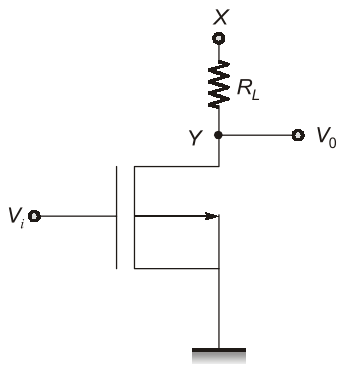
[ESE-2000]

7. Logic Families

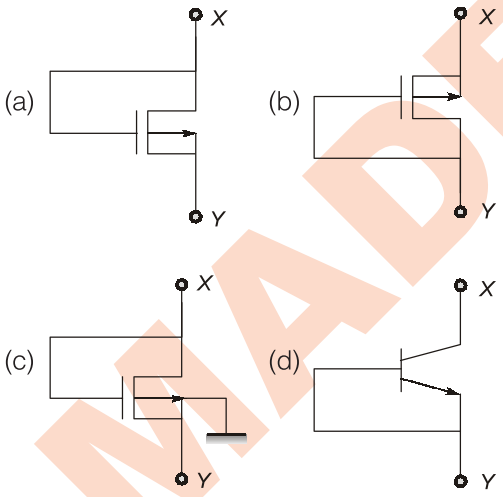
7.1 The voltage levels of a negative logic system
(a) must necessarily be negative
(b) may be negative or positive
(c) must necessarily be positive
(d) must necessarily be 0 V and –5 V

[ESE-1999]

7.2 The load resistance R_L between X and Y in the switch shown in Figure-I



CANNOT be replaced by



[ESE-1999]

7.3 Consider the following statements regarding *IC*s:
1. ECL has the least propagation delay.
2. TTL has the largest fanout.
3. CMOS has the biggest noise margin.
4. TTL has the lowest power consumption.

Which of these statements are correct?
(a) 1 and 3 (b) 2 and 4
(c) 3 and 4 (d) 1 and 2

[ESE-1999]

7.4 For a logic family
V_{OH} is the minimum output high level voltage
V_{OL} is the maximum output low level voltage
V_{IH} is the minimum acceptable input high level voltage
V_{IL} is the maximum acceptable input low level voltage
The correct relationship among these is
(a) $V_{IH} > V_{OH} > V_{IL} > V_{OL}$
(b) $V_{OH} > V_{IH} > V_{IL} > V_{OL}$
(c) $V_{IH} > V_{OH} > V_{OL} > V_{IL}$
(d) $V_{OH} > V_{IH} > V_{OL} > V_{IL}$

[ESE-1999]

7.5 **Assertion (A):** Schottky transistors are preferred over normal transistors in digital circuits.
Reason (R): Schottky transistors operate in active and saturation region.
(a) Both A and R are true and R is the correct explanation of A
(b) Both A and R are true but R is NOT the correct explanation of A
(c) A is true but R is false
(d) A is false but R is true

[ESE-2000]

7.6 The figure of merit of a logic family is given by
(a) Gain × Bandwidth
(b) Propagation delay time × Power dissipation
(c) Fan-out × Propagation delay time
(d) Noise margin × Power dissipation

[ESE-2000]

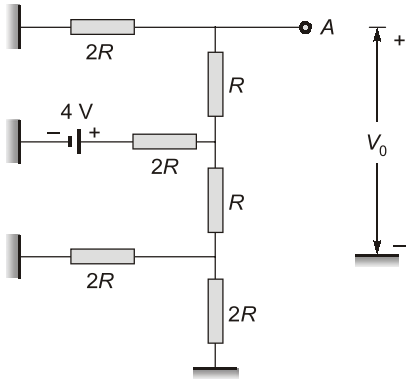
8. ADC and DAC

8.1 **Assertion (A):** The output of an 8-bit A to D converter is 80H for an input of 2.5 V.
Reason (R): ADC has an output range of 00 to FFH for an input range of –5 V to + 5 V.
(a) Both A and R are true and R is the correct explanation of A
(b) Both A and R are true but R is NOT the correct explanation of A
(c) A is true but R is false
(d) A is false but R is true

[ESE-1999]

8.2 The output voltage V_0 with respect to ground of the *R-2R* ladder network shown in the given figure is

(a) 1 V (b) 2 V
(c) 3 V (d) 4 V [ESE-1999]



Answers Digital Circuits

1.1	(b)	2.1	(a)	2.2	(b)	3.1	(d)	3.2	(b)	3.3	(d)	3.4	(c)	3.5	(d)	3.6	(a)		
3.7	(b)	3.8	(a)	3.9	(a)	4.1	(b)	4.2	(b)	4.3	(d)	4.4	(b)	4.5	(b)	4.6	(c)		
4.7	(c)	5.1	(a, b)	5.2	(d)	5.3	(b)	5.4	(c)	5.5	(a)	5.6	(c)	5.7	(a)	5.8	(a)		
5.9	(a)	5.10	(a)	5.11	(b)	6.1	(d)	6.2	(b)	6.3	(a)	7.1	(b)	7.2	(d)	7.3	(a)		
7.4	(b)	7.5	(c)	7.6	(b)	8.1	(d)	8.2	(a)										

Explanations Digital Circuits

1. Number Systems

1.1 (b)

Let the base be x.
Decimal value = $1 \cdot x^2 + 1 \cdot x + 12 \cdot x^0$
Taking base $x = 13$,
$13^2 + 13 + 12 = 194$

2. Boolean Algebra

2.1 (a)

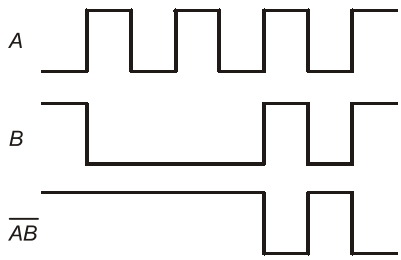
$AB + \bar{A}C + BC = AB + \bar{A}C$
Taking dual of the given equation
$(A + B)(\bar{A} + C)(B + C) = (A + B)(\bar{A} + C)$

2.2 (b)

Karnaugh map provides a simple straight forward procedure for minimizing Boolean functions and hence the number of gates to realize the Boolean function are minimized.

3. Logic Gates

3.1 (d)



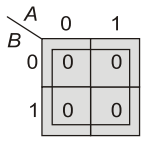
3.2 (b)

$Y = X \oplus [X \oplus \{X \oplus X\}]$
$\Rightarrow \quad Y = X \oplus [X \oplus 0]$
$\Rightarrow \quad Y = X \oplus X$
$\Rightarrow \quad Y = 0$

3.3 (d)

$Y = f(A, B) = \Pi M(0, 1, 2, 3)$

K-map for Y:



If all the cells in a maxterms *K*-map are grouped, this means that the output y is equal to 0 for every possible input.

$y = 0$ which represents a situation where output is independent of input.

3.4 (c)

$$\text{Duty cycle} = \frac{T_{on}}{T} \times 100$$

$$= \frac{(1.7-0.4)}{(2.2-0.4)} \times 100 \times 100$$

$$= 72.2\%$$

3.5 (d)

$(FE35)_{16} \oplus (CB15)_{16}$ converting to binary

$= (1111\ 1110\ 0011\ 0101)_2 \oplus (1100\ 1011\ 0001\ 0101)_2$

$= (0011\ 0101\ 0010\ 0000)_2$ converting to Hex.

$= (3520)_{16}$

Truth table for XOR gate is

A	B	$A \oplus B$
0	0	0
0	1	1
1	0	1
1	1	0

3.6 (a)

EX-NOR logic is also called coincidence logic.

$F = AB + \bar{A}\bar{B}$.

3.7 (b)

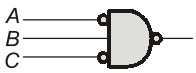
$$F = A + \overline{\bar{A}B\bar{C}} + C$$

or $$F = A + A + \bar{B} + C + C$$

or $$F = A + \bar{B} + C$$

or $$F = \overline{\bar{A}B\bar{C}}$$

Therefore, the given circuit can be minimised as below:



3.8 (a)

$$F = \overline{\overline{A+B+C} + \overline{D+E}}$$

or $$F = (\overline{A+B}+C)\overline{(D+E)}$$

or $$F = (\overline{A+B}+C)(\bar{D}\bar{E})$$

3.9 (a)

In Figure I,

$$F_1 = \overline{\overline{(X+\bar{Y})} + X}$$

$$= (X+\bar{Y})\bar{X} = \bar{X}\bar{Y}$$

In Figure II,

$$F_2 = X\bar{Y}$$

Thus, the logic operations of two combinational circuits are entirely different.

4. Combinational Circuits

4.3 (d)

$$F = \bar{A}\bar{B}C + \bar{A}BC + A\bar{B}\bar{C} + AB\bar{C}$$

$$\Rightarrow F = \bar{A}C(\bar{B}+B) + A\bar{C}(\bar{B}+B)$$

$$\Rightarrow F = \bar{A}C + A\bar{C}$$

$$\because \bar{B}+B = 1$$

$$\Rightarrow F = A \oplus C$$

4.5 (b)

$A = 1, B = 1$

$P = A \oplus B = A\bar{B} + \bar{A}B = 0$

$Q = AB = 1$

4.6 (c)

Multiplexer can be used as parallel to series converter.

5. Sequential Circuits

5.1 (a, b)

Characteristic Table for *JK* flip-flop is

J	K	$Q(t+1)$	
0	0	$Q(t)$	Hold state
0	1	0	Reset state
1	0	1	Set state
1	1	$\overline{Q(t)}$	Toggle state

5.2 (d)

$37 = 16 \times 2 + 5$

After 37 clock pulses, the state of MOD-16 DOWN counter will be five states below the present state.

$$\begin{array}{r} 0110 \\ -0101 \\ \hline 0001 \end{array}.$$

5.3 (b)

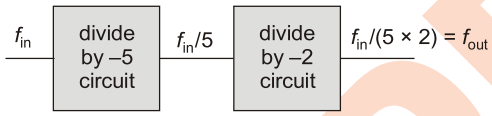
The given circuit is a switch-tail ring counter or Johnson counter in which n flip-flops provide 2n distinguishable states. Therefore, 3 flip-flops will provide 6 states.

5.4 (c)

Output frequency $f_{out} = \dfrac{1}{100\ \mu s}$

Input frequency $f_{in} = \dfrac{1}{10\ \mu s}$

$f_{out} = \dfrac{f_{in}}{10}$



5.5 (a)

A monostable multivibrator is used as a pulse stretcher.

5.8 (a)

For a *JK*-flip-flop to function as *T*-flip-flop, $J = K$. If the flip-flop belongs to a *TTL* family, then $J = K = 1$.

5.9 (a)

Master-slave configuration is used in flip-flops to store one bit of information.

5.10 (a)

A ring counter consisting of n flip-flips will have n states.

5.11 (b)

A crystal oscillator has high frequency stability.

6. Memories and Programmable Logic Devices

6.2 (b)

RAM is a volatile memory which means that RAM loses the stored information when power is turned off. ROM is a non-volatile memory which means that ROM retains the stored information when the power is turned off.

7. Logic Families

7.1 (b)

The voltage levels of a negative logic system may be negative or positive provided voltage level of logic 1 < voltage level of logic 0.

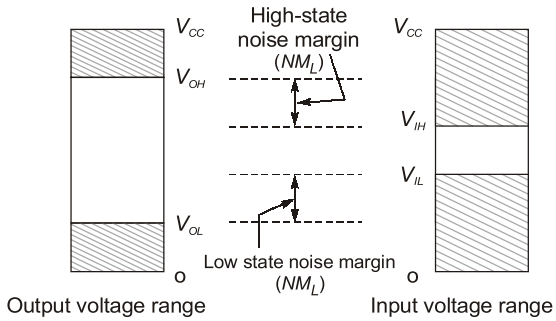
7.2 (d)

One advantage of the MOS device is that it can be used not only as a switch, but as a resistor as well. A resistor is obtained from the MOS by permanently biasing the gate terminal for conduction, the resistance of the conduction channel thus created effectively acts as load resistance. In MOS, channel resistance, $R \propto \dfrac{1}{W/L}$ where W and L are the width and length of the channel respectively.

7.3 (a)

(i) CMOS has the largest fan-out.
(ii) CMOS has the lowest power consumption.

7.4 (b)



7.5 (c)

Schottky transistors are prevented from entering saturation to reduce the propagation delay time. Therefore, they are preferred over normal transistors in digital circuits.

7.6 (b)

Figure of merit (pJ) = Propagation delay time (ns) × Power dissipation (mW)

8. ADC and DAC

8.1 (d)

$(FFH)_{16} = (255)_{10}$

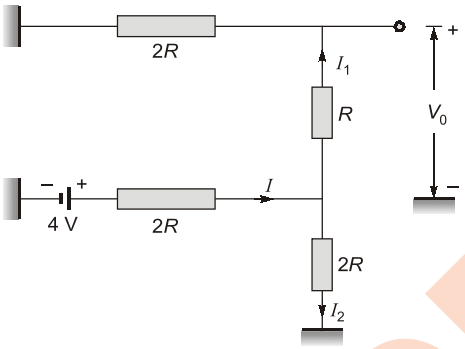
$(80H)_{16} = (128)_{10}$

Input for the output of 80H is

$$-5 + \frac{128}{255} \times [5 - (-5)], \text{ i.e. } 0 \text{ V.}$$

8.2 (a)

The equivalent circuit is shown:



$2R.I + (R + 2R).I_1 = 4$

$I_1 + I_2 = I$ and $3I_1 = 2I_2$

$$\Rightarrow \quad I_1 + \frac{3}{2}I_1 = I$$

$$\Rightarrow \quad I = 2.5\, I_1$$

$$\Rightarrow \quad 2R(2.5I_1) + 3RI_1 = 4$$

$$\Rightarrow \quad 8RI_1 = 4$$

$$\Rightarrow \quad I_1 = \frac{4}{8R} = \frac{1}{2R}$$

$$\Rightarrow \quad V_0 = 2R.I_1$$

$$= 2R \cdot \frac{1}{2R} = 1 \text{ V}$$

■■■

5 Materials Science

1. Crystalline Structures

1.1 The difference between the number of atoms in a unit cell of a BCC crystal and an FCC crystal is
(a) 1 (b) 2
(c) 4 (d) 6 **[ESE-2000]**

2. Dielectric and Ceramic Materials

2.1 Consider the following statements regarding an insulating material connected to an a.c. signal:
1. The dielectric constant increases with frequency
2. The dielectric constant decreases with frequency
3. Atomic polarization decreases with frequency

Which of these statement(s) is/are correct?
(a) 3 alone (b) 2 alone
(c) 2 and 3 (d) 1 and 3
[ESE-1999]

2.2 The most important set of specifications of transformer oil includes
(a) dielectric strength and viscosity
(b) dielectric strength and flash point
(c) flash point and viscosity
(d) dielectric strength, flash point and viscosity
[ESE-1999]

2.3 **Assertion (A) :** A uniaxial stress on the ends of a piezoelectric crystal develops a potential difference between the two ends of the crystal.
Reason (R) : The ions in the crystal get displaced and produce dipoles.
(a) Both A and R are true and R is the correct explanation of A
(b) Both A and R are true but R is NOT the correct explanation of A
(c) A is true but R is false
(d) A is false but R is true **[ESE-1999]**

2.4 For an insulating material, dielectric strength and dielectric loss should be respectively
(a) high and high (b) low and high
(c) high and low (d) low and low
[ESE-2000]

2.5 **Assertion (A):** $BaTiO_3$ is a piezoelectric material and is used in a record player.
Reason (R): In a piezoelectric transducer, stress induces polarization and an electric field strains the material.
(a) Both A and R are true and R is the correct explanation of A
(b) Both A and R are true but R is NOT the correct explanation of A
(c) A is true but R is false
(d) A is false but R is true
[ESE-2000]

3. Magnetic Materials

3.1 The magnetic moment in units of Bohr magnetron of a ferrous ion in any ferrite is
(a) zero (b) 2
(c) 4 (d) 6
[ESE-1999]

3.2 For a permanent magnetic material
(a) the residual induction and the coercive field should be large
(b) the residual induction and the coercive field should be small
(c) the area of hysteresis loop should be small
(d) the initial relative permeability should be large
[ESE-1999]

3.3 Match **List-I** (Magnetic materials) with **List-II** (Dipole arrangement in external field) and select the correct answer using the codes given below the lists:

List-I
A. Paramagnetic
B. Ferromagnetic
C. Antiferromagnetic
D. Ferrimagnetic

List-II
1. All dipoles are aligned in one preferred direction and have equal magnitudes
2. Half of the dipoles are aligned in opposite direction and have equal magnitudes
3. Half of the dipoles (with equal magnitudes) are aligned in opposite direction to other half having equal but lower magnitudes
4. All dipoles have equal magnitudes but are randomly oriented

Codes:

	A	B	C	D
(a)	4	3	2	1
(b)	4	1	2	3
(c)	2	1	4	3
(d)	2	3	4	1

[ESE-2000]

3.4 **Assertion (A):** Alnico is commonly used for electromagnets.
Reason (R): Alnico has low hysteresis loss.
(a) Both A and R are true and R is the correct explanation of A
(b) Both A and R are true but R is NOT the correct explanation of A
(c) A is true but R is false
(d) A is false but R is true

[ESE-2000]

4. Conductors and Superconductors

4.1 The magnetization '*M*' of a superconductor in a field of *H* is
(a) extremely small (b) $-H$
(c) -1 (d) zero [ESE-1999]

4.2 The maximum power handling capacity of a resistor depends on
(a) total surface area
(b) resistance value
(c) thermal capacity of the resistor
(d) resistivity of the material used in the resistor

[ESE-1999]

4.3 If a small amount of Cu is added to a Ni conductor, then the
(a) resistivity of Ni will increase at all temperatures because Cu is a better conductor than Ni
(b) residual resistivity of Ni at low temperature will increase as Cu atoms act as defect centres
(c) resistivity of Ni will increase at all temperatures as Cu destroys the periodicity of Ni and acts as defects
(d) resistivity of Ni remains unaltered as Cu atoms give the same number of free electrons as Ni atoms.

[ESE-2000]

4.4 Which one of the following is the best definition of a superconductor?
(a) It is a material showing perfect conductivity and Meissner effect below a critical temperature
(b) It is a conductor having zero resistance
(c) It is a perfect conductor with highest diamagnetic susceptibility
(d) It is a perfect conductor but becomes resistive when the current density through it exceeds a critical value

[ESE-2000]

■■■

Answers Materials Science

1.1	(b)	2.1	(c)	2.2	(d)	2.3	(a)	2.4	(c)	2.5	(a)	3.1	(c)	3.2	(a)	3.3	(b)		
3.4	(c)	4.1	(b)	4.2	(c)	4.3	(c)	4.4	(a)										

Explanations Materials Science

1. Crystalline Structures

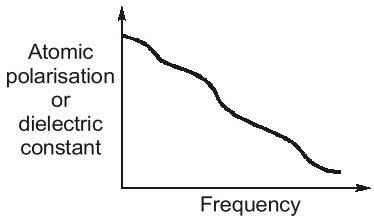
1.1 (b)

Number of atoms in a unit cell of BCC crystal = 2
Number of atoms in a unit cell of FCC crystal = 4
Difference = 4 – 2 = 2

2. Dielectric and Ceramic Materials

2.1 (c)

In an insulating material connected to an a.c. signal, the dielectric constant and atomic polarisation decrease with frequency.



2.3 (a)

In piezoelectric crystals, the mechanical strain may produce an electrostatic charge on the faces of the crystal because the ions in the crystal get displaced and produce dipoles.

2.4 (c)

A good insulating material should have:
- A low dissipation factor.
- High insulation resistance.
- Good dielectric strength.
- High mechanical strength.
- High thermal conductivity.

3. Magnetic Materials

3.1 (c)

Ferrous ion (Fe^{2+}) has electron configuration
$1s^2\ 2s^2\ 2p^6\ 3s^2\ 3p^6\ 4s^2\ 3d^4$

3d shell | 1 | 1 | 1 | 1 | 0 |

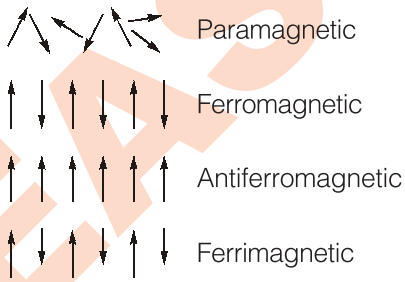
Since number of unpaired electrons = 4
Therefore, magnetic moment
= 4 Bohr magnetron

3.2 (a)

Permanent magnetic materials are those which retain a considerable amount of their magnetic energy after the magnetizing force has been removed, i.e. the materials which are difficult to demagnetize. Therefore for a permanent magnetic material, the residual induction and coercive field should be large.

3.3 (b)

The arrangement of dipole moments in different magnetic materials is shown below



3.4 (c)

Alnico has high hysteresis loss.

4. Conductors and Superconductors

4.1 (b)

In superconductor, $B = 0$
or $\mu(H + M) = 0$
$\Rightarrow \quad M = -H$

4.2 (c)

Maximum power handling capacity of a resistor depends on thermal capacity of the resistor.

4.3 (c)

$$\rho_{alloy} = \rho_{pure\ metal} + s \cdot \rho_i$$

where s is atomic percentage of added impurity and ρ_i is increase in resistivity per atomic percentage.

■■■

6 Electronic Measurements and Instrumentation

1. Basics of Measurement and Error Analysis

1.1 Loading effect is primarily caused by instruments having
(a) high resistance (b) high sensitivity
(c) low sensitivity (d) high range
[ESE-1999]

1.2 The difference between the measured value and the true value is called
(a) gross error (b) relative error
(c) probable error (d) absolute error
[ESE-1999]

1.3 A 300 V full-scale deflection voltmeter has an accuracy of ±2%, when it reads 222 V. The actual voltage
(a) lies between 217.56 V and 226.44 V
(b) lies between 217.4 V and 226.6 V
(c) lies between 216 V and 228 V
(d) is exactly 222 V **[ESE-1999]**

1.4 An ammeter of range 0-25 A has a guaranteed accuracy of 1% of full-scale reading. The current measured by the ammeter is 5 A. The limiting error in the reading is
(a) 2% (b) 2.5%
(c) 4% (d) 5% **[ESE-2000]**

1.5 "The current internationally recognised unit of time and frequency is based on the Caesium clock, which gives an accuracy better than 1 μs per day." This statement is related to
(a) Working standards
(b) International standards
(c) Primary standards
(d) Secondary standards **[ESE-2000]**

2. Analog Systems for Measurements

2.1 Measurement of an unknown voltage with a dc potentiometer loses its advantage of open-circuit measurement when
(a) the primary circuit battery is changed
(b) standardization has to be done again to compensate for drifts
(c) voltage is larger than the range of the potentiometer
(d) range reduction by a factor of 10 is employed
[ESE-1999]

2.2 Match **List-I** with **List-II** and select the correct answer using the codes given below the lists:

List-I
A. Former
B. Coil
C. Core
D. Spring

List-II
1. Produces deflecting torque
2. Provides base for the coil
3. Makes the magnetic field radial
4. Provides controlling torque

Codes:

	A	B	C	D
(a)	1	2	3	4
(b)	1	2	4	3
(c)	2	1	3	4
(d)	2	1	4	3

[ESE-1999]

2.3 If the secondary winding of a current transformer opened while the primary winding is carrying current, then
(a) the transformer will burn immediately
(b) there will be weak flux density in the core
(c) there will be a very high induced voltage in the secondary winding
(d) there will be a high current in the secondary winding
[ESE-1999]

2.4 **Assertion (A):** The needle of an indicating instrument attains a position where deflecting and control torques acting on the moving system are equal and opposite.

Reason (R): The oscillations of the needle are suppressed by the damping mechanism.

(a) Both A and R are individually true and R is the correct explanation of A
(b) Both A and R are individually true but R is not the correct explanation of A
(c) A is true but R is false
(d) A is false but R is true [ESE-1999]

2.5 Match **List-I** (Instrument) with **List-II** (Property/use) and select the correct answer using the codes given below the lists:

List-I
A. PMMC
B. Moving iron
C. Thermocouple
D. Electrostatic type

List-II
1. Square law type scale
2. Very good high frequency response
3. Linear scale over the entire range
4. Voltmeter

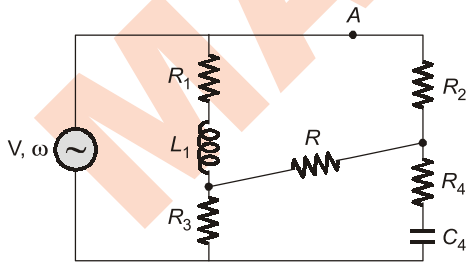
Codes:

	A	B	C	D
(a)	4	1	2	3
(b)	3	2	1	4
(c)	4	2	1	3
(d)	3	1	2	4

[ESE-2000]

3. Bridge Measurements and Q-meter

3.1 In the circuit shown in the figure, if the current in resistance '*R*' is Nil, then



(a) $\frac{\omega L_1}{R_1} = \frac{1}{\omega C_4 R_4}$

(b) $\frac{\omega L_1}{R_1} = \omega C_4 R_4$

(c) $\tan^{-1}\frac{\omega L_1}{R_1} + \tan^{-1}\omega C_4 R_4 = 0$

(d) $\tan^{-1}\frac{\omega L_1}{R_1} + \tan^{-1}\frac{1}{\omega C_4 R_4} = 0$

[ESE-1999]

3.2 Consider the following operations in respect of a Wheatstone bridge:
(Key "K_b" ; is used for the supply battery and Key "K_g" is used for the galvanometer)

1. Open K_b
2. Close K_g
3. Close K_b
4. Open K_g

The correct sequence of these operations is

(a) 1, 2, 3, 4 (b) 3, 1, 2, 4
(c) 4, 3, 2, 1 (d) 3, 2, 4, 1

[ESE-1999]

3.3 A coil is tuned to resonance at 1 MHz with a resonating capacitance of 72 pF. At 500 kHz, the resonance is obtained with a resonating capacitance value of 360 pF. The self-capacitance of the coil is

(a) 12 pF (b) 24 pF
(c) 36 pF (d) 72 pF

[ESE-1999]

3.4 Match **List-I** (Bridges) with **List-II** (Parameters) and select the correct answer using the codes given below the lists:

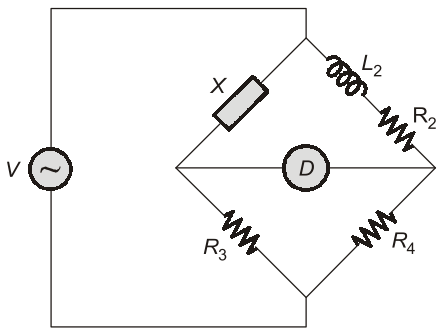
List-I	List-II
A. Anderson bridge	**1.** Low Resistance
B. Kelvin Bridge	**2.** Medium Resistance
C. Schering Bridge	**3.** Inductance
D. Wheatstone Bridge	**4.** Capacitance

Codes:

	A	B	C	D
(a)	4	2	3	1
(b)	3	2	4	1
(c)	3	1	4	2
(d)	4	1	3	2

[ESE-1999]

3.5 In the balanced bridge shown in the figure, '*X*' should be



(a) a self-inductance having resistance
(b) a capacitance
(c) a non-inductive resistance
(d) an inductance and a capacitance in parallel

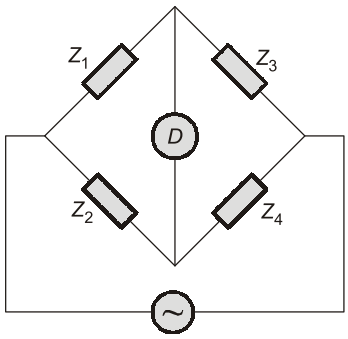
[ESE-1999]

3.6 While using Maxwell bridge, the Q factor of a coil is obtained as

(a) $1/\omega CR$ (b) ωCR
(c) $\omega C/R$ (d) $R/\omega C$

[ESE-1999]

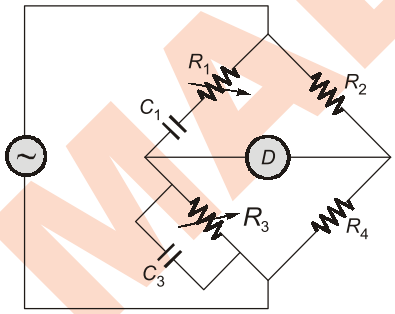
3.7 The a.c. bridge shown in the figure is balanced if $Z_1 = 100\ \angle 30°$; $Z_2 = 150\ \angle 0°$; $Z_3 = 250\ \angle -40°$ and Z_4 is equal to



(a) $350\ \angle 70°$ (b) $375\ \angle -70°$
(c) $150\ \angle 0°$ (d) $150\ \angle 20°$

[ESE-1999]

3.8 The Wein bridge circuit shown in the figure below can be used as a frequency measuring device, provided



(a) $R_2/R_4 = 2$ (b) $R_4/R_2 = 2$
(c) $R_2/R_4 = 4$ (d) $R_2/R_4 = 3$

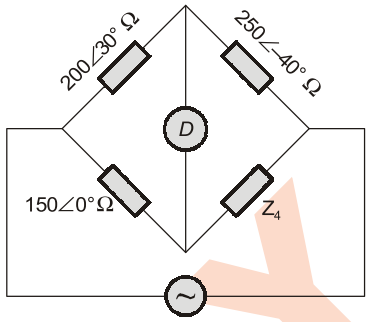
[ESE-2000]

3.9 The equations under balance condition for a bridge are $R_1 = R_2 R_3/R_4$ and $L_1 = R_2 R_3 C_4$ where R_1 and L_1 are unknown quantities. Which one of the following sets of parameters should be chosen as variables in order to achieve converging balance?

(a) R_2 and R_3 (b) R_2 and C_4
(c) R_4 and C_4 (d) R_3 and C_4

[ESE-2000]

3.10 At the balance condition of the A.C. bridge shown in the figure below, the value of Z_4 would be



(a) $120\ \angle 70°\ \Omega$ (b) $187.5\ \angle -10°\ \Omega$
(c) $187.5\ \angle -70°\ \Omega$ (d) $333.3\ \angle -70°\ \Omega$

[ESE-2000]

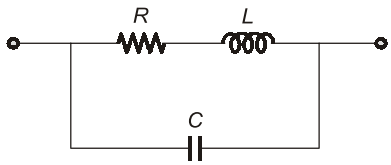
3.11 Wagner's earth in A.C. bridge circuits is used to eliminate the effect of

(a) stray electrostatic fields
(b) stray electromagnetic fields
(c) inter-component capacitances
(d) parasitic capacitance to earth

[ESE-2000]

4. Power and Energy Measurement

4.1 The equivalent circuit of a resistor is shown in the given figure. The resistor will be non-inductive if



(a) $R = L/C$ (b) $R = \sqrt{L/C}$
(c) $L = CR^2$ (d) $C = LR^2$

[ESE-1999]

4.2 Consider the following statements:
A 3-phase balanced supply system is connected to a 3-phase unbalanced load. Power supplied to this load can be measured using

1. two wattmeters
2. one wattmeter
3. three wattmeters

Which of these statement(s) is/are correct?

(a) 1 and 2 (b) 1 and 3
(c) 2 and 3 (d) 3 alone

[ESE-2000]

5. Cathode Ray Oscilloscope (CRO)

5.1 A dual-trace CRO has
(a) one electron gun
(b) two electron guns
(c) one electron gun and one two-pole switch
(d) two electron guns and one two-pole switch
[ESE-1999]

5.2 The bandwidth of a CRO is from 0 to 20 MHz. The fastest rise time which a square wave can have, in order that it is accurately reproduced by the CRO is
(a) 0.175 μs (b) 17.5 ns
(c) 35 ns (d) 52.5 ns **[ESE-2000]**

5.3 **Assertion (A):** CRTs, used in TV receivers are of electrostatic deflection type and those used in oscilloscopes are of magnetic deflection type.
Reason (R): TV receivers need a large screen to view pictures, whereas accuracy is the main consideration in oscilloscopes.
(a) Both A and R are individually true and R is the correct explanation of A
(b) Both A and R are individually true but R is not the correct explanation of A
(c) A is true but R is false
(d) A is false but R is true **[ESE-2000]**

5.4 A d.c. voltage of 1 V is applied to the *X*-plates of a CRO and an a.c. voltage 2 sin100t is applied to the *Y*-plates. The resulting display on the CRO screen will be a
(a) vertical straight line
(b) horizontal straight line
(c) sine wave
(d) slant line **[ESE-2000]**

6. Digital System for Measurement

6.1 A $3\frac{1}{2}$ digit voltmeter having a resolution of 100 mV can be used to measure maximum voltage of
(a) 100 V (b) 200 V
(c) 1000 V (d) 5000 V **[ESE-1999]**

6.2 Consider the following statements:
1. Use of digital computers along with transducers makes data manipulation easier.
2. Digital signals are not dependent on signal amplifiers and so are easy to transmit without distortion and external noise.
3. Increased accuracy in pulse count is possible.
4. There are ergonomic advantages in presenting digital data.

The main advantages of digital transducers include
(a) 1, 2 and 4 (b) 1, 2 and 3
(c) 2, 3, and 4 (d) 1, 2, 3, and 4
[ESE-1999]

6.3 Harmonic distortion analyser
(a) measures the amplitude of each harmonic component
(b) measures the rms value of fundamental frequency component
(c) measures the rms value of all the harmonic components except the fundamental frequency component
(d) displays the rms value of each harmonic component on the screen of a CRO
[ESE-1999]

6.4 In a distortion factor meter, the filter at the front end is used to suppress
(a) odd harmonics
(b) even harmonics
(c) fundamental component
(d) dc component **[ESE-2000]**

7. Transducers

7.1 A Hall effect transducer can be used to measure
(a) displacement, temperature and magnetic flux
(b) displacement, position and velocity
(c) position, magnetic flux and pressure
(d) displacement, position and magnetic flux
[ESE-1999]

7.2 Load cell employs
(a) piezoelectric crystal
(b) capacitor
(c) mutual inductance
(d) strain gauges **[ESE-1999]**

7.3 **Assertion (A) :** The capacitive transducer is best suited for measurement of very small pressure differentials under dynamic conditions.
Reason (R) : The capacitance transducer can be excited by both dc and AC voltages.

(a) Both A and R are individually true and R is the correct explanation of A
(b) Both A and R are individually true but R is not the correct explanation of A
(c) A is true but R is false
(d) A is false but R is true [ESE-1999]

7.4 The device possessing the highest photosensitivity is a
(a) photoconductive cell
(b) photovoltaic cell
(c) photodiode
(d) phototransistor [ESE-1999]

7.5 Radiation pyrometers are used for the measurement of temperature in the range of
(a) –200°C to 500°C (b) 0°C to 500°C
(c) 500°C to 1200°C (d) 1200°C to 2500°C
[ESE-2000]

7.6 Magnetic flux can be measured by
(a) capacitive pick-up
(b) inductive pick-up
(c) resistive pick-up
(d) Hall-effect pick-up [ESE-2000]

7.7 A semiconductor based temperature transducer has temperature coefficient of –2500 μV/°C. This transducer indeed is a
(a) thermistor
(b) forward-biased pn junction diode
(c) reverse-biased pn junction diode
(d) FET [ESE-2000]

7.8 The function of the reference electrode in a pH meter is to
(a) produce a constant voltage
(b) provide temperature compensation
(c) provide a constant current
(d) measure average pH value
[ESE-2000]

7.9 Pirani gauge is used for the measurement of pressure in the range of
(a) 10^{-8} mm to 10^{-5} mm of Hg
(b) 10^{-3} mm to 10^{-1} mm of Hg
(c) 10 mm to 10^{3} mm of Hg
(d) 10^{5} mm to 10^{8} mm of Hg
[ESE-2000]

7.10 The most light sensitive transducer for conversion of light into electrical power is the
(a) photodiode
(b) solar cell
(c) photoconductive cell
(d) photovoltaic cell [ESE-2000]

8. Data Acquisition Systems and Telemetry Systems

8.1 A 5-channel dc to 60 Hz telemetry system uses PAM and PCM systems. For a good quality data transmission, the minimum sampling rate must be
(a) 300 samples/s (b) 500 samples/s
(c) 1500 samples/s (d) 1250 samples/s
[ESE-1999]

8.2 Which one of the following pairs of Modulation techniques and Telemetry situations and conditions is correctly matched?
(a) Pulse amplitude modulation : Low amplitude signals
(b) Pulse position modulation : For short distances when power is enough
(c) Pulse width modulation : Power to be spent in telemetry is required to be low
(d) Pulse code modulation : Minimisation of interference effects
[ESE-1999]

8.3 **Assertion (A):** Prescalers are used in digital counters to extend the frequency range.
Reason (R): Prescalers are simple dividing circuits and as such do not have the high frequency limitation of digital counters.
(a) Both A and R are individually true and R is the correct explanation of A
(b) Both A and R are individually true but R is not the correct explanation of A
(c) A is true but R is false
(d) A is false but R is true
[ESE-2000]

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Answers Electronic Measurements and Instrumentation

1.1	(c)	1.2	(d)	1.3	(c)	1.4	(d)	1.5	(c)	2.1	(c)	2.2	(c)	2.3	(c)	2.4	(b)
2.5	(d)	3.1	(a)	3.2	(d)	3.3	(b)	3.4	(c)	3.5	(a)	3.6	(b)	3.7	(b)	3.8	(a)
3.9	(c)	3.10	(c)	3.11	(d)	4.1	(b, c)	4.2	(b)	5.1	(c)	5.2	(b)	5.3	(d)	5.4	(a)
6.1	(a)	6.2	(b)	6.3	(c)	6.4	(c)	7.1	(d)	7.2	(d)	7.3	(c)	7.4	(b)	7.5	(d)
7.6	(d)	7.7	(b)	7.8	(a)	7.9	(b)	7.10	(d)	8.1	(*)	8.2	(d)	8.3	(a)		

Explanations Electronic Measurements and Instrumentation

1. Basics of Measurement and Error Analysis

1.1 (c)

Loading effect is primarily caused by instruments having low sensitivity.

1.2 (d)

Absolute error,

$$\delta A = A_m - A_t$$

where, A_m = measured value of quantity

A_t = true value of quantity

1.3 (c)

$$\text{Deflection} = \pm 300 \times \frac{2}{100} = \pm 6 \text{ V}$$

Therefore, the actual voltage = 222 ± 6 V Thus, actual voltage lies between 216 V and 228 V.

1.4 (d)

1% of 25 A = 0.25 A

$\therefore$ Absolute error

$\Rightarrow$ $\delta A = 0.25$ A and $A_s = 5$ A

$$\therefore \quad \text{limiting error} = \frac{\delta A}{A_s} \times 100$$

$$= \frac{0.25}{5} \times 100 = \pm 5\%$$

2. Analog Systems for Measurements

2.5 (d)

(i) In PMMC instruments, the scale is linear over the entire range.

(ii) Thermocouple is used for measurement of radio frequency a.c. signals.

(iii) In moving iron instruments have square law type scale.

3. Bridge Measurements and Q-meter

3.1 (a)

For the bridge to be a balanced, the condition should be

$$(R_1 + j\omega L_1)\left(R_4 + \frac{1}{j\omega C_4}\right) = R_2 R_3$$

On comparing real and imaginary part

$$R_1 R_4 + \frac{L_1}{C_4} = R_2 R_3 \qquad \ldots(i)$$

$$\frac{R_1}{j\omega C_4} + R_4 j\omega L_1 = 0 \qquad \ldots(ii)$$

$$\frac{\omega L_1}{R_1} = \frac{1}{\omega C_4 R_4}$$

3.2 (d)

The steps in the operation of a Wheatstone bridge are as follows:

(i) Close K_b (ii) Close K_g

(iii) Open K_g (iv) Open K_b

3.3 (b)

$$C_D = \frac{C_1 - n^2 C_2}{n^2 - 1}$$

$$n = 2$$

$$C_d = \frac{C_1 - 4C_2}{3} = \frac{360 - 4 \times 72}{3} = 24 \text{ pF}$$

3.4 (c)

(i) Anderson's bridge method is used to measure the self-inductance in terms of a standard capacitor.

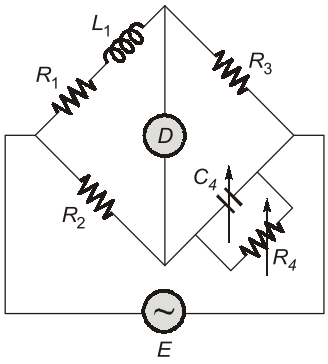
(ii) Kelvin's double bridge method is used for the measurement of low resistance.

(iii) Schering bridge is used to measure the capacitance.

3.5 (a)

The given circuit is Maxwell's inductance bridge.

3.6 (b)



Maxwell's Inductance–Capacitance bridge

At balance, $R_1 = \frac{R_2 R_3}{R_4}$

and $L_1 = C_4 R_2 R_3$

$$Q = \frac{\omega L_1}{R_1} = \omega C_4 R_4$$

3.7 (b)

$$Z_4 = \frac{Z_2 Z_3}{Z_1}$$

$$= \frac{150\angle 0^\circ \cdot 250\angle -40^\circ}{100\angle 30^\circ} = 375\angle -70^\circ$$

3.8 (a)

Under balance conditions,

$$\left(R_1 - \frac{j}{\omega C_1}\right) R_4 = \left(\frac{R_3}{1 + j\omega C_3 R_3}\right) R_2$$

or $$\frac{R_2}{R_4} = \frac{R_1}{R_3} + \frac{C_3}{C_1} + j\left(\omega C_3 R_1 - \frac{1}{\omega C_1 R_3}\right)$$

Equating real parts,

$$\frac{R_2}{R_4} = \frac{R_1}{R_3} + \frac{C_3}{C_1}$$

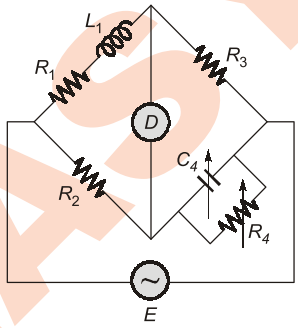
In most Wien bridges, the components are so chosen that $R_1 = R_3 = R$ and $C_1 = C_3 = C$.

So, the above equation reduces to

$$\frac{R_2}{R_4} = 2$$

3.9 (c)

The given bridge is Maxwell's inductance-capacitance bridge in which the two balance equations are independent if we choose R_4 and C_4 as variable elements.



Maxwell's Inductance–Capacitance bridge

The two balance equations are

$$R_1 = \frac{R_2 R_3}{R_4} \text{ and } L_1 = R_2 R_3 C_4$$

3.10 (c)

At the balance condition,

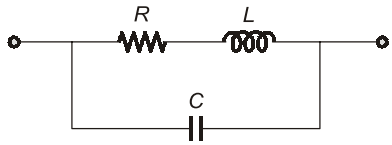
$$Z_4 = \frac{150\angle 0^\circ \cdot 250\angle -40^\circ}{200\angle 30^\circ} = 187.5\angle -70^\circ\ \Omega$$

3.11 (d)

Wagner's earthing device removes all the earth capacitances from the bridge network.

4. Power and Energy Measurement

4.1 (b, c)



Equivalent circuit of resistor

Equivalent impedance,

$$Z = \frac{(1/j\omega C)(R + j\omega L)}{R + j\omega L + (1/j\omega C)}$$

$$= \frac{R + j\omega (L - \omega^2 L^2 C - CR^2)}{1 + \omega^2 C^2 R^2 - 2\omega^2 LC + \omega^4 L^2 C^2}$$

So, the effective reactance,

$$X_{eff} = \frac{\omega\{L(1-\omega^2LC) - CR^2\}}{1+\omega^2C^2R^2 - 2\omega^2LC + \omega^4L^2C^2}$$

Since X_{eff} is small, we have, $\omega^2LC << 1$.

So, ω^2LC can be neglected.

$$\therefore \quad X_{eff} = \frac{\omega(L - CR^2)}{1+\omega^2C(CR^2 - 2L)}$$

If the resistance is non-inductive, then

$$L - CR^2 = 0$$

$$\Rightarrow \quad R = \sqrt{\frac{L}{C}}$$

4.2 (b)

One wattmeter method is used only for balanced load.

5. Cathode Ray Oscilloscope (CRO)

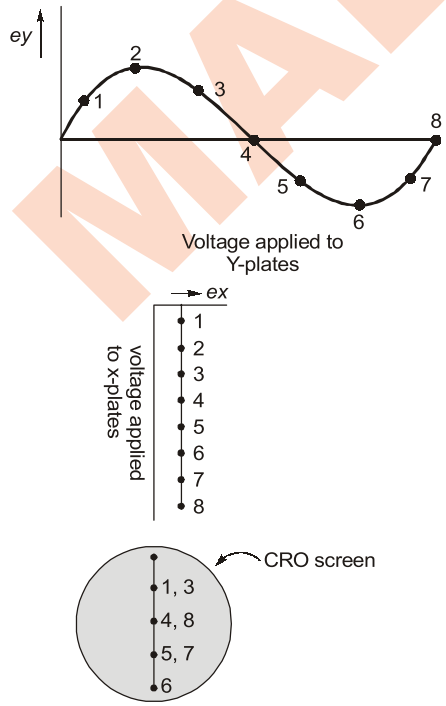
5.2 (b)

$$\text{Rise time, } t_r = \frac{0.35}{\text{Bandwidth}} = \frac{0.35}{20\times10^6} = 17.5 \text{ ns}$$

5.3 (d)

The CRO uses electrostatic method of focusing as compared to a TV picture tube which employs electromagnetic focusing.

5.4 (a)



6. Digital System for Measurement

6.1 (a)

$$\text{Resolution} = \frac{V_{FS}}{10^n}$$

where, V_{FS} = Full scale voltage

So, n = Number of full digital = 3

$$100 \text{ mV} = \frac{V_{FS}}{10^3} \Rightarrow V_{FS} = 100 \text{ V}$$

6.3 (c)

Harmonic distortion analyser is used to measure the total harmonic distortion (THD).

$$\text{THD} = \frac{\left[\Sigma(\text{Harmonics})^2\right]^{1/2}}{\text{Fundamental}}$$

$$\text{or THD} = \sqrt{\left(\frac{E_2}{E_1}\right)^2 + \left(\frac{E_3}{E_1}\right)^2 + \ldots} = \frac{\sqrt{E_2^2 + E_3^2 + \ldots}}{E_1}$$

where, E_n = amplitude of nth harmonic

E_1 = amplitude of fundamental

7. Transducers

7.1 (d)

The principle of Hall effect is that if a specimen (metal or semiconductor) carrying a current I is placed in a transverse magnetic field B, an electric field E is induced in the direction perpendicular to both I and B.

Hall effect transducer can be used to measure

(i) Magnetic flux (ii) Displacement

(iii) Current (iv) Power

(v) Position

7.2 (d)

Load cells utilize an elastic member as the primary transducer and strain gauges as secondary transducers.

7.3 (c)

The capacitance transducer can be excited only by AC voltages.

7.6 (d)

Magnetic flux (ϕ) = BA

Where magnetic field B can be measured with the help Hall effect as

$$B = \frac{V_H \cdot W}{I \cdot R_H}$$

7.8 **(a)**

In a pH meter, the reference electrode is at a constant voltage regardless of the pH value of the solution under test.

8. Data Acquisition Systems and Telemetry Systems

8.1 **(*)**

Minimum sampling rate

$= 2nf_m$

$= 2 \times 5 \times 60$

$= 600$ samples/s

So, in the given options, option (d) is the most suitable.

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