CLASS TEST S.No.:01SK_JKLMNOPQ_14092025

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ANALOG ELECTRONICS

ELECTRICAL ENGINEERING

Date of Test : 14/09/2025

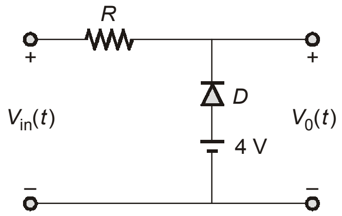
ANSWER KEY

1.	(b)	7.	(c)	13.	(b)	19.	(c)	25.	(b)
2.	(b)	8.	(d)	14.	(a)	20.	(a)	26.	(b)
3.	(c)	9.	(d)	15.	(c)	21.	(a)	27.	(c)
4.	(a)	10.	(c)	16.	(b)	22.	(a)	28.	(b)
5.	(a)	11.	(a)	17.	(c)	23.	(b)	29.	(d)
6.	(b)	12.	(a)	18.	(d)	24.	(c)	30.	(a)

DETAILED EXPLANATIONS

1. (b)

The circuit can be redrawn as



Case (I): when $V_{in}(t) > 4$ V

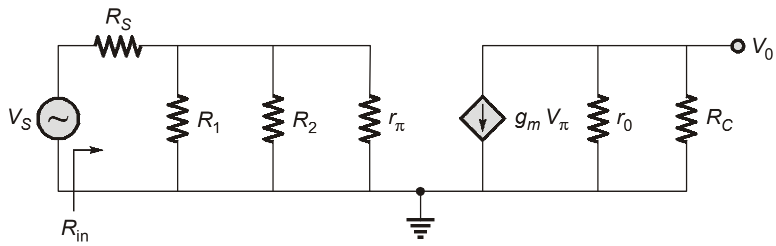
The diode D will be in OFF state and $V_{in}(t) = V_0(t)$.

Case (II): when $V_{in}(t) < 4$ V

The diode D will be in ON state and $V_{out}(t) = 4$ V.

2. (b)

By drawing the small signal equivalent model of the transistor by deactivating all the supply voltages, we get,



Now, the resistance seen by the source is equal to,

$$R_{in} = R_s + (R_1 \| R_2 \| r_\pi)$$

$$r_\pi = 2.74 \text{ k}\Omega \quad \text{(given)}$$

Thus,
$$R_{in} = 0.5\times 10^3 + (2.74\text{k} \| 93.7\text{k} \| 6.3\text{k})$$

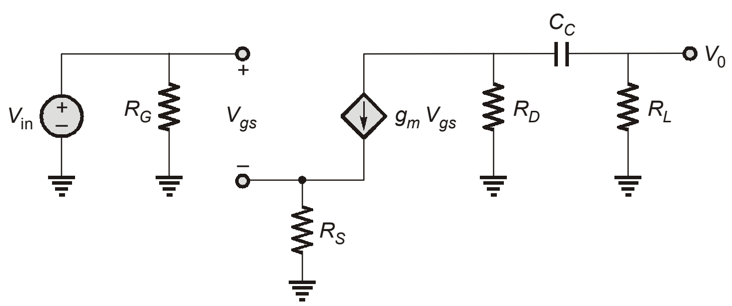
$$= (0.5 + 1.87) \times 10^3\ \Omega = 2.37 \text{ k}\Omega$$

3. (c)

The three figures are equivalent except in the first figure the resistance R_1 should have been a parallel combination of R_1 and R_2 and in the second figure the direction of dependent current source is not correct for the V_π polarity.

4. (a)

The small signal equivalent of the circuit can be drawn as,



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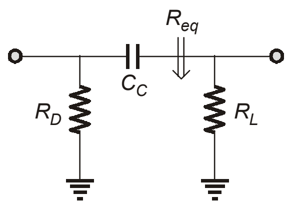
Now, the time constant for capacitor C_C can be calculated by short circuiting the input voltage source thus the resultant circuit becomes



$$\therefore \quad \tau_S = R_{eq}\, C_C = (R_D + R_L)\, C_C$$

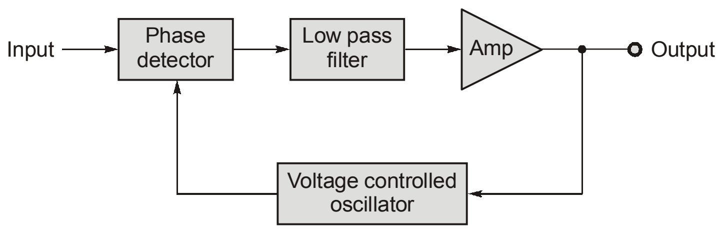
$$\therefore \quad f_L = \frac{1}{2\pi(R_D + R_L)C_C}$$

$$\Rightarrow \quad C_C = \frac{1}{2\pi(R_D + R_L)\, f_L} = \frac{1}{2\pi(6.7 + 10)\times 10^3 \times 20}$$

$$C_C = 0.477\ \mu\text{F}$$

5. (a)

The basic mode of a phase lock loop can be represented as

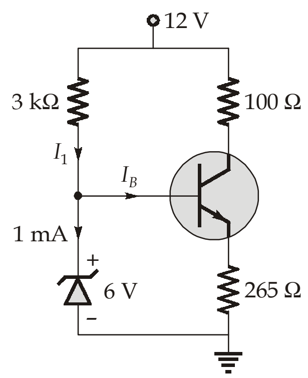


6. (b)

The current through base resistor,

$$I_B = I_1 - 1\text{ mA}$$

$$= \frac{6}{3\text{k}} - 1\text{ mA} = 1\text{ mA}$$



Apply KVL in base circuit,

$$-6 + 0.7 + 265\,(1 + \beta)I_B = 0$$

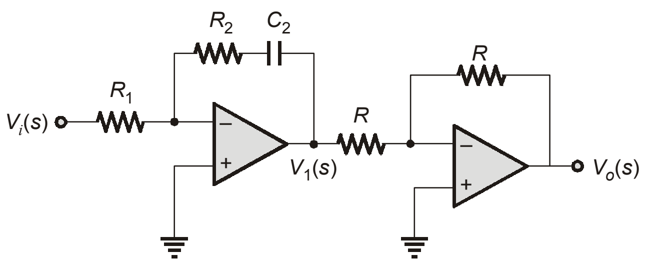
$$265\,(1 + \beta)I_B = 5.3$$

$$(1 + \beta) = \frac{5.3}{265 \times 10^{-3}}$$

$$1 + \beta = \frac{5.3}{0.265}$$

$$\beta = 20 - 1 = 19$$

7. (c)



$$\frac{V_1(s)}{V_i(s)} = -\frac{R_2 + \frac{1}{sC_2}}{R_1}$$

$$\frac{V_o(s)}{V_1(s)} = -\frac{R}{R} = -1$$

So,
$$\frac{V_o(s)}{V_i(s)} = \frac{R_2}{R_1} + \frac{1}{sR_1C_2} = \frac{R_2}{R_1}\left(1 + \frac{1}{s\tau}\right); \quad \tau = R_2 C_2$$

$$= K\left(1 + \frac{1}{s\tau}\right)$$

It works as proportional + Integral controller.

8. (d)

$$I_{D1} = I_{D2} = K_n(V_{GS} - V_t)^2$$

$$I_D = \frac{\mu_n C_{ox}}{2} \cdot \frac{W}{L}(V_{GS} - V_t)^2$$

$$= 0.1\,(5 - 2)^2 = 0.9 \text{ mA}$$

9. (d)

In the given circuit, the feedback resistor RF is not directly connected to the output node and directly connected to the input node. Hence, the feedback topology present in the circuit is Current - Shunt.

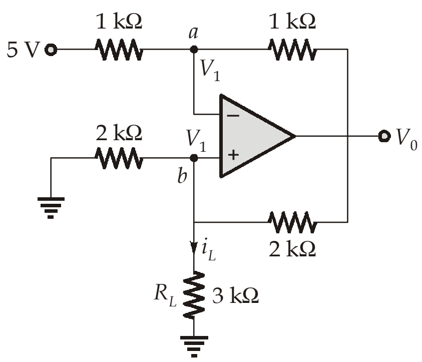
Current - Shunt topology is also known as Shunt - Series topology.

10. (c)

Voltage gain,
$$\frac{V_0}{V_{in}} \approx \frac{-h_{fe} \cdot R_C}{h_{ie}}$$

$$A_V \approx \frac{-150 \times 3\text{ k}\Omega}{3\text{ k}\Omega} \approx -150$$

11. (a)



Apply KCL at node '*a*'

$$\frac{5 - V_1}{1} = \frac{V_1 - V_0}{1}$$

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$$5 - V_1 = V_1 - V_0$$
$$-V_0 = 5 - 2V_1$$
$$V_0 = 2V_1 - 5 \quad \text{...(i)}$$

Apply KCL at node '*b*'

$$\frac{V_1}{2} + \frac{V_1}{3} + \frac{V_1 - V_0}{2} = 0$$
$$V_1\left[\frac{1}{2} + \frac{1}{3} + \frac{1}{2}\right] = \frac{V_0}{2}$$
$$V_1\left[\frac{4}{3}\right] = \frac{V_0}{2}$$
$$V_1 = \frac{3}{8}V_0 \quad \text{...(ii)}$$

From equation (i) and (ii), we get

$$V_1 = \frac{3}{8}(2V_1 - 5)$$
$$8V_1 = 6V_1 - 15$$
$$2V_1 = -15$$
$$V_1 = -7.5 \text{ Volt}$$

Load current, $i_L = \frac{V_1}{3K} = \frac{-7.5}{3K} = -2.5 \text{ mA}$

12. **(a)**

For upper MOSFET,

$$V_{DS} = 8 - V_a$$
$$V_{GS} - V_T = 6 - V_a - 2 = 4 - V_a$$

Upper MOS will be in saturation because

$$V_{DS} > V_{GS} - V_T$$

For lower MOS, $V_{DS} = V_a$

$$V_{GS} - V_T = V_a - 2$$

So, $V_{DS} > V_{GS} - V_T$

Hence both MOS will be in saturation

$$I_D = \mu_n C_{ox}\left(\frac{W}{L}\right)(V_{GS} - V_T)^2$$
$$I_{D1} = \mu_n C_{ox}(9)(4 - V_a)^2$$
$$I_{D2} = \mu_n C_{ox}(4)(V_a - 2)^2$$

But $I_{D1} = I_{D2}$

$$\therefore \quad \mu_n C_{ox}(9)(4 - V_a)^2 = \mu_n C_{ox}(4)(V_a - 2)^2$$

$$\frac{9}{4} = \left(\frac{V_a - 2}{4 - V_a}\right)^2$$

$$\frac{3}{2} = \frac{V_a - 2}{4 - V_a}$$

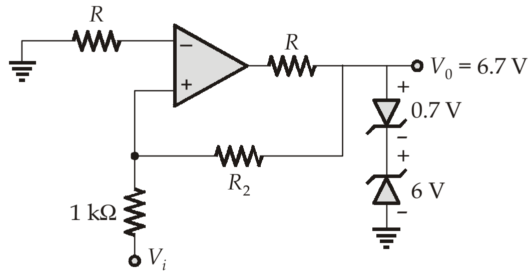
$$12 - 3V_a = 2V_a - 4$$

$$16 = 5V_a$$

$$V_a = \frac{16}{5} = 3.2 \text{ Volts}$$

13. (b)

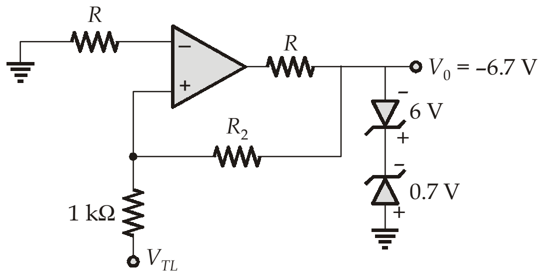
At upper Threshold point,



$$\therefore \quad \frac{R_2 V_{TH} + 6.7(1)}{R_2 + 1} = 0$$

$$V_{TH} = \frac{-6.7}{R_2}$$

At lower Threshold point,



$$\frac{R_2 V_{TL} - 6.7(1)}{R_2 + 1} = 0$$

$$V_{TL} = \frac{6.7}{R_2}$$

Given that, $|V_{TH} - V_{TL}| = 2$

$$\frac{13.4}{R_2} = 2$$

$$R_2 = 6.7 \text{ k}\Omega$$

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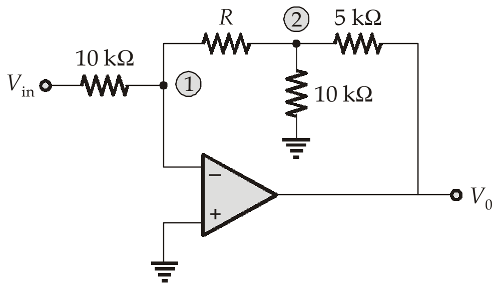
14. (a)



$$V_1 = 0$$

Apply KCL at node-1

$$\frac{V_{in} - 0}{10} = \frac{0 - V_2}{R}$$

$$-\left[\frac{V_{in}}{10} \times R\right] = V_2 \quad \text{...(i)}$$

Apply KCL at node-2

$$\frac{V_2}{R} + \frac{V_2}{10} + \frac{V_2 - V_0}{5} = 0$$

$$V_2\left[\frac{1}{R} + \frac{1}{10} + \frac{1}{5}\right] = \frac{V_0}{5} \quad \text{...(ii)}$$

From equation (i) and (ii), we get

$$\frac{-V_{in} \cdot R}{10}\left[\frac{1}{R} + \frac{3}{10}\right] = \frac{V_0}{5}$$

$$\frac{R}{10}\left[\frac{10 + 3R}{10R}\right] = \frac{-V_0}{V_{in}} \times \frac{1}{5}$$

$$\frac{10 + 3R}{20} = \left(\frac{-V_0}{V_{in}}\right)$$

Given that, $$\frac{V_0}{V_{in}} = -6$$

$$\frac{10 + 3R}{20} = 6$$

$$10 + 3R = 120$$

$$R = \frac{110}{3} \text{k}\Omega$$

$$R = 36.66 \text{ k}\Omega$$

15. (c)

$$\text{Line regulation} = \frac{\Delta V_{out}}{\Delta V_{in}} \times 100\%$$

By replacing the zener diode with it's equivalent circuit, we get,

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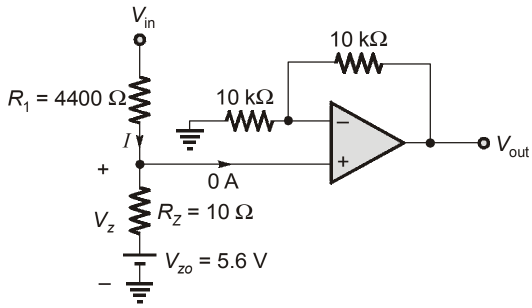

$$I = \frac{V_{in} - V_{zo}}{4410\ \Omega}$$

$$V_z = V_{zo} + IR_z = V_{zo} + \frac{10}{4410}(V_{in} - V_{zo})$$

$$= V_{zo} + \frac{1}{441}(V_{in} - V_{zo}) = \frac{440}{441}V_{zo} + \frac{1}{441}V_{in}$$

$$V_{out} = \left(1 + \frac{10\text{ k}\Omega}{10\text{ k}\Omega}\right)V_z = 2V_z = \frac{880}{441}V_{zo} + \frac{2}{441}V_{in}$$

$$\Delta V_{out} = \frac{\partial V_{out}}{\partial V_{in}} \times \Delta V_{in}$$

$$\frac{\Delta V_{out}}{\Delta V_{in}} = \frac{\partial V_{out}}{\partial V_{in}} = \frac{2}{441}$$

$$\text{Line regulation} = \frac{\Delta V_{out}}{\Delta V_{in}} \times 100 = \frac{2}{441} \times 100 \simeq 0.454\%$$

16. (b)

Case I : When $V_{in} < 0$ V

When $V_{input} < 0$ V, then the diode D_1, will be in forward biased and diode D_2 will be OFF, hence the output is equal to 0 V, which is shown in figure-1.

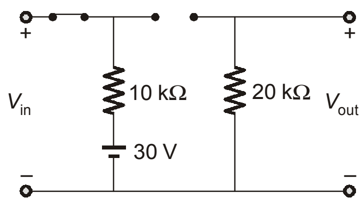

Figure (1)

Case II : $0 < V_{in} < 20$ V

D_1 is ON and D_2 is ON.

The equivalent circuit is shown in figure (2).

From the figure it is clear that the output

$$V_{out} = V_{in}$$

Thus it will be a straight line when plotted in the transfer curve [part (2)].

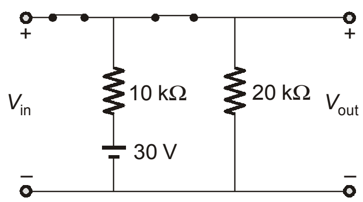

Figure (2)

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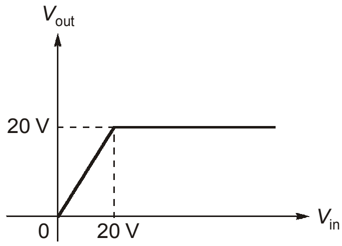
Case III : For $V_{input} > 20$ V
D_1 = OFF and D_2 = ON
Thus, the output will be a constant voltage V_{out}.

$$V_{out} = \frac{20}{20+10} \times 30 \text{ V} \qquad (\because \text{ voltage division})$$

Thus, $$V_{out} = 20 \text{ V}$$

Hence, the output response can be drawn as



17. (c)

Now, $$I_{in} = I_{D_1} + I_{D_2}$$

and $$V_{D_1} = V_{D_2} \qquad (\because \text{ diodes are in parallel})$$

thus, $$V_T \ln\left(\frac{I_{D_1}}{I_{s_1}}\right) = V_T \ln\left(\frac{I_{D_2}}{I_{s_2}}\right)$$

$$\Rightarrow \quad \frac{I_{D_1}}{I_{s_1}} = \frac{I_{D_2}}{I_{s_2}}$$

$$I_{D_1} = \left(\frac{I_{D_2}}{I_{s_2}}\right) \cdot I_{s_1}$$

Now, $$I_{in} = I_{D_2} + I_{D_2}\left(\frac{I_{s_1}}{I_{s_2}}\right)$$

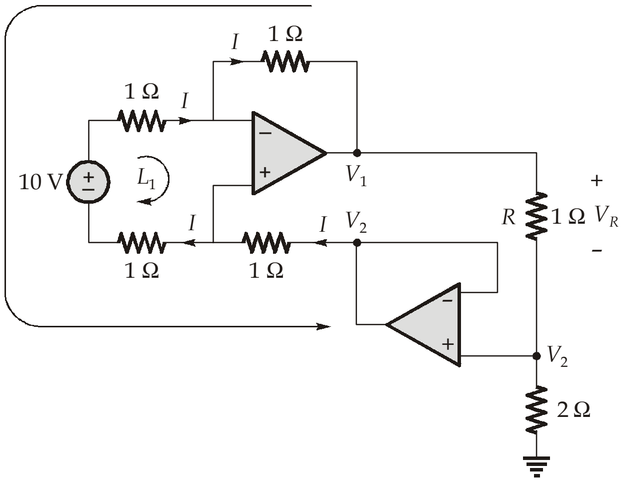
$$I_{in} = \left(1 + \frac{I_{s_1}}{I_{s_2}}\right) I_{D_2}$$

$$\Rightarrow \quad I_{D_2} = \frac{I_{in}}{1 + \frac{I_{s_1}}{I_{s_2}}}$$

Now, I_{s_1} and I_{s_2} are reverse saturation currents of the diodes and $I_s \propto A$.
Thus the above equation can be written as,

$$I_{D_2} = \frac{I_{in}}{1 + \frac{I_{s_1}}{I_{s_2}}} = \left(\frac{I_{in}}{1 + \frac{A_1}{A_2}}\right)$$

18. (d)



Apply KVL in loop-1,

$$-10 + I + I = 0$$
$$2I = 10$$
$$I = 5 \text{ A}$$

Applying KVL in the loop shown,

we get, $V_1 = -5 -5 + 10 - 5 - 5 + V_2$

$$V_1 - V_2 = -10 \text{ V}$$

$\therefore$ voltage across resistor,

$$R = V_R = V_1 - V_2 = -10 \text{ V}$$

19. (c)

$$\frac{I_{D1}}{I_{D2}} = \frac{\frac{\mu_n C_{ox}}{2}\left(\frac{W_1}{L}\right)(V_{GS1} - V_t)^2}{\frac{\mu_n C_{ox}}{2}\left(\frac{W_2}{L}\right)(V_{GS2} - V_t)^2}$$

$V_{GS1} = 3$ V; $\quad V_{GS2} = 2$ V;

$$I_{D1} = I_{D2} = 120 \ \mu\text{A}$$

$$\therefore \quad 1 = \frac{W_1(3-1)^2}{W_2(2-1)^2}$$

$$\therefore \quad 1 = \frac{W_1(4)}{W_2}$$

$$W_2 = 4\,W_1$$

$$I_{D1} = \frac{\mu_n C_{ox}}{2}\left(\frac{W_1}{L}\right)(V_{GS1} - V_t)^2$$

$$120\ \mu = \frac{120\mu}{2}\left(\frac{W_1}{1\,\mu}\right)(3-1)^2$$

$$1 = \frac{W_1}{2\mu} \times 4$$

$$W_1 = 0.5\ \mu\text{m}$$

$$\therefore \quad W_2 = 4 \times W_1 = 4 \times 0.5\ \mu = 2\ \mu\text{m}$$

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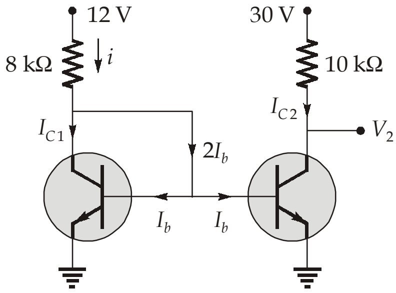
20. (a)



$$12 - i \times 8 \times 10^3 - 0.7 = 0$$

Now, $$i = \frac{12-0.7}{8\times10^3} = 1.4125 \text{ mA}$$

$$i = I_{c1} + 2I_b = (\beta + 2)I_b$$

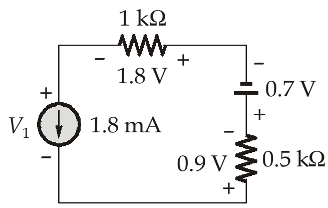
$$I_b = \frac{i}{\beta+2} = \frac{1.4125}{202} = 6.99\ \mu\text{A} \approx 7\ \mu\text{A}$$

$$I_{c2} = 200I_b = 200 \times 7\ \mu$$
$$= 1.4 \text{ mA}$$

∴ $$V_2 = 30 - I_{c2} \times 10k$$
$$V_2 = 30 - 1.4 \times 10$$
$$= 16 \text{ V}$$

21. (a)

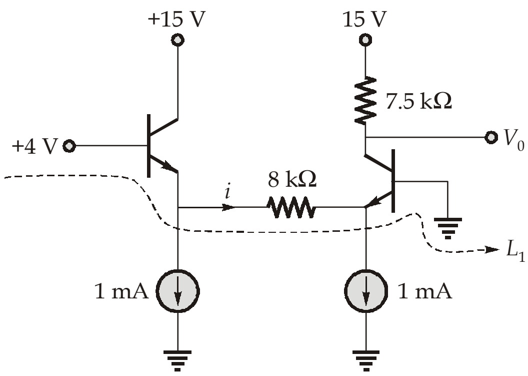
From the circuit given, after observation, we can conclude that D_2 will be ON and D_1 will be OFF.



∴ $$V_1 = -0.9 - 0.7 - 1.8 = -3.4 \text{ V}$$

22. (a)

Apply KVL in the loop (L_1) shown in figure.



$$-4 + 0.7 + 8i - 0.7 = 0$$
$$8i = 4$$
$$i = 0.5 \text{ mA}$$

∴ $$I_{E2} = 1 \text{ mA} - 0.5 \text{ mA}$$
$$= 0.5 \text{ mA}$$

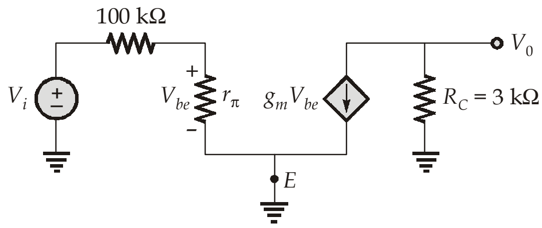
As, $$I_{C2} \simeq I_{E2}$$

∴ $$V_0 = 15 - 7.5\ I_{C2}$$
$$= 15 - 7.5 \times 0.5$$
$$V_0 = 11.25 \text{ volt}$$

23. (b)

The first step in the analysis consists of determining the quiescent operating point. For this purpose we assume that $V_i = 0$.

$$\therefore \quad I_B = \frac{V_{BB} - 0.7}{100k} = \frac{3 - 0.7}{100k} = 23\ \mu A$$



$$I_C = \beta I_B = 100 \times 23\ \mu = 2.3 \text{ mA}$$

$$\therefore \quad V_C = 10 - I_C \cdot R_C$$

$$= 10 - 2.3 \times 3 = 3.1 \text{ V}$$

$$r_e = \frac{V_T}{I_E} = \frac{25 \text{ mV}}{(2.3/0.99) \text{ mA}} = 10.8\ \Omega$$

$$g_m = \frac{I_C}{V_T} = \frac{2.3 \text{ mA}}{25 \text{ mV}} = 92 \text{ mA/V}$$

$$r_\pi = \frac{\beta}{g_m} = \frac{100}{92} = 1.09 \text{ k}\Omega$$

$$\therefore \quad V_{be} = V_i \times \frac{r_\pi}{r_\pi + R_{BB}}$$

$$V_{be} = V_i \times \frac{1.09}{101.09} = 0.011\ V_i$$

$$\therefore \quad V_0 = -g_m V_{be} R_C$$

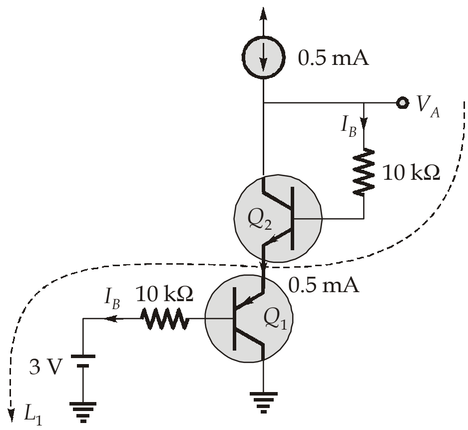
$$= -92 \times 0.011\ V_i \times 3$$

$$= -3.04\ V_i$$

$$\therefore \quad A_V = \frac{V_0}{V_i} = -3.04 \approx -3$$

24. (c)

For the circuit shown above,



Emitter current of both transistors is,

$$I_E = 0.5 \text{ mA}$$

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∴ Base current of both transistor is,

$$I_B = \frac{0.5\text{ mA}}{\beta+1} = \frac{0.5\text{ mA}}{101} = 4.95\ \mu\text{A}$$

Apply KVL in the loop shown in above figure,

$$\therefore \quad V_A = 10K \times 4.95\ \mu + 0.7 + 0.7 + 10K \times 4.95\ \mu + 3$$
$$= 4.499$$
$$V_A = 4.5\text{ V}$$

25. (b)

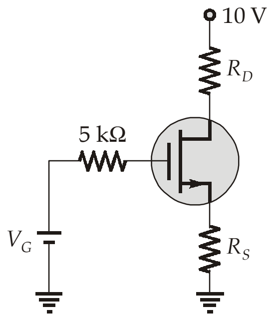
For V_P = 1 V and R_L reduced, the lowest value possible for while the output remaining an undistorted sine wave of 10 V peak can be found from

$$i_{0\,max} = 20\text{ mA} = \frac{10\text{ V}}{R_{L\min}} + \frac{10\text{ V}}{9\text{ k}\Omega + 1\text{ k}\Omega}$$

$$19\text{ mA} = \frac{10\text{ V}}{R_{L\min}}$$

$$R_{L\min} = \frac{10\text{ V}}{19\text{ mA}} = 526\ \Omega$$

26. (b)



$$V_G = V_{DD} \times \frac{R_{G2}}{R_{G1}+R_{G2}} = \frac{10}{10+10} \times 10 = 5\text{ V}$$

$$R_G = (10\ ||\ 10) = 5\text{ k}\Omega$$
$$V_{GS} = (V_G - I_D \times R_S) = (5 - 6I_D)$$

Assuming the saturation mode of operation

$$I_D = \frac{1}{2}K_n' \frac{W}{L}(V_{GS} - V_t)^2$$

$$\left(\frac{5 - V_{GS}}{6}\right) = \frac{1}{2} \times 1(V_{GS} - 1)^2$$

$$5 - V_{GS} = 3V_{GS}^2 + 3 - 6V_{GS}$$

$$3V_{GS}^2 - 5V_{GS} - 2 = 0$$

$$V_{GS} = 2,\ -\frac{1}{3}$$

$$V_{GS} = 2\text{ V}$$

$$\therefore \quad I_D = \left(\frac{5-2}{6}\right) = 0.5 \text{ mA}$$

$$V_{DS} = 10 - 0.5 \times 12 = 4 \text{ V}$$

$$\because \quad V_{DS} > (V_{GS} - V_t)$$

$\therefore$ Assumption is correct.

27. (c)

$$V_0 \text{ (offset due to } V_{I0}) = V_{I0}\frac{R_1 + R_f}{R_1} = (4\text{mV})\frac{5\text{k}\Omega + 500\text{k}\Omega}{5\text{k}\Omega} = 404 \text{ mV}$$

$$V_0 \text{ (offset due to } I_{I0}) = I_{I0}R_f = (150 \text{ nA})\ (500 \text{ k}\Omega) = 75 \text{ mV}$$

Resulting in a total offset,

$$V_0 \text{ (total offset)} = V_0 \text{ (offset due to } V_{I0}) + V_0 \text{ (offset due to } V_{I0})$$

$$= 404 + 75 = 479 \text{ mV}$$

28. (b)

We assume that both diodes are conducting, then voltage at point-B, $V_B = 0$ and $V = 0$. The current in D_1 is obtained from

$$I_{D1} = \frac{10-0}{5} = 2 \text{ mA}$$

The node equation at B is

$$I_{D2} + 2 = \frac{0-(-10)}{10}$$

Which yields $I_{D2} = -1$ mA. Since this is not possible our assumption is not correct. We start again assumption that D_2 is off and D_1 is on. The current I_{D1} is given

$$I_{D1} = \frac{10-(-10)}{15} = 1.33 \text{ mA}$$

and the voltage at node-B is

$$V_B = -10 + 10 \times 1.33 = +3.3 \text{ V}$$

Thus D_2 is reverse biased as assumed and the final result is $V = 3.33$ V.

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29. **(d)**

$$g_{m0} = \frac{2I_{Dss}}{|V_p|} = \frac{2(8\,\text{mA})}{6} = 2.67 \text{ ms}$$

$$g_m = g_{m0}\left(1 - \frac{V_{GSQ}}{V_P}\right) = 2.67\,\text{mS}\left(1 - \frac{(-2.6)}{(-6)}\right) = 1.51 \text{ mS}$$

$$r_d = 50 \text{ k}\Omega$$

$$Z_i = R_G = 1 \text{ M}\Omega$$

$$r_d > 10R_D$$

Therefore, $Z_0 = R_D = 3.3 \text{ k}\Omega$

With r_d,

$$= \frac{-g_m R_D}{1 + g_m R_s + \dfrac{R_D + R_s}{r_d}}$$

$$A_V = \frac{-(1.51\,\text{mS})(3.3\,\text{k}\Omega)}{1 + (1.51\,\text{mS})(1\,\text{k}\Omega) + \dfrac{3.3\text{k}\Omega + 1\text{k}\Omega}{50\text{k}\Omega}}$$

$$= \frac{-4.983}{1 + 1.51 + 0.086} = -1.92$$

30. **(a)**

The amplifier gain is calculated to be

$$A = A_1 A_2 A_3$$

$$= \left(1 + \frac{R_f}{R_1}\right)\left(\frac{-R_f}{R_2}\right)\left(\frac{-R_f}{R_3}\right)$$

$$= \left(1 + \frac{470}{4.3}\right)\left(\frac{-470}{33}\right)\left(\frac{-470}{33}\right)$$

$$= (110.3)\ (-14.24)\ (-14.24) = 22.2 \times 10^3$$

So that, $V_0 = AV_i = 22.2 \times 10^3 \times 80\ \mu\text{V}$

$$= 1.78 \text{ V}$$

■■■■