S.No.:03SK_ECEE_DEFGHI_13925

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DIGITAL ELECTRONICS

EC-EE

Date of Test : 13/09/2025

ANSWER KEY ➤

1.	(a)	7.	(c)	13.	(a)	19.	(a)	25.	(b)
2.	(d)	8.	(a)	14.	(d)	20.	(a)	26.	(b)
3.	(d)	9.	(d)	15.	(b)	21.	(b)	27.	(d)
4.	(a)	10.	(b)	16.	(d)	22.	(b)	28.	(c)
5.	(a)	11.	(b)	17.	(a)	23.	(c)	29.	(d)
6.	(c)	12.	(b)	18.	(a)	24.	(b)	30.	(a)

DETAILED EXPLANATIONS

1. (a)

$$A = 10,\ B = 11,\ C = 12$$

Therefore, $x > C(12)$

$$x = 13$$

Therefore, the least decimal equivalent

$$= (13)^2 + 10 \times 13 + 12 = 311$$

2. (d)

After 1st pulse contents are 1110
After 2nd pulse contents are 0111
After 3rd pulse contents are 0011
After 4th pulse contents are 1001
After 5th pulse contents are 1100

3. (d)

$$N = 5,$$
$$t_{pd} = 2 \text{ nsec}$$
$$T = 2\ N\ t_{pd}$$
$$\Rightarrow \quad T = 2 \times 5 \times 2 \times 10^{-9}$$
$$= 20 \text{ nsec}$$

4. (a)

$$Y = \bar{S}_0\bar{S}_1I_0 + S_0\bar{S}_1I_1 + \bar{S}_0S_1I_2 + S_0S_1I_3$$
$$= \bar{A}\bar{B}C + \bar{A}B\cdot 1 + A\bar{B}\cdot 0 + AB\cdot\bar{C}$$
$$= \bar{A}\bar{B}C + \bar{A}B\cdot(C+\bar{C}) + AB\bar{C}$$
$$= \bar{A}\bar{B}C + \bar{A}BC + \bar{A}B\bar{C} + AB\bar{C}$$
$$\approx 001,\ 011,\ 010,\ 110$$
$$Y(A, B, C) = \Sigma m\ (1,2,3,6)$$

5. (a)

From the given circuit

$$X_1 = Y_1$$

and $$X_2 = \bar{Y}_1Y_2 + Y_1\bar{Y}_2 = Y_1 \oplus Y_2$$

let $Y_1Y_2 = 10$
then $X_1X_2 = 11$
and $Y_1Y_2 = 11$
$X_1X_2 = 10$

Hence answer (a) is correct.

6. (c)

7. (c)

$$f_{out} = \frac{f_{in}}{\text{MOD (total)}}$$

$$\therefore \quad \text{MOD} = \frac{f_{in}}{f_{out}} = 5 \times 10 \times 2x \times 4$$

$$x = \frac{1}{400} \times \frac{1.6 \times 10^9}{1 \times 10^6} = \frac{1600}{400}$$

$$x = 4 \text{ flip-flops}$$

8. (a)

The output logic function of the given circuit can be expressed as,

$$f = \overline{\left(\overline{(\overline{AB})C}\right)\left(\overline{\overline{C}D}\right)} = (\overline{AB})C + \overline{C}D = (\overline{A} + \overline{B})C + \overline{C}D$$

9. (d)

$$I_R = I_3 + I_2 + I_0$$

$$= \left(\frac{E_{reff}}{2R} + \frac{E_{reff}}{4R} + \frac{E_{reff}}{16R}\right) = \left(\frac{10}{10} + \frac{10}{20} + \frac{10}{80}\right)$$

$$= \frac{130}{80} = \frac{13}{8} = 1.625 \text{ mA}$$

10. (b)

$$Y = \overline{AB + CD}$$

Given $A = B = 0$

Thus only $C = 1 = D$ will give $Y = 0$

11. (b)

The given circuit represents a 3-bit counter. So the count can be represented as

Clk	Q_2	Q_1	Q_0	
Initially	0	0	0	
1	0	0	1	
2	0	1	0	
3	0	1	1	
4	1	0	0	
5	1	0	1	$\Rightarrow$5th clock pulse
6	1	1	0	
7	1	1	1	

$$\therefore \quad Y = Q_2 \oplus Q_1 \oplus Q_0$$

$$= 1 \oplus 0 \oplus 1 = 0$$

12. (b)

Let n number of flip flop cascaded each having propagation delay of t_{pd}.

Frequency of operation

$$\frac{1}{nt_{pd}} \geq 10 \text{ MHz}$$

$$\therefore \quad n \leq \frac{1}{t_{pd} \times 10 \text{ MHz}} \leq \frac{1}{12 \times 10^{-9} \times 10^{7}} \leq \frac{100}{12}$$

$$n = 8$$

For $n = 8$ MOD number of counter $2^8 = 256$

13. (a)

$$\text{Full scale voltage} = \text{Step size} \times \text{Maximum count}$$
$$= \text{Step size} \times (2^n - 1)$$
$$= 10 \text{ mV} \times 255$$
$$= 2.55 \text{ V}$$

$$\% \text{ Resolution} = \frac{1}{2^n - 1} \times 100 = \frac{100}{255} = 0.392\%$$

14. (d)

$$f_1(A, B, C) = \Sigma(2, 3, 4)$$
$$f_2(A, B, C) = \pi(0, 1, 3, 6, 7) = \Sigma(2, 4, 5)$$

For function f to be zero

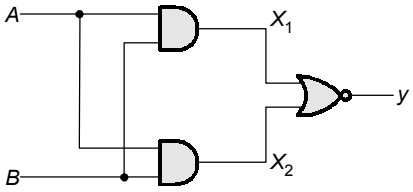
$$f_3(A, B, C) = \overline{[f_1(A, B, C) \cap f_2(A, B, C)]}$$
$$= \Sigma(0, 1, 3, 5, 6, 7)$$

Maximum minterms possible are 6.

15. (b)

Clock Pulses	Register Content	Output of 4 × 1 MUX
	0 0 1 1	→ 0
1	0 0 0 1	→ 0
2	0 0 0 0	→ 1
3	1 0 0 0	→ 1
4	1 1 0 0	→ 1
5	1 1 1 0	→ 1
6	1 1 1 1	→ 0
7	0 1 1 1	→ 0
8	0 0 1 1	

16. (d)



$$X_1 = AB$$

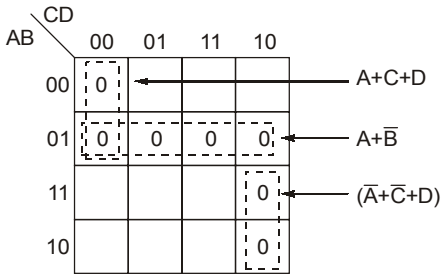
$$X_2 = AB$$

$$y = \overline{AB + AB} = \overline{AB}$$

A	B	$y = \overline{AB}$
0	0	1
0	1	1
1	0	1
1	1	0 → LED will be ON

17. (a)

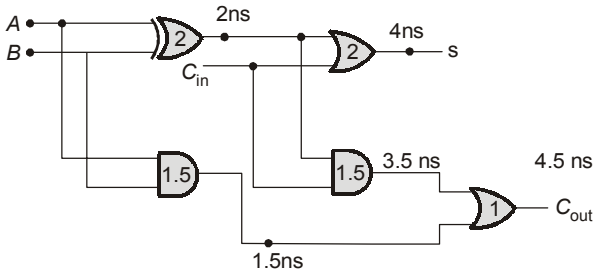
Drawing k-map for x.



$\therefore$ $$x = (A + C + D)(\overline{A} + \overline{C} + D)(A + \overline{B})$$

18. (a)

Full adder implementation



$$s = A \oplus B \oplus C$$

$$C_{out} = (A \oplus B)\, C_{in} + AB$$

From figure, it is clear that delay for sum and carry will be 4ns and 4.5ns respectively.

19. (a)

Here

$$J_0 = 1,$$
$$K_0 = Q_2,$$
$$J_1 = \bar{Q}_2 \odot Q_0,$$
$$K_1 = 1,$$
$$J_2 = Q_1,$$
$$K_2 = 1$$

CLK	Q_2	Q_1	Q_0
Initial state	0	0	0
1	0	0	1
2	0	1	1
3	1	0	1
4	0	0	0

Modulus of the counter is 4.

$$115 = (28 \times 4) + 3$$

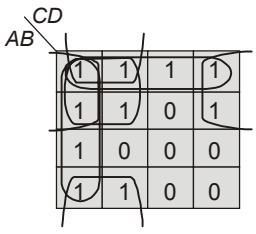
Thus, the count after 115 clock pulses will be $(Q_2Q_1Q_0)_2 = (101)_2$

20. (a)

Using Truth table:

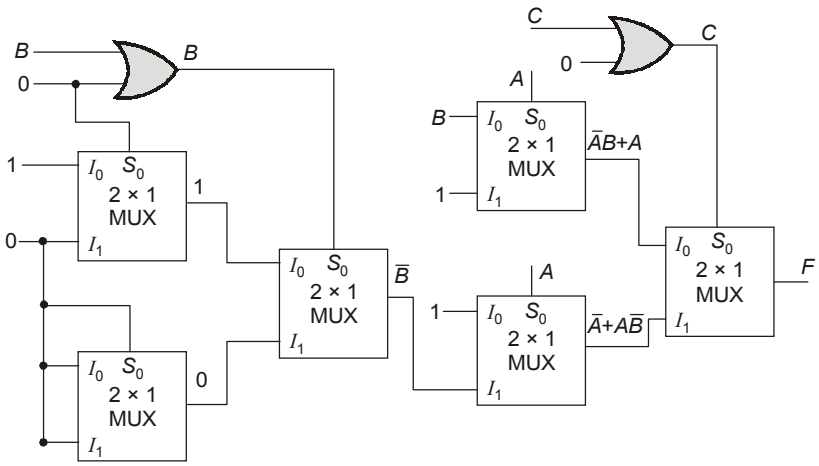
A	B	C	D	$S_1 \times S_2$	F
0	0	0	0	$0 \times 0 = 0 \le 2$	1
0	0	0	1	$0 \times 1 = 0 \le 2$	1
0	0	1	0	$0 \times 2 = 0 \le 2$	1
0	0	1	1	$0 \times 3 = 0 \le 2$	1
0	1	0	0	$1 \times 0 = 0 \le 2$	1
0	1	0	1	$1 \times 1 = 1 \le 2$	1
0	1	1	0	$1 \times 2 = 2 \le 2$	1
0	1	1	1	$1 \times 3 = 3 > 2$	0
1	0	0	0	$2 \times 0 = 0 \le 2$	1
1	0	0	1	$2 \times 1 = 2 \le 2$	1
1	0	1	0	$2 \times 2 = 4 > 2$	0
1	0	1	1	$2 \times 3 = 6 > 2$	0
1	1	0	0	$3 \times 0 = 0 \le 2$	1
1	1	0	1	$3 \times 1 = 3 > 2$	0
1	1	1	0	$3 \times 2 = 6 > 2$	0
1	1	1	1	$3 \times 3 = 9 > 2$	0

$\therefore$ $F =$



$$F = \bar{A}\bar{B} + \bar{A}\bar{C} + \bar{C}\bar{D} + \bar{A}\bar{D} + \bar{B}\bar{C}$$

21. (b)



$\therefore$

$$F = \bar{C}(A+\bar{A}B)+C(\bar{A}+A\bar{B})$$

$$= \bar{C}(A+B)+C(\bar{A}+\bar{B})$$

$$= A\bar{C}+B\bar{C}+\bar{A}C+\bar{B}C$$

$$= (A\oplus C)+(B\oplus C)$$

22. (b)

23. (c)

$$F = \bar{A}\bar{B}I_0+\bar{A}BI_1+A\bar{B}I_2+ABI_3$$

$$= \bar{A}\bar{B}C+\bar{A}BC+A\bar{B}\bar{C}$$

$$= \bar{A}C+A\bar{B}\bar{C}$$

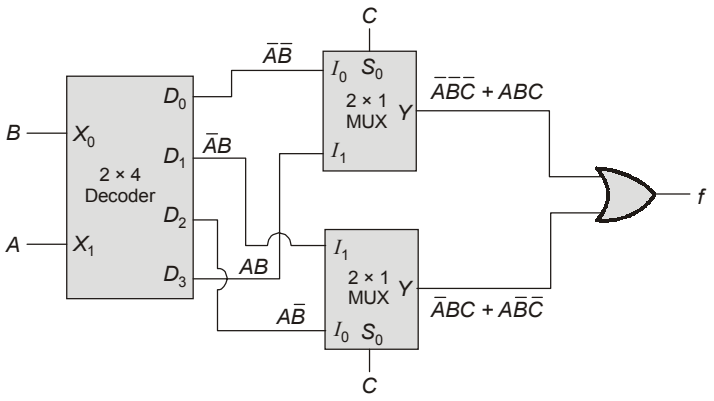
24. (b)

X	Y	Z
0	0	0
0	1	1
1	0	0
1	1	0

X	Y	Q	Z
0	0	OFF	0
0	$+5V$	OFF	$+5V$
$+5V$	0	ON	0
$+5V$	$+5V$	ON	0

25. (b)

The above circuit can be redrawn as

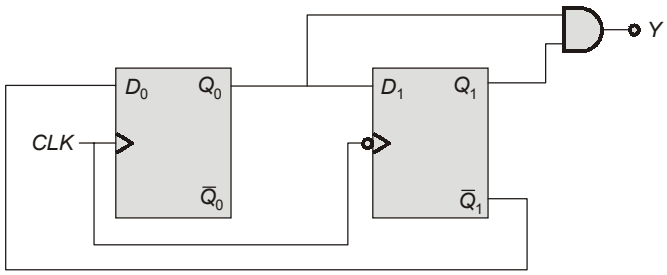


Thus, $$f = \underbrace{\bar{A}\bar{B}\bar{C} + ABC}_{} + \underbrace{\bar{A}BC + A\bar{B}\bar{C}}_{} = \bar{B}\bar{C}(A + \bar{A}) + BC(\bar{A} + \bar{A})$$

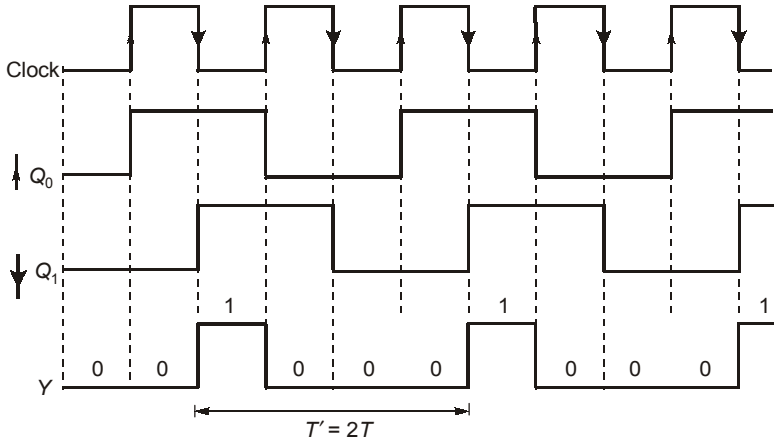
$$= \bar{B}\bar{C} + BC = B \odot C$$

26. (b)

Assume the output of both the flip-flops is 0 initially.



Waveforms :



$$\text{Duty cycle} = \frac{T_{ON}}{T_{ON} + T_{OFF}} \times 100\% = \frac{1}{1+3} \times 100\%$$

$$= \frac{1}{4} \times 100\% = 25\%$$

27. (d)

The logic outputs of the OR gates can be given as

$$F_1 = \Sigma m(0, 1, 2, 4, 6)$$
$$F_2 = \Sigma m(0, 3, 6)$$
$$F_3 = \Sigma m(0, 4, 6, 7)$$

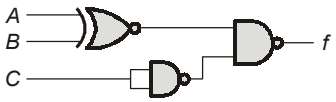
After passing the functions through a NAND gate, we get,

$$f = \overline{F_1 \cdot F_2 \cdot F_3}$$

$$\overline{f} = F_1 \cdot F_2 \cdot F_3 = \Sigma m(0, 6)$$

$$\overline{f} = \overline{A}\overline{B}\overline{C} + AB\overline{C} = (\overline{A}\overline{B} + AB)\cdot\overline{C} = (A \odot B)\cdot\overline{C}$$

$$f = (A \oplus B) + C = \overline{(A \odot B)\,(\overline{C})}$$



Thus, we require 5 + 2 = 7 gates.

5 for EX-NOR gate and 2 more NAND gates.

28. (c)

Number of states for 8-bit up-counter = $2^8 - 1 = 255$

thus the counter ranges from –0 to 255

Hence, to go from $(10101011)_2 = (171)_{10}$ to $(00111010)_2 = (58)_{10}$

The counter has to go initially from 171 to 255 and then from 0 to 58.

Hence,

from 171 to 255 = 255 – 171 = 84 clock pulse required

from 255 to 0 = 1 clock pulse requried

and from 0 to 58 = 58 clock pulse requried

∴ The total number of clock pulse required is

= 84 + 1 + 58

= 143

29. (d)

The accuracy is ± 0.1% of full scale, i.e.

$$\text{Accuracy} = \pm\frac{0.1}{100}\times 1.260\ \text{V} = \pm 1.26\ \text{mV}$$

The offset error is = ± 1 mV

∴ maximum error = ± 1.26 mV + ± 1 mV = ± 2.26 mV

30. (a)

$$2r + 3 + 4r + 4 + r + 4 + 3r + 2 = 2r^2 + 2r + 3$$
$$10r + 13 = 2r^2 + 2r + 3$$
$$2r^2 - 8r - 10 = 0$$
$$r^2 - 4r - 5 = 0$$
$$r = 5, -1$$

∵ Radix cannot be negative

∴ $r = 5$

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