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DIGITAL ELECTRONICS

EC-EE

Date of Test : 28/08/2025

ANSWER KEY ➤

1.	(c)	7.	(c)	13.	(b)	19.	(a)	25.	(d)
2.	(d)	8.	(a)	14.	(c)	20.	(d)	26.	(c)
3.	(d)	9.	(d)	15.	(c)	21.	(b)	27.	(c)
4.	(b)	10.	(b)	16.	(c)	22.	(a)	28.	(d)
5.	(c)	11.	(d)	17.	(a)	23.	(d)	29.	(d)
6.	(d)	12.	(a)	18.	(b)	24.	(b)	30.	(b)

DETAILED EXPLANATIONS

1. (c)

$$(EOB)_H - (ABF)_H = (34C)_H$$
$$(34C)_H = (001101001100)_2 = (1514)_8$$
$$7\text{'s compliment} = (6263)_8$$
$$8\text{'s compliment} = (6263)_8 + 1$$
$$= (6264)_8$$

2. (d)

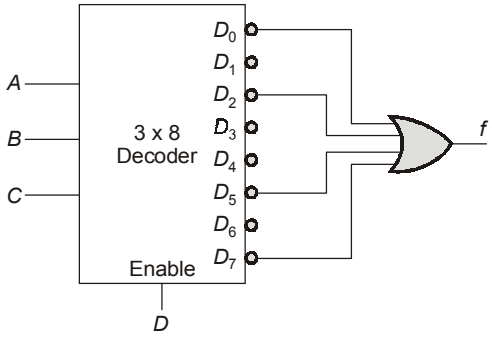
3. (d)

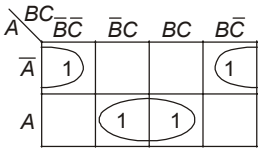
$$Y = \bar{C}\bar{D} + (\bar{A}\cdot\bar{B})(\bar{D}C) + \bar{C}DS = Y = \bar{C}\bar{D} + (\overline{D+\bar{C}})(\overline{A+B}) + \overline{C+\bar{D}+\bar{S}}$$

4. (b)

Redrawing the circuit

A	B	C	D	f
X	X	X	0	0
0	0	0	1	1
0	0	1	1	0
0	1	0	1	1
0	1	1	1	0
1	0	0	1	0
1	0	1	1	1
1	1	0	1	0
1	1	1	1	1





$$f = D(\bar{A}\bar{C} + AC)$$

5. (c)

ECL is fastest logic family. So, ECL RAM's are used as cache memory.
In ROM, data can be read from random locations.

6. (d)

Inhibitor - If one of the input of AND gate or OR gate is complemented, the gate is called inhibitor.
So output of inhibitor are

$$A\bar{B}, \quad \bar{A} + B$$
$$\overline{\bar{A}B}, \quad A + \bar{B}$$

7. (c)

For a 12 bit BCD number
Range is 000 to 999

$$\text{Step size} = \frac{10.24}{999} = 10.25 \text{ mV}$$

8. (a)

Conversion time for an n-bit successive approximation type ADC = nT_{clk} (independent of the input voltage)

Given $n = 8$

Therefore, $T_{conversion} = 8\ T_{clk}$

$$= \frac{8}{f_{clk}}$$

$$= \frac{8}{10 \times 10^6}$$

$$= 800 \text{ nsec}$$

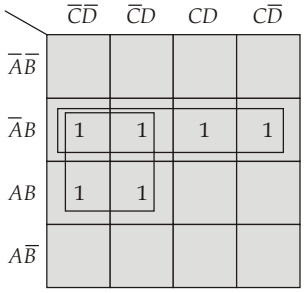
9. (d)

$$Y = \overline{A\overline{B}C} \cdot (\overline{A}BC + \overline{A}BD + B\overline{C})$$

$$Y = (\overline{A} + B + \overline{C})(\overline{A}BC + \overline{A}BD + B\overline{C})$$

$$Y = \overline{A}BC + \overline{A}BD + \overline{A}B\overline{C} + B\overline{C} + \overline{A}B\overline{C}D$$

$$Y = \overline{A}BC + \overline{A}BD + B\overline{C}$$



$$Y = B\overline{C} + \overline{A}B = B\left[\overline{A} + \overline{C}\right]$$

10. (b)

From the combinational logic,

Assuming D is input, Q_n is present state and Q_{n+1} is the next state, then

$$R = \overline{D \oplus Q_n} \quad \text{and} \quad S = D \oplus Q_n$$

Characteristic equation of R-S flip flop.

$$Q_{n+1} = S + \overline{R}Q_n$$

So, $Q_{n+1} = (D \oplus Q_n) + (\overline{\overline{D \oplus Q_n}})Q_n$

$= (D \oplus Q_n) + (D \oplus Q_n)Q_n$

$= (D \oplus Q_n)(1 + Q_n)$

$= D \oplus Q_n$

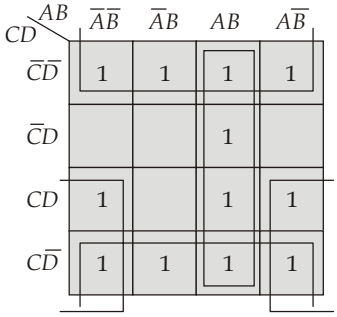
$= D\overline{Q_n} + \overline{D}Q_n$

For $D = 0$, $Q_{n+1} = Q_n$

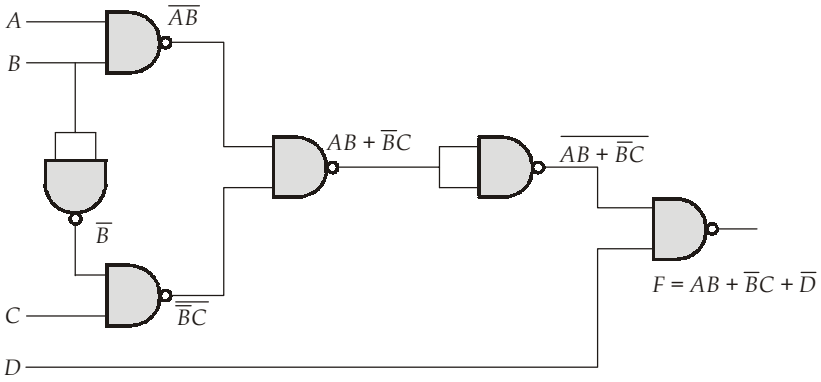
For $D = 1$, $Q_{n+1} = Q_{n+1} = \overline{Q_n}$

So, the circuit represent a T flip-flop.

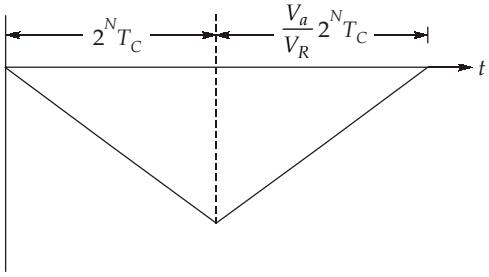
11. (d)



$$F = \overline{D} + \overline{B}C + AB$$



12. (a)



$$\text{Total conversion time, } (t) = 2^N T_C + \frac{V_a}{V_R} \cdot 2^N T_C$$

where, N = Number of bits of converter

T_C = Time period of the clock

V_a = analog voltage

V_R = Reference voltage

The largest V_a can be equal to V_R, therefore,

$$V_a = V_R$$

$$t = 2^{N+1} T_C$$

$$\frac{1}{f_{max}} = 2^{13+1} \cdot \frac{1}{f_c}$$

$\therefore$

$$f_c = 2^{14} \times f_{max} = 16384 \times 2$$

$$f_c = 32768 \text{ Hz}$$

13. (b)

$$(5330)_y = 5y^3 + 3y^2 + 3y + 0$$
$$= 5y^3 + 3y^2 + 3y$$
$$(1425)_x = x^3 + 4x^2 + 2x + 5$$

and,
$$(50)_y = 5y$$
$$(15)_x = x + 5$$

Hence,

$$5y^3 + 3y^2 + 3y + x^3 + 4x^2 + 2x + 5 = (5y + x + 5)^2$$

Putting the values of x and y from the options

$\left.\begin{matrix} x = 7 \\ y = 6 \end{matrix}\right\}$ satisfies the given equation.

$\therefore$ $(x, y) = (7, 6)$

14. (c)

This is an asynchronous counter, $\overline{Q_3Q_2}$ is connected to $\overline{CLR}$ input which means when Q_3Q_2 both are '1' then circuit will be reset to 000 state.

Clock	Q_3	Q_2	Q_1	
Initial	0	0	0	
1st	0	0	1	
2nd	0	1	0	
3rd	0	1	1	
4th	1	0	0	
5th	1	0	1	
6th	1	1	0	$\Rightarrow$ Counter will be reset

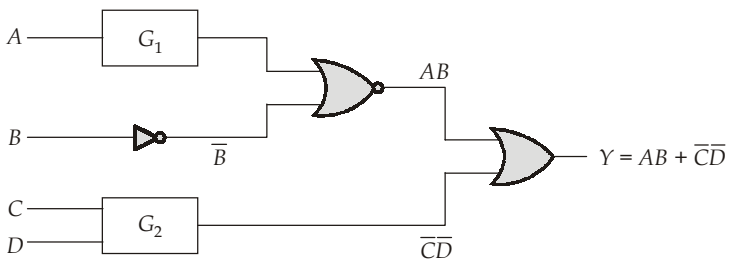
15. (c)

$$f_1 = \Sigma m(0, 1, 4, 5)$$
$$f_2 = \Sigma m(2, 3, 6, 7)$$

As f_1 and f_2 are independent outputs

So, $$y = f_1 \cdot f_2 = 0$$

16. (c)



$$G_1 = \text{NOT} = \overline{A}$$

$$G_2 = \text{NOR} = \overline{C + D} = \overline{C} \cdot \overline{D}$$

17. (a)

From the state transition diagram we can write,

A	Q	Q^+
0	0	1
0	1	1
1	0	1
1	1	0

$$Q^+ = \bar{A}\bar{Q} + \bar{A}Q + A\bar{Q}$$

$$= \bar{A} + A\bar{Q}$$

$$Q^+ = \bar{A} + \bar{Q} = \overline{A \cdot Q}$$

For D flip flop, $Q^+ = D$

So from option (a), we have

$$Q^+ = D = \overline{Q \cdot A}$$

18. (b)

State table

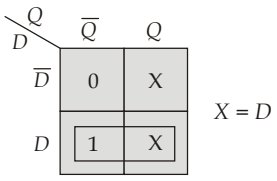
X	Y	Q	Q^+
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	1

Excitation table for XY

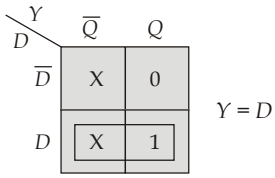
Q	Q^+	X	Y
0	0	0	X
0	1	1	X
1	0	X	0
1	1	X	1

Conversion of XY-flip-flop to D flip-flop.

D	Q	Q^+	X	Y
0	0	0	0	X
0	1	0	X	0
1	0	1	1	X
1	1	1	X	1



$X = D$



$Y = D$

19. (a)

$$I_{OL(\max)} = 32\ \text{mA}$$
$$I_{IL(\max)} = 1.6\ \text{mA}$$
$$I_{OH(\max)} = 400\ \mu\text{A}$$
$$I_{IH(\max)} = 10\ \mu\text{A}$$
$$\text{fanout (HIGH)} = \frac{I_{OH}}{I_{IH}} = \frac{400}{10} = 40$$
$$\text{fanout LOW} = \frac{I_{OL}}{I_{IL}} = \frac{32}{1.6} = 20$$
$$\therefore \quad \text{The overall fanout} = \text{Min (40, 20)}$$
$$= 20$$

Therefore, statements (a) is correct.

20. (d)

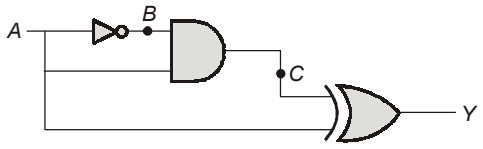
Since 16 ICs are used to form 32 kB RAM, each IC would provide

$$\frac{32k \times 8}{16} = 16\ \text{Kbits}$$

14 Address bits
↓
2^{14} cells/memory locations
↓
16 K cells
↓
16 K bits

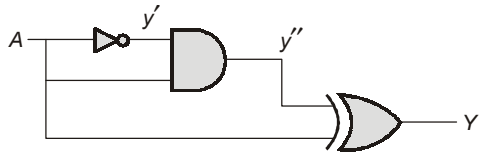
Since 16 K cells provide a capacity of 16 Kbits, so cell size must be 1 bit.

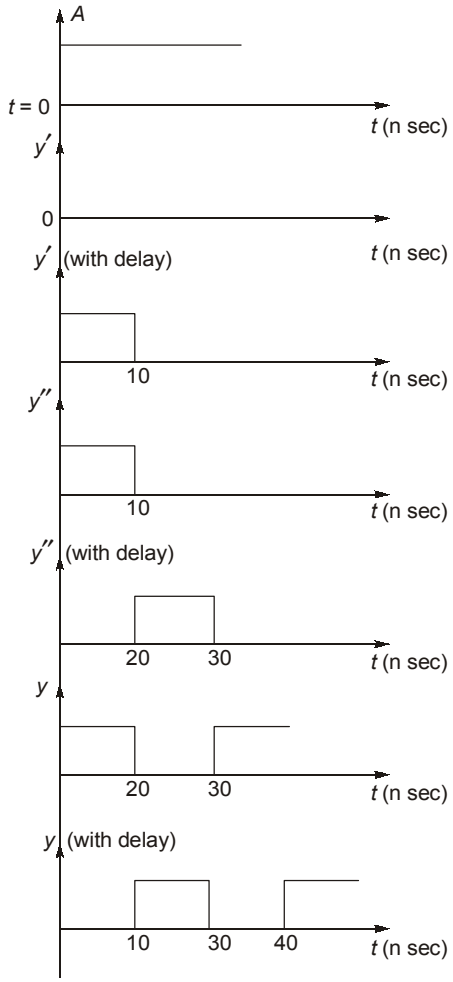
21. (b)



	A	B	C	Y
$t < 10$ ns	1	1	0	0
10 ns < t < 20 ns	1	0	0	1
20 ns < t < 30 ns	1	0	1	1
30 ns < t < 40 ns	1	0	0	0
40 ns < t	1	0	0	1

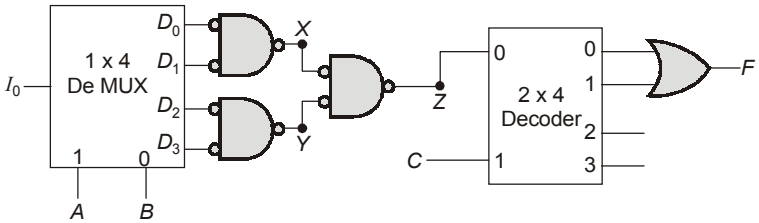
Alternate:





$\Rightarrow$ option (b) is correct.

22. (a)



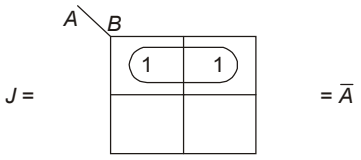
$$X = \overline{\bar{D}_0 \bar{D}_1}\, I_0 = (D_0 + D_1)I_0$$
$$= (\bar{A}\bar{B} + \bar{A}B)I_0 = \bar{A}I_0$$
$$Y = \overline{\bar{D}_2\, \bar{D}_3}\, I_0 = (D_2 + D_3)I_0$$
$$= (A\bar{B} + AB)I_0 = A\, I_0$$

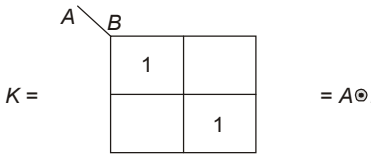
$$Z = (\overline{\bar{X}\cdot\bar{Y}}) = X + Y$$
$$= \bar{A}\cdot I_0 + A I_0 = I_0$$
$$F = (\bar{Z}\bar{C} + Z\bar{C}) = \bar{C}(\bar{I}_0 + I_0)$$
$$= \bar{C}$$

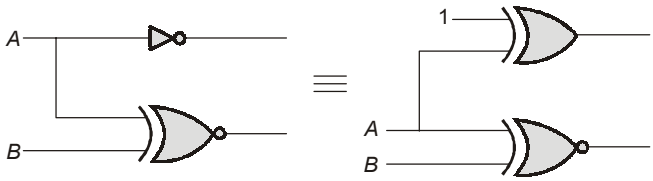
23. (d)

State Table

A	B	Q_{n+1}	J	K
0	0	$\bar{Q}_n$	1	1
0	1	1	1	0
1	0	Q_n	0	0
1	1	0	0	1







24. (b)

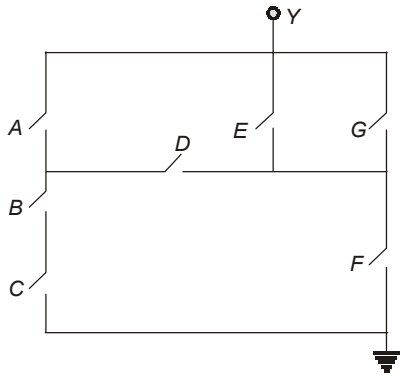
Full scale reading = Resolution × $(2^n - 1)$ = $2 \times 10^{-3} \times (2^8 - 1)$
= 510 mA

Error = $\pm\frac{0.5}{100}\times 0.51$ = 2.55 mA

Analog output = Decimal equivalent × Resolution
= 170 × 2 ± 2.55 mA
= (340 ± 2.55) mA

25. (d)

Drawing switch equivalent



From this Y is

$$Y = [ADF + ABC + (E + G)DBC + (E + G)\,F]'$$
$$Y = [ADF + ABC + (E + G)\,(DBC + F)]'$$

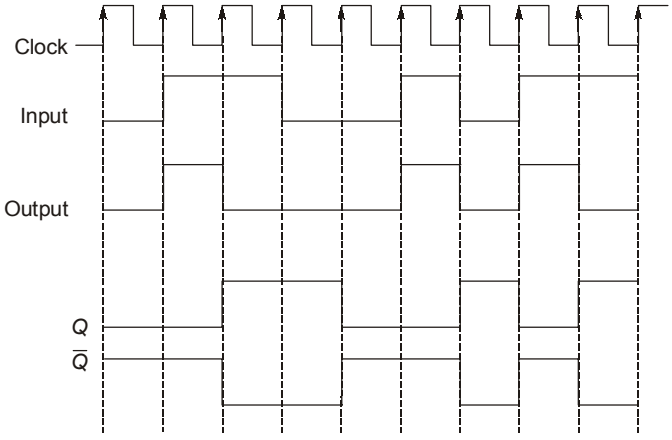
26. (c)

Output of counter

D_3	D_2	D_1	D_1	I_1	I_0	Y_2
0	0	0	0	0	1	0
0	0	0	1	1	1	0
0	0	1	0	1	1	0
0	0	1	1	0	1	0
0	1	0	0	0	0	0
0	1	0	1	1	0	1
0	1	1	0	1	0	1
0	1	1	1	0	0	0
1	0	0	0	0	0	0
1	0	0	1	1	0	1

$$\text{Duty cycle} = \frac{3}{10}\times 100 = 30\%$$

27. (c)



By checking all the options. Option (c) correctly matches.

28. (d)

NMOS requires less silicon area for fabrication.

29. (d)

An ADC must perform at a rate equal to at least twice the frequency of the highest component of the input. (according to Nyquist criterion)

If f_m is the highest frequency component in the message signal, then

$$T_{conv} = 100\ \mu\text{sec/sample} \le \frac{1}{2f_m\ (\text{samples/sec})}$$

i.e.,

$$f_m \le \frac{1}{2\times 100\times 10^{-6}}$$

$$f_m \le 5\ \text{kHz}$$

30. (b)

In ripple counter, $S = 4t_{pd} = 4 \times 20 = 80$ nsec

In synchronous counter, $R = t_{pd} = 20$ nsec [$\because$ all the flip-flops are clocked simultaneously in synchronous counter]

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