

**ESE | GATE | PSUs**

**State Engg. Exams**

**MADE EASY**  
**WORKBOOK 2025**



**Detailed Explanations of  
Try Yourself Questions**

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**Electronics Engineering**  
Digital Circuits



# 1

## Number Systems and Binary Codes



### Detailed Explanation of Try Yourself Questions

**T1. Sol.**

$$\begin{array}{r} 1\ 1\ 1\ 1\ 1 \\ -\ 1\ 0\ 0\ 1\ 1 \\ \hline 1\ 1\ 0\ 0 \\ +\ 1 \\ \hline 1\ 1\ 0\ 1 \end{array}$$

$$(1101)_2 = (13)_{10}$$

Therefore, the decimal equivalent value = -13.

**T2. (d)**

Given that,

$$\begin{aligned} (10)_x \times (10)_x &= (100)_x \\ x \times x &= x^2 \end{aligned}$$

and 
$$\begin{aligned} (100)_x \times (100)_x &= (10000)_x \\ x^2 \times x^2 &= x^4 \end{aligned}$$

so, above conditions are valid for all values of  $x$ .

**T3. (c)**

Converting both sides into decimal

$$\begin{aligned} (2^4 \times 1 + 0 + 2^2 \times w + 2^1 \times 1 + 2^0 \times z) \times 15 &= 2^8 y + 2^6 \times 1 + 2^4 \times 1 + 2^3 \times 1 + 2^0 \times 1 \\ (18 + 4w + z) \times 15 &= 256y + 64 + 16 + 8 + 1 \\ 270 + 60w + 15z &= 256y + 89 \end{aligned}$$

Only  $w = 1$ ,  $z = 1$  and  $y = 1$  satisfies.

**T4. (a)**

$$\begin{array}{r} 9\ 9\ 9\ 9\ 9 \\ -\ 2\ 5\ .\ 6\ 3\ 9 \\ \hline 7\ 4\ .\ 3\ 6\ 0 \end{array}$$





### Detailed Explanation of Try Yourself Questions

**T1. (c)**

Bulb is On when both switch S1 and S2 are in same state, either off or on.

S1	S2	Bulb
0	0	ON
0	1	OFF
1	0	OFF
1	1	ON

Above truth table derives EX-NOR operation.

**T2. (a)**

EXNOR gate on logic in called coincidence logic.

So,  $f = AB + A'B'$

**T3. (b)**

D will be '1' majority of input is 1, so

$$D = A \oplus B \oplus C$$

■■■■

# 3

## Combinational Logic Circuits



### Detailed Explanation of Try Yourself Questions

**T1. (c)**

Since the delay is of  $1 \mu\text{sec}$  the output will a square wave with time period of  $2 \mu\text{sec}$ .  
So, frequency =  $0.5 \text{ MHz}$

**T2. (a)**

For

$A_2$	$A_1$	$A_0$	$S_0$ ( $A_1$ )	$S_1$ ( $A_2$ )
0	0	0	0	0

MUX is enabled and output is  $I_0$

For

$A_2$	$A_1$	$A_0$	$S_0$	$S_1$
0	0	1	0	0

MUX is disable and output is '1'

Similarly, for

$A_2$	$A_1$	$A_0$	$S_0$	$S_1$	$\bar{E}$ ( $A_0$ )	O/P
0	0	0	0	0	0	$I_0$
0	0	1	0	0	1	1
0	1	1	0	1	1	1
0	1	0	0	1	0	$I_1$
1	1	0	1	1	0	$I_3$
1	1	1	1	1	1	1
1	0	1	1	0	1	1
1	0	0	1	0	0	$I_2$

**T3. (6)**

When,  $T = \text{logic } 0$ , the path followed by the circuit would be,  
NOR gate  $\rightarrow$  MUX 1  $\rightarrow$  MUX 2

$$\Rightarrow 2 \text{ ns} \rightarrow 1.5 \text{ ns} \rightarrow 1.5 \text{ ns}$$

$$\Rightarrow 5 \text{ ns}$$

When,  $T = \text{logic } 1$ , the path followed by the circuit would be,  
NOR gate  $\rightarrow$  MUX 1  $\rightarrow$  NOR gate  $\rightarrow$  MUX 2

$$\Rightarrow 1 \text{ ns} \rightarrow 1.5 \text{ ns} \rightarrow 2 \text{ ns} \rightarrow 1.5 \text{ ns}$$

$$\Rightarrow 6 \text{ ns}$$

$\therefore$  Maximum propagation delay is 6 ns

**T4. (c)**

**T5. (b)**

The number of AND gates in carry generator circuit in 'n' bit adder =  $\frac{n(n+1)}{2}$

$$\text{If } n = 4 \Rightarrow \frac{4(5)}{2} = 10.$$

The number of OR gates in carry generator circuit in 'n' bit adder = n.

$$\text{If } n = 4 \Rightarrow 4$$

**T6. (b)**

So, the input to adder is  $y$  and 1's complement  $x$  since carry input in 1.  
So, output is complement of  $x + 1$ , so output is  $y - x$ .

**T7. (b)**

$P_1$	$P_2$	$a$	$b$	$c$	$d$	$e$	$f$	$g$
0	0	1	1	1	1	1	1	0
0	1	1	0	1	1	0	1	1
1	0	1	1	0	1	1	0	1
1	1	1	0	0	1	1	1	1

$$a = 1$$

$$b = \bar{P}_2 \quad \dots 1 \text{ (NOT)}$$

$$c = \bar{P}_1 \quad \dots 1 \text{ (NOT)}$$

$$d = 1 = c + e$$

$$e = P_1 + \bar{P}_2 \quad \dots 1 \text{ (OR)}$$

$$f = \bar{P}_1 + P_2 \quad \dots 1 \text{ (OR)}$$

$$g = P_1 + P_2 \quad \dots 1 \text{ (OR)}$$

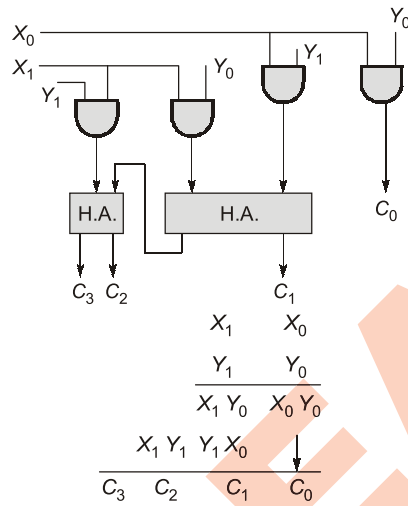
$$\Rightarrow \begin{aligned} g &= P_1 + P_2 \\ d &= 1 = c + e \end{aligned}$$

**T8. (d)**

- 2 – NOT gates
- 3 – OR gates

**T9. (b)**

Two bit binary multiplier



$$\begin{array}{r}
 X_1 \quad X_0 \\
 Y_1 \quad Y_0 \\
 \hline
 X_1 Y_0 \quad X_0 Y_0 \\
 X_1 Y_1 \quad Y_1 X_0 \\
 \hline
 C_3 \quad C_2 \quad C_1 \quad C_0
 \end{array}$$



# 4

## Sequential Circuits



### Detailed Explanation of Try Yourself Questions

**T1. (76.92)**

Total propagation delay  
 $= (t_{pd} + t_{\text{set-up}})_{\text{max}} = 8\text{ns} + 5\text{ns} = 13\text{ns}$   
 $\therefore$  Frequency of operations  
 $= \frac{1000}{13}\text{MHz} = 76.92\text{MHz}$

**T2. (c)**

**T3. (6)**

JK Flip-flop 1 and 2 form a synchronous sequential circuits and they are synchronized with the output of 0<sup>th</sup> JK Flip-flop.

$J_1$	$K_1$	$J_2$	$K_2$	$Q_2$	$Q_1$	$Q_0$
1	1	0	1	0	0	0
1	1	1	1	0	1	1
0	1	0	1	1	0	0
1	1	0	1	0	0	0

$\left. \begin{array}{l} \text{---} \\ \text{---} \\ \text{---} \end{array} \right\} T_1$   
 $\left. \begin{array}{l} \text{---} \\ \text{---} \end{array} \right\} T_2$   
 $\left. \begin{array}{l} \text{---} \\ \text{---} \end{array} \right\} T_3$

Number of cycles = 3 i.e. equal to 6 clock cycles.

**T4. (d)**

$$D = \bar{X}Z + Y\bar{Z}, D = \bar{K}Q + J\bar{Q}$$

$$Y = J, X = K, D = Q \text{ (for } D \text{ flip-flop)}$$

**T5. (d)**

Trick up/down =  $CP \oplus Q$ , 1 for up and 0 for down.

$CP$  = (clock pulse)

$Q$  = (O/P)

0 = -ve edge;  $Q = 1$

1 = +ve edge;  $\bar{Q} = 1$

=  $1 \oplus 1 = 0$  (down counter)

Counting sequence

1	1	1
1	1	0
1	0	1
1	0	0
0	1	1 (preset state) so Mod 5

**T6. (b)****T7. Sol.**

Clock	$Q_A$	$Q_B$	$Q_C$	$Q'_A$	$Q'_B$	$Q'_C$	$Q_A \oplus Q'_A$	$Q_B \oplus Q'_B$	$Q_C \oplus Q'_C$	Z
0	1	0	0	1	0	0	0	0	0	0
1	0	1	0	1	1	0	1	0	0	1
2	0	0	1	1	1	1	1	1	0	1
3	1	0	0	0	1	1	1	1	1	1
4	0	1	0	0	0	1	0	1	1	1
5	0	0	1	0	0	0	0	0	1	1
6	1	0	0	1	0	0	0	0	0	0

The output Z will again become zero after 6 clock cycles.

**T8. (c)**

The counter represents a Johnson counter. Thus, total number of states =  $2n$ . Where  $n = 3$ .

Therefore the MOD of the counter =  $2 \times 3 = 6$

**T9. (d)**

In a  $2^8$  Counter the range would be from 0-255.

Hence to go from 10101100 (172) to 00100111 (39), the counter has to go initially from 172 to 255 and then from 0 to 39.

Hence to go from 172 to 255,  $255 - 172 = 83$  Clock pulses would be required.

From 255 to 0, again 1 clock pulse would be required.

Then from 0 to 39, 39 clock pulses would be required.

Hence in total  $83 + 1 + 39 = 123$  Clock pulses would be required.





# 5

## Integrated-Circuit Logic Families



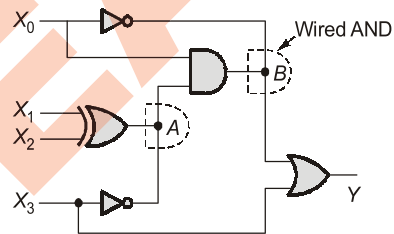
### Detailed Explanation of Try Yourself Questions

**T1. (8)**

$$A = (X_1 \oplus X_2) \bar{X}_3$$

$$B = [(X_1 \oplus X_2) \bar{X}_3 X_0] \cdot \bar{X}_0 = 0$$

$$Y = B + X_3 = 0 + X_3 = X_3$$



Out of 16 possible combinations of  $X_3 X_2 X_1 X_0$ ,  $X_3$  will be high for 8 combinations. So,  $Y$  will be high for 8 combinations.

**T2. (b)**

$$V_{OH} > V_{IH} > V_{IL} > V_{OL}$$

**T3. (b)**

It is CMOS gate where 2 PMOS are parallel and in series with 2 NMOS (series combination of NMOS). It is equivalent to NAND gate.

Series combination of NMOS equivalent to parallel combination of PMOS.

**T4. (c)**

Truth table:

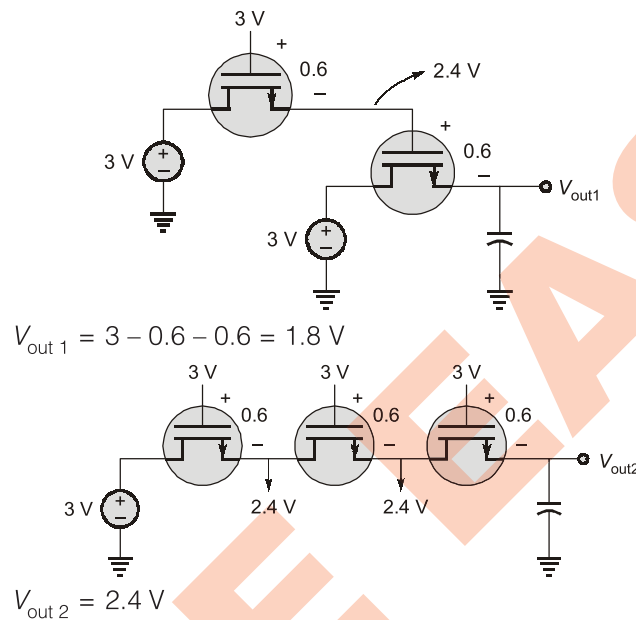
X	Y	$V_0$
0	0	1
0	1	0
1	0	0
1	1	0

$$V_0 = \overline{X+Y}$$

**T5. (a)**

Series combination of n-mos is equivalent to AND and parallel combination is equivalent to OR.

$$\text{So, } Y = \overline{C} \cdot (\overline{A+B}) = \overline{C} + \overline{(A+B)} = \overline{C} + \overline{A} \cdot \overline{B}$$

**T6. (c)****T7. (a)****T8. (c)**

- HTL → High noise immunity
- CMOS → Highest fanout
- $I^2L$  → Lowest of product power and delay
- ECL → Highest speed of operation

**T9. (a)**

For TTL logic floating input = 1

$$\therefore Y = (AB + 1)' = \overline{AB \cdot 0} = 0$$

**T10. (a)**

ECL is the fastest logic family.



# 6

## ADC and DAC



### Detailed Explanation of Try Yourself Questions

**T1. (a)**

Sequence of Johnson counter is

$Q_2$	$Q_1$	$Q_0$	$D_2$	$D_1$	$D_0$	$V_0$
0	0	0	0	0	0	0
1	0	0	1	0	0	4
1	1	0	1	1	0	6
1	1	1	1	1	1	7
0	1	1	0	1	1	3
0	0	1	0	0	1	1
0	0	0	0	0	0	0

**T2. (a)**

- Conversion time is the time taken for a new digital output to appear in response to a change in the input voltage.
- Flash converter is the fastest converter. It uses no clock signal.
- Type of  $N$ -bit ADC**

Type of $N$ -bit ADC	Max. conversion time
• Successive approximation	$N$ clock cycles
• Counter ramp	$2^N - 1$ clock cycles

**T3. (c)**

Initial state of the counter =  $(111)_2 = (7)_{10}$

So output will be equal to 7 V.

Next state of counter =  $(110)_2 = (6)_{10}$

So output should be = 6 V

But output is 3 V that means LSB of counter is connected to MSB of DAC and MSB of counter is connected to LSB of DAC.

Similarly next state of counter =  $(101)_2 = (5)_{10}$

Input to DAC =  $(101)_2 = (5)_{10}$

So output = 5 V

When counter goes to  $(100)_2$  then input to DAC =  $(001)_2 = (1)_{10}$

So output = 1 V

So connections are not proper.

**T4. (c)**

No. of comparators in a flash ADC is equal to  $2^n - 1$  where  $n$  = no. of bits.

$$2^4 - 1 = 15$$

**T5. (a)**

The reference voltage is 5 V.

The number of bits in ADC are 8.

$$\text{So, the resolution will be} = \frac{5}{2^8 - 1} = \frac{5}{255}$$

The applied input is 3.5 V.

The successive approximation ADC start working from the MSB so.

**After one clock:**

SAR will toggle its MSB from 0 → 1 so output of SAR will be 1000 0000.

**After second clock:**

SAR will toggle its 7<sup>th</sup> bit from 0 → 1 but 1100 0000 will result in value greater than 3.5 so output of SAR after 2<sup>nd</sup> clock will be 1000 0000.

**After third clock:**

SAR will toggle its 6<sup>th</sup> bit from 0 → 1 and output will be 10100000.

■■■■

# 7

## Semiconductor Memories



### Detailed Explanation of Try Yourself Questions

**T1. (b)**

$x_3$	$x_2$	$x_1$	$x_0$	$y_3$	$y_2$	$y_1$	$y_0$	
0	0	0	0	0	0	0	0	→ 0
0	0	0	1	0	0	0	1	→ 1
0	0	1	0	0	0	1	0	→ 2
0	0	1	1	0	0	1	1	→ 3
0	1	0	0	0	1	0	0	→ 4
0	1	0	1	0	1	0	1	→ 5
0	1	1	0	1	1	0	0	→ 6
0	1	1	1	1	1	0	1	→ 7
1	0	0	0	1	1	1	0	→ 8
1	0	0	1	1	1	1	1	→ 9

∴ It is 8421BCD to 2421BCD.

**T2. (b)**

