

# GATE

## MADE EASY WORKBOOK 2025



**Detailed Explanations of  
Try Yourself Questions**

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**Electronics Engineering  
Computer Organization**



# 2

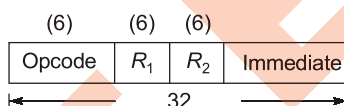
## Machine Instructions and Addressing Modes



### Detailed Explanation of Try Yourself Questions

#### T1 : Solution

(16383)



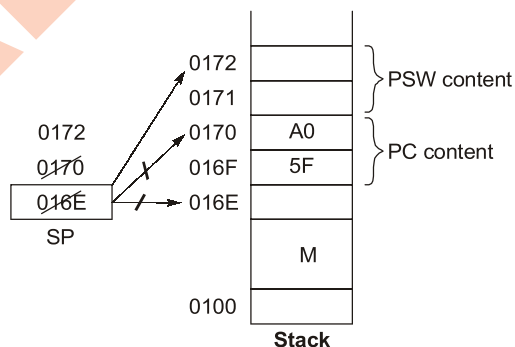
$$32 - (6 + 6 + 6) = 14 \text{ bits for immediate field}$$

⇒

$$2^{14} - 1 = 16383 \text{ maximum possible value of immediate operand.}$$

#### T2 : Solution

(d)



Just before CALL instruction execution, SP contains 016E

**While CALL execution:**

- (i) PC contents are pushed i.e., SP incremented by 2 ⇒ SP = 0170
  - (ii) PSW contents are pushed i.e., SP incremented by 2 ⇒ SP = 0172
- ∴ The value of stack pointer is  $(0172)_{16}$ .

**T3 : Solution**

(c)

$$EA = PC + \text{Address field value}$$

$$EA = 38248 + (-12) = 38236$$

**T4 : Solution**

(b)

$$\text{Number of registers} = 128$$

$$\text{Number of bits} = \log_2 128 = 7$$

Opcode	Register	Index address
$n$ bits	7 bits	$7+20$ bits

In indexing addressing mode effective memory location is stored in register.

$$\text{So Index Address bit} = \text{Register bit} + \text{Address bit}$$

$$= 7 + 20 = 27$$

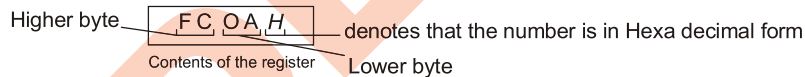
$$\therefore n + 7 + 27 = n + 34 \text{ is length of the instruction.}$$

**T5 : Solution**

(c)

The given instruction is stored in 16 bits register. The first byte (lower byte) of the instruction store at the memory location 4002 and second byte (higher byte) stored at 4003.

When we use little-endian mechanism the lower byte of the instruction is copied into lower byte of the register and higher byte of the instruction is copied into higher byte of the register.

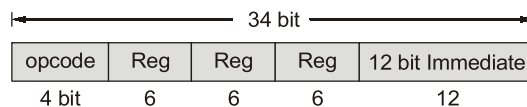


When we use big endian mechanism the lower byte of the instruction is copied into higher byte of the register and higher byte of the instruction is copied into lower byte of register.



**T6 : Solution**

(500)



One instruction size = 34 bit = 5 bytes

100 instruction occupies 500 bytes.

**T7 : Solution**

(b)

Average of time =  $\{(0.2 \times 0) + (0.2 \times 0) + (0.2 \times 4) + (0.1 \times 8) + (0.17 \times 6) + (0.13 \times 6)\} = 3.4$  cycles

$$\text{Clock cycle time} = \frac{1}{1} \text{ GHz} = 1 \text{ ns}$$

So, average of time =  $3.4 \text{ cycles} \times 1 \text{ ns} = 3.4 \text{ ns}$

1 operand 3.4 ns

Number of operands in 1 sec

$$\text{Number of operands} = \frac{1 \text{ operand}}{3.4 \text{ ns}} = 0.29411 \times 10^9 \text{ operand/sec.}$$

$\therefore$  Operand fetch rate = 294.11 million words/sec

**T8 : Solution**

(a)

- Indirect addressing → Passing array as parameter.
- Indexed addressing → Array implementation.
- Base register addressing → Writing relocatable code.

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# 3

## ALU, data-path and Control Unit



### Detailed Explanation of Try Yourself Questions

#### T1 : Solution

(a)

Average CPI =  $\Sigma(\text{IC} \times \text{CPI})$  cycle time

$$\text{Total IC} = \frac{(45000 \times 1) + (32000 \times 2) + (15000 \times 2) + (8000 \times 2)}{45000 + 32000 + 15000 + 8000} = 1.55 \text{ cycles}$$

$$\text{Cycle time} = \frac{1}{80 \text{ MHz}} \text{ sec} = 0.0125 \mu\text{sec}$$

$$\text{Average instruction ET} = (1.55 \times 0.0125) = 0.019375 \mu\text{sec}$$

1 instruction  $\Rightarrow$  0.019375  $\mu\text{sec}$

Number of instructions in 1 sec

$$\text{Number of instructions} = \frac{1}{0.019375} \times 10^6 \text{ inst./sec} = 51.61 \text{ MIPS}$$

#### T2 : Solution

(c)

In the given  $\mu$ -program we have used the register MAR, MBR and Instruction Register (IR).

IR is used only during fetching of the instruction.

Hence operation is instruction fetching.

#### T3 : Solution

(b)

Configurations for CPU in decreasing order of operating speeds: Hardwired control > Horizontal micro-programming > Vertical micro-programming (slowest because it involves decoding).

**T5 : Solution**

(10)

Atmost 2 control signals are active, that means for one signals minimum log (25) bits required i.e. 5.  
For 2 control signals =  $5 \times 2 = 10$  bits required.

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# 4

## Instruction Pipelining



### Detailed Explanation of Try Yourself Questions

#### T1 : Solution

(4)

$$\text{Speed up}(S) = \frac{\text{Pipe depth}}{(1 + \# \text{ stalls/instruction})}$$

$$\text{Number of stalls/instruction} = 0.75 \times 0 + 0.25 \times 2 = 0.5$$

$$\therefore S = \frac{6}{1+0.5} = 4$$

#### T2 : Solution

(c)

Clock cycle time = Maximum of stage delays.

For P1: clock cycle time = Maximum is 2

For P2: clock cycle time = Maximum is 1.5

For P3: clock cycle time = Maximum is 1

For P4: clock cycle time = Maximum is 1.1

Minimum clock cycle time gives the high clock rate.

Minimum of (2, 1.5, 1, 1.1) = 1

$\therefore$  P3 has peak clock cycle rate.

**T3 : Solution**

(3.2)

**Non-pipelined processor:** For  $n$  instructions execution time =  $(n \times 4) / 2.5 = 1.6 n$  nanoseconds.

**Pipelined processor:** For  $n$  instructions execution time =  $n / 2 = 0.5 n$  nanoseconds.

$$\text{Speedup} = 1.6 n / 0.5 n = 3.2$$

**T4 : Solution**

(c)

S <sub>4</sub>				I <sub>1</sub>	I <sub>2</sub>	I <sub>3</sub>	I <sub>4</sub>	I <sub>5</sub>	I <sub>6</sub>				
S <sub>3</sub>			I <sub>1</sub>	I <sub>2</sub>	I <sub>3</sub>	I <sub>4</sub>	I <sub>5</sub>	I <sub>6</sub>	I <sub>7</sub>				
S <sub>2</sub>		I <sub>1</sub>	I <sub>2</sub>	I <sub>3</sub>	I <sub>4</sub>	I <sub>5</sub>	I <sub>6</sub>	I <sub>7</sub>	I <sub>8</sub>				
S <sub>1</sub>	I <sub>1</sub>	I <sub>2</sub>	I <sub>3</sub>	I <sub>4</sub>	I <sub>5</sub>	I <sub>6</sub>	I <sub>7</sub>	I <sub>8</sub>	I <sub>12</sub>	I <sub>13</sub>	I <sub>14</sub>	I <sub>15</sub>	I <sub>16</sub>

So total 13 instruction are executed.

$$\begin{aligned} \therefore K &= 4; n = 13, t_p = 4 \text{ ns} \\ \text{ET} &= (K + n - 1) + t_p \\ &= (4 + 13 - 1) 4 \text{ ns} = 64 \text{ ns} \end{aligned}$$

**T5 : Solution**

(a)

	CC <sub>1</sub>	CC <sub>2</sub>	CC <sub>3</sub>	CC <sub>4</sub>	CC <sub>5</sub>	CC <sub>6</sub>	CC <sub>7</sub>	CC <sub>8</sub>	CC <sub>9</sub>	CC <sub>10</sub>
I <sub>1</sub>	IF	ID	OF	EX	MA	WB				
I <sub>2</sub>		IF	ID	OF	///	EX	MA	WB		
I <sub>3</sub>			IF	ID	///	OF	EX	MA	WB	
I <sub>4</sub>				IF	///	ID	OF	EX	MA	WB

**T6 : Solution**

(33.28)

P<sub>1</sub>: 4-stage

$$t_p = \text{Max (stage delay)} = 800 \text{ ps}$$

1 instruction — 800 ps

? number of instruction — 1 sec

$$TP_{P_1}(\text{throughput}) = 1250 \text{ instruction/sec}$$

P<sub>2</sub>: 5-stage

$$t_p = 600 \text{ ps}$$

1 instruction — 600 ps

? number of instruction — 1 sec

$$TP_{P_2}(\text{throughput}) = 1666 \text{ instruction/sec}$$



1250 — 100% (old)  
(1666 – 1250) — ? (New)

$$\Rightarrow \frac{416}{1250} = 0.3328$$

i.e., 33.28%

**T7 : Solution**

(4)

Given that, 3 stage pipeline with stage latencies

$$\tau_1 = \frac{3\tau_2}{4} = 2\tau_3 = \frac{3\tau_2}{4}, \frac{3\tau_2}{4} = 2\tau_3$$

$$\tau_1 : \tau_2 = 3 : 4, \tau_2 : \tau_3 = 8 : 3$$

Ratio of  $\tau_1 : \tau_2 : \tau_3$  is  $6x, 8x, 3x$  respectively. So, largest stage time  $8x$ .

So, calculate frequency =  $\frac{1}{8x}$

$$\Rightarrow \frac{1}{8x} = 3 \text{ GHz}$$

$$\Rightarrow \frac{1}{x} = 24 \text{ GHz} \quad \dots(1)$$

Now, largest stage latency divide into 2 half parts i.e.,  $8x$  divide into  $4x$  and  $4x$ .

So, 4 pipeline with stage latencies are  $6x, 4x, 4x, 3x$ .

Now, largest stage time =  $6x$

So, calculate new frequency =  $\frac{1}{6x}$

$$\frac{1}{6x} = \frac{24}{6} = 4 \text{ GHz}$$

[ $\because \frac{1}{x} = 24 \text{ GHz}$  from eq. (1)]

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