



MADE EASY

India's Best Institute for IES, GATE & PSUs

Delhi | Bhopal | Hyderabad | Jaipur | Pune | Bhubaneswar | Kolkata

Web: www.madeeasy.in | E-mail: info@madeeasy.in | Ph: 011-45124612

DIGITAL ELECTRONICS

EC + EE

Date of Test : 03/08/2023

ANSWER KEY >

- | | | | | |
|--------|---------|---------|---------|---------|
| 1. (b) | 7. (b) | 13. (c) | 19. (b) | 25. (a) |
| 2. (a) | 8. (d) | 14. (b) | 20. (a) | 26. (d) |
| 3. (c) | 9. (b) | 15. (d) | 21. (b) | 27. (c) |
| 4. (b) | 10. (d) | 16. (a) | 22. (b) | 28. (d) |
| 5. (c) | 11. (a) | 17. (d) | 23. (d) | 29. (b) |
| 6. (d) | 12. (d) | 18. (a) | 24. (b) | 30. (b) |

DETAILED EXPLANATIONS

1. (b)

$(1110011.0011)_2 \rightarrow$ Convert this binary no. to octal

001110011.001100

$(163.14)_8$

$(163.14)_8 \rightarrow$ Convert this octal no. to decimal

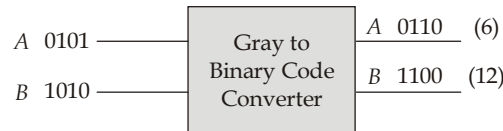
$$1 \times 8^2 + 6 \times 8 + 3 + \frac{1}{8} + \frac{4}{64}$$

$$= 64 + 48 + 3 + \frac{8+4}{64}$$

$$= 115 + \frac{3}{16}$$

$$= (115.1875)_{10}$$

2. (a)



$$6 < 12$$

$$A < B$$

$$X = 1$$

3. (c)

Clk	J_1	K_1	Q_1	J_2	K_2	Q_2
0	1	1	0	0	1	1
1	0	1	1	1	1	0
2	1	0	0	0	1	1
3	0	1	1	1	1	0

4. (b)

$$X = \overline{A}B + A\overline{B} = \overline{B}$$

$$Y = \overline{X}A + XA$$

$$Y = A$$

5. (c)

Conversion time for an n-bit successive approximation type ADC

$$= n T_{\text{clk}}$$

$$n = 8$$

Given,

Therefore,

$$T_{\text{conversion}} = 8 T_{\text{clk}}$$

$$= \frac{8}{f_{\text{clk}}} = \frac{8}{5 \times 10^6}$$

$$= 1.6 \times 10^{-6} \text{ sec}$$

$$= 1.6 \mu\text{sec}$$

6. (d)

$$\bar{Z} = (P + A)(Q + \bar{A})$$

$$\bar{Z} = PQ + AQ + \bar{A}P$$

$$Z = \bar{A} + B$$

$$\bar{Z} = \overline{\bar{A} + B} = A\bar{B}$$

$$Q = \bar{B}, P = 0$$

7. (b)

In ripple counter,

$$R = 4 \times 10 = 40 \text{ ns}$$

In synchronous counter,

$$S = T_c = 10 \text{ ns}$$

8. (d)

$$\begin{aligned} \text{From figure, } Z &= \bar{A}\bar{B}C + \bar{A}B + A\bar{B} + AB = \bar{A}(\bar{B}C + B) + A(\bar{B} + B) \\ &= \bar{A}(\bar{B}C + B) + A = (\bar{A} + A)(A + B + \bar{B}C) \\ &= (A + [(B + \bar{B})(B + C)]) \\ &= A + (B + C) \end{aligned}$$

Hence option (d) is correct

9. (b)

$$F = y_0 + y_2 + y_3 + y_4 + y_5 + y_7 = \Sigma m(0, 2, 3, 4, 5, 7)$$

10. (d)

$$\begin{aligned} t_{pd(\max)} &= n \times t_{pdff} \\ &= 3 \times 8 = 24 \text{ ns} \end{aligned}$$

11. (a)

$$\begin{aligned} Q(n) &= Q(n-1) \oplus X \\ \text{Output } Y &= X \cdot Q \end{aligned}$$

12. (d)

$$Y = \overline{\bar{A}\bar{B}C} \cdot (\bar{A}BC + \bar{A}BD + B\bar{C})$$

$$= (\bar{A} + B + \bar{C})(\bar{A}BC + \bar{A}BD + B\bar{C})$$

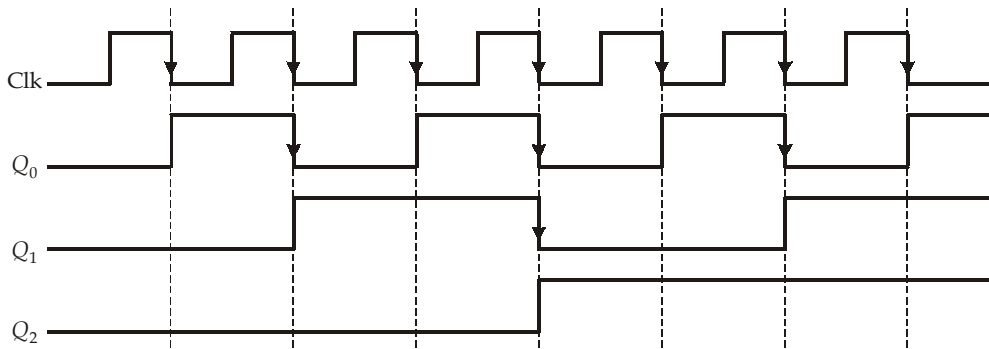
$$Y = \bar{A}BC + \bar{A}BD + \bar{A}B\bar{C} + B\bar{C} + \bar{A}B\bar{C}D$$

$$Y = \bar{A}BC + \bar{A}BD + B\bar{C} + \bar{A}B\bar{C}D$$

	$\bar{C}\bar{D}$	$\bar{C}D$	CD	$C\bar{D}$
$\bar{A}\bar{B}$				
$\bar{A}B$	1	1	1	1
AB	1	1		
$A\bar{B}$				

$$Y = B\bar{C} + \bar{A}B$$

13. (c)
Timing Diagram



Sequence followed by counter

000 - 001 - 010 - 011 - 100 - 101 - 110 - 111

It is an up-counter.

Flip-flops are cleared when $Q_2 \overline{Q_1} Q_0 = 111$

$$Q_2 Q_1 Q_0 = 101$$

Therefore it follows → $000 - 001 - 010 - 011 - 100$

It is a MOD-5 Up-counter.

14. (b)

Output of series NMOS = $A\overline{B}$

Output of CMOS inverter = $\overline{\overline{A\overline{B}}} \cdot 1 = \overline{A\overline{B}} = A\overline{B}$

15. (d)

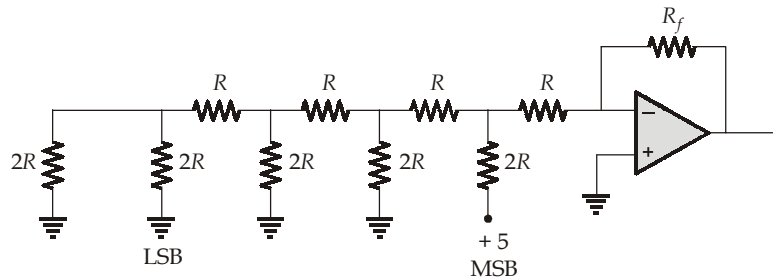
	J_0	K_0	Q_0	J_1	K_1	Q_1	J_2	K_2	Q_2
	1	1	0	0	1	0	1	1	0
①	1	1	1	1	1	0	1	1	1
②	1	1	0	0	1	1	0	1	0
③	1	1	1	1	1	0	1	1	0
④	1	1	0	0	1	1	0	1	1
⑤	1	1	1	1	1	0	1	1	0

4-clock pulse are required for the state $Q_2 Q_1 Q_0$ to become 110.

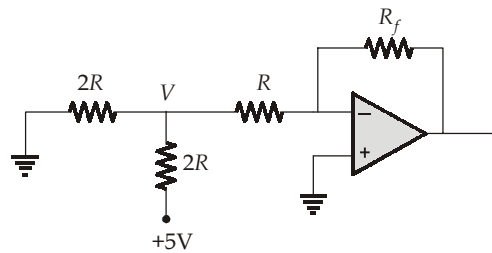
Time required = $4T$

$$= 4 \times \frac{1}{f} = 4 \times \frac{1}{10 \times 10^6} = 0.4 \mu\text{sec}$$

16. (a)



Reducing the ladder

Using nodal analysis to find voltage V .

$$\frac{V}{2R} + \frac{V-5}{2R} + \frac{V}{R} = 0$$

Given, $R = 5 \text{ k}\Omega$

$$\frac{V}{10K} + \frac{V-5}{10K} + \frac{V}{5K} = 0$$

$$\frac{V}{5K} + \frac{V}{5K} = \frac{5}{10K}$$

$$\frac{2V}{5K} = \frac{5}{10K}$$

$$V = \frac{5}{4} \text{ Volt}$$

Applying KCL at inverting terminal of op-amp.

$$\frac{V-0}{R} = \frac{0-V_0}{R_f}$$

$$V_0 = \frac{-R_f}{R} V$$

$$V_0 = \frac{-10}{5} \times \frac{5}{4}$$

$$V_0 = -2.5 \text{ Volts}$$

17. (d)

For input $AB = 00$ Transistor Q_1 and Q_2 are off Q_3 is ON, $\Rightarrow V_0 = 1$ For $AB = 10$ Q_1 ON, Q_2 OFF, Q_3 OFFOutput is not connected to ground and V_{CC} . \therefore Output is in high impedance (Z) state.

18. (a)

Clk	D_0	D_1	Q_0^+	Q_1^+
1	1	1	1	1
2	1	1	1	1
3	1	1	1	1

19. (b)

$$Y = (R + \bar{Q})(\bar{P}\bar{Q} + PQ) + P(\bar{P}Q + P\bar{Q})$$

$$Y = \bar{P}R\bar{Q} + PRQ + \bar{P}\bar{Q} + P\bar{Q}$$

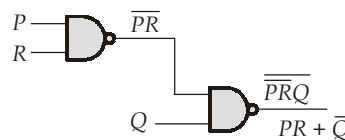
$$Y = PRQ + \bar{Q}(P + \bar{P} + \bar{P}R)$$

$$Y = PRQ + \bar{Q}(1 + \bar{P}R)$$

$$Y = PRQ + \bar{Q}$$

$$Y = (\bar{Q} + Q)(\bar{Q} + PR)$$

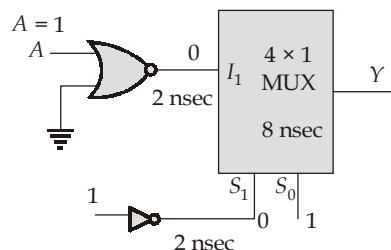
$$Y = PR + \bar{Q}$$



2- NAND are required to realise $PR + \bar{Q}$.

20. (a)

For $A = 1, B = 0$, the circuit is simplified as



Select line of 2nd MUX is ready after 2ns because input at I_1 is available after 2ns.

$$\text{Delay of MUX} = 8 \text{ nsec}$$

$$\text{Total delay of the circuit} = 8 + 2 = 10 \text{ ns}$$

Output will be stable after 10 ns.

21. (b)

Given Boolean function is,

$$Y(A, B, C, D) = \sum m(1, 3, 7, 11, 15) + d(0, 2, 5)$$

The function is defined in form of minterm don't care conditions K-map representation of the given function is shown. The simplified Boolean expression is,

$$Y(A, B, C, D) = CD + \bar{A}\bar{B}$$

		CD				
	AB	00	01	11	10	
00		×	1	1	×	→ $\bar{A}\bar{B}$
01			×	1		
11				1		
10				1		→ CD

22. (b)

The function f of the network is given by

$$f = 1 \cdot \bar{S}_0 + \bar{A} \cdot S_0$$

Output at MUX-1, f_1 is given to S_0 of the MUX-2, i.e.

$$f_1 = 0 \cdot \bar{C} + B \cdot C = BC$$

Hence, we get the output of the network as,

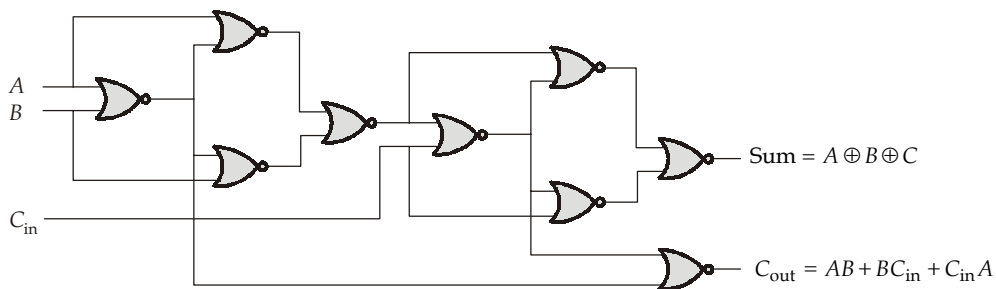
$$\begin{aligned} f &= 1 \cdot \bar{f}_1 + \bar{A} \cdot f_1 = \bar{B}\bar{C} + \bar{A}BC \\ &= (\bar{B}\bar{C} + \bar{A}) \cdot (\bar{B}\bar{C} + BC) \\ &= \bar{B}\bar{C} + \bar{A} \\ &= \bar{A} + \bar{B} + \bar{C} \\ &= \overline{ABC} \end{aligned}$$

23. (d)

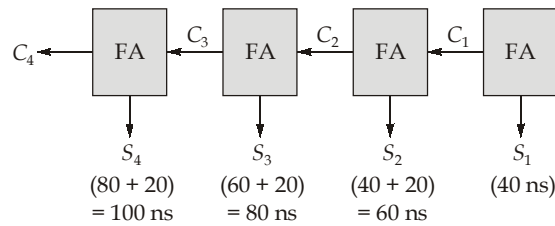
$$\begin{aligned} Q_{n+1} &= J\bar{Q}_n + \bar{K}Q_n \\ &= \bar{Q}_n \cdot \bar{Q}_n + \bar{1}Q_n \\ Q_{n+1} &= \bar{Q}_n \end{aligned}$$

24. (b)

$$\begin{aligned} \text{Sum} &= A \oplus B \oplus C \\ C_{\text{out}} &= AB + BC_{\text{in}} + C_{\text{in}}A \end{aligned}$$



25. (a)



$$\text{Maximum rate of addition} = \frac{1}{100 \text{ ns}} = 10^7 / \text{sec} = 10 \times 10^6 / \text{sec}$$

26. (d)

J_2	K_2	J_1	K_1	J_0	K_0	Q_2^+	Q_1^+	Q_0^+
						1	0	1
0	1	1	0	1	1	0	1	0
1	0	0	1	0	0	1	0	1
0	1	1	0	1	1	0	1	0
1	0	0	1	0	0	1	0	1

101 repeated after every two cycles, hence frequency of the output will be $\frac{15}{2} = 7.5 \text{ MHz}$.

27. (c)

$$(7.FD6)_{16} = (0111.1111111010110)_2$$

The binary number is converted into octal number as:

$$\begin{array}{cccccccc} \underbrace{000}_0 & \underbrace{111}_7 & \cdot & \underbrace{111}_7 & \underbrace{111}_7 & \underbrace{010}_2 & \underbrace{110}_6 & : \text{ Binary} \\ & & & & & & & : \text{ Octal} \end{array}$$

Thus, $(7.FD6)_{16} = (7.7726)_8$

Thus, $x = 8$

Also, $(7864)_{10} \rightarrow (1EB8)_y$

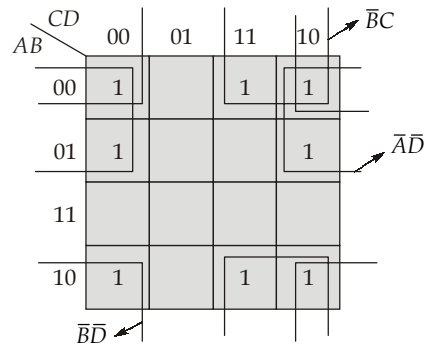
for $y = 16$, on converting decimal number $(7864)_{10}$ into hexadecimal number, we obtain $(1EB8)_{16}$ as follows:

16	7864	
16	491	$8 \rightarrow 8 \text{ (LSB)}$
16	30	$11 \rightarrow B$
16	1	$14 \rightarrow E$
	0	$1 \rightarrow 1 \text{ (MSB)}$

Thus, $(7864)_{10} = (1EB8)_{16}$

Hence, $y = 16$

28. (d)



The above k-map has 3 quads. Which are $\bar{A}\bar{D}, \bar{B}\bar{D}, \bar{B}C$
Therefore the minimized expression is $\bar{A}\bar{D} + \bar{B}\bar{D} + \bar{B}C$.

29. (b)

x	y	z	f
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

When $z = 0$

x	y	f
0	0	0
0	1	0
1	0	0
1	1	1

$f = xy$

When $z = 1$

x	y	f
0	0	0
0	1	1
1	0	1
1	1	1

$f = \bar{x}y + x\bar{y} + xy$

$f = y + x$

30. (b)

	$T_A = Q_A Q_B$	$T_B = \overline{Q_A Q_B}$	Q_A	Q_B	
	0	1	0	0	(Initially)
1 st clock →	0	0	0	1	
2 nd clock →	0	0	0	1	

