CLASS TEST

Sl. : 03 SK_EC+EE_ABCD_030823

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EC + EE

DIGITAL ELECTRONICS

Duration : 1:00 hr. **Maximum Marks : 50**

Read the following instructions carefully

1. This question paper contains **30** objective questions. **Q.1-10** carry one mark each and **Q.11-30** carry two marks each.
2. Answer all the questions.
3. Questions must be answered on Objective Response Sheet (**ORS**) by darkening the appropriate bubble (marked **A**, **B**, **C**, **D**) using HB pencil against the question number. Each question has only one correct answer. In case you wish to change an answer, erase the old answer completely using a good soft eraser.
4. There will be **NEGATIVE** marking. For each wrong answer **1/3rd** of the full marks of the question will be deducted. More than one answer marked against a question will be deemed as an incorrect response and will be negatively marked.
5. Write your name & Roll No. at the specified locations on the right half of the **ORS**.
6. No charts or tables will be provided in the examination hall.
7. Choose the **Closest** numerical answer among the choices given.
8. If a candidate gives more than one answer, it will be treated as a **wrong answer** even if one of the given answers happens to be correct and there will be same penalty as above to that questions.
9. If a question is left blank, i.e., no answer is given by the candidate, there will be **no penalty** for that question.

DO NOT OPEN THIS TEST BOOKLET UNTIL YOU ARE ASKED TO DO SO

Q.No. 1 to Q.No. 10 carry 1 mark each

Q.1 The value of X and Y is

$(1110011.0011)_2 = (X)_8 = (Y)_{10}$

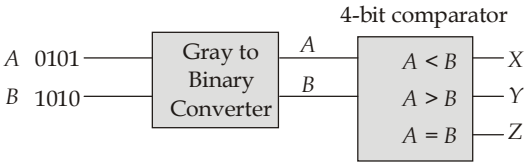
(a) $X = 163.14 \quad Y = 110.3$

(b) $X = 163.14 \quad Y = 115.1875$

(c) $X = 155.30 \quad Y = 110.3$

(d) $X = 155.3 \quad Y = 115.1875$

Q.2 The output of the 4-bit comparator is



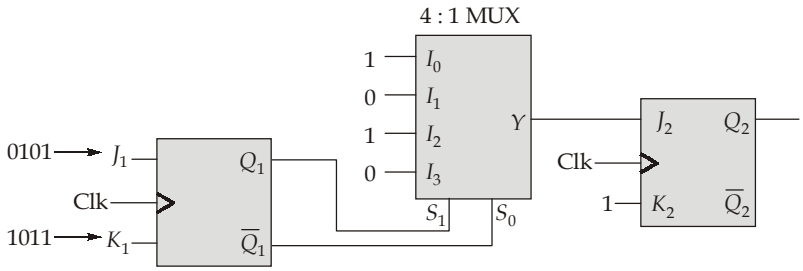
(a) $X = 1, Y = 0, Z = 0$

(b) $X = 0, Y = 1, Z = 0$

(c) $X = 1, Y = 0, Z = 1$

(d) $X = 0, Y = 0, Z = 1$

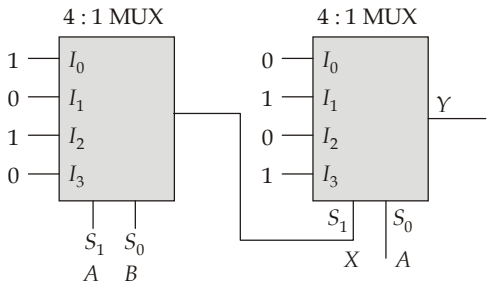
Q.3 Identify the state of the flip-flops Q_2Q_1 after 3 clock cycles if the initial state, $Q_1Q_2 = 01$.



(a) 10 (b) 11

(c) 01 (d) 00

Q.4 The final expression Y at the output of the MUX is



(a) $A + B$ (b) A

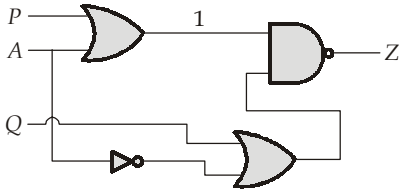
(c) $A + \overline{B}$ (d) $\overline{B}$

Q.5 The input clock frequency to an 8-bit successive approximation ADC is 5 MHz. The time required to convert 16 V analog input into equivalent digital output is

(a) 0.5 μsec (b) 1 μsec

(c) 1.6 μsec (d) 2.5 μsec

Q.6 The circuit shown below is used the implement the function $Z = f(A, B) = \overline{A} + B$. The values of P and Q are:



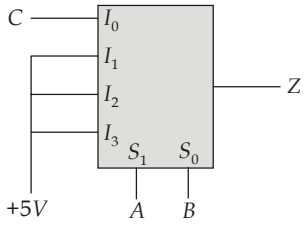
(a) $P = A, Q = B$ (b) $P = B, Q = \overline{A}$

(c) $P = \overline{B}, Q = 0$ (d) $P = 0, Q = \overline{B}$

Q.7 A 4-bit ripple counter and 4-bit synchronous counter are made by flip-flops having propagation delay of 10 ns each. If the worst case delay in the ripple counter and the synchronous counter be R and S respectively then,

(a) R = 10 ns, S = 40 ns
(b) R = 40 ns, S = 10 ns
(c) R = 10 ns, S = 30 ns
(d) R = 30 ns, S = 10 ns

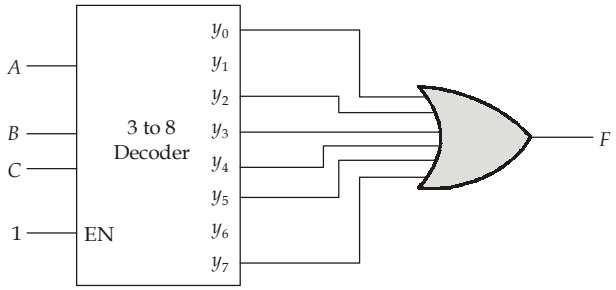
Q.8 The MUX shown below is 4 × 1 multiplexer. The output for an input of A, B, C will be



(a) ABC (b) $A \oplus B \oplus C$

(c) $A \odot B \odot C$ (d) $A + B + C$

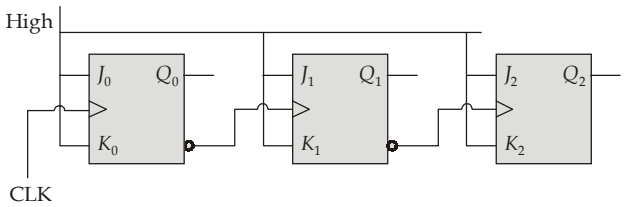
Q.9 The circuit shown below represents a Boolean expression. Number of minterms present in the Boolean expression are



(a) 4 (b) 6

(c) 8 (d) 12

Q.10 In the given counter, each flip-flop has a propagation delay of 8 ns.



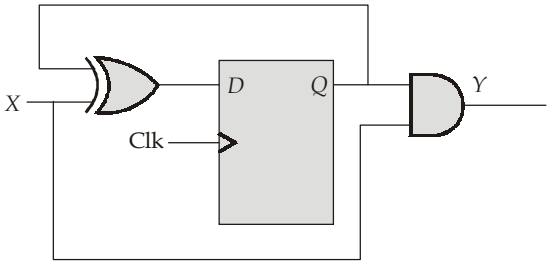
The worst-case (longest) delay time from a clock pulse to the arrival of the counter in a given state is

(a) 10 nsec (b) 12 nsec

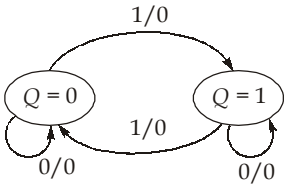
(c) 15 nsec (d) 24 nsec

Q.No. 11 to Q.No. 30 carry 2 marks each

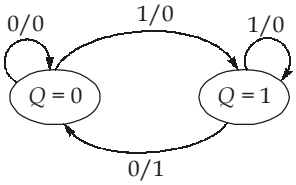
Q.11 Which of the following represents the correct state diagram for circuit given with input X and output Y?



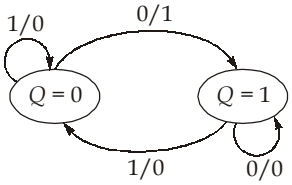
(a)



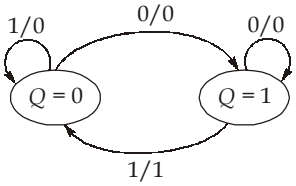
(b)



(c)



(d)



Q.12 Consider the Boolean expression given below

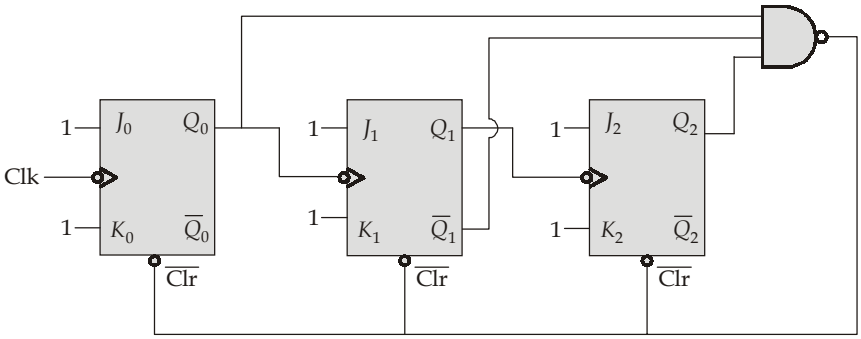
$$Y = \overline{A\bar{B}C + \bar{\bar{A}}B(C+D) + B\bar{\bar{C}}}$$

The simplified Boolean expression for Y is

(a) $\bar{A}\bar{B} + BC$ (b) $A\bar{B} + \bar{B}C$

(c) $\bar{A}B + \bar{B}\bar{C}$ (d) $\bar{A}B + B\bar{C}$

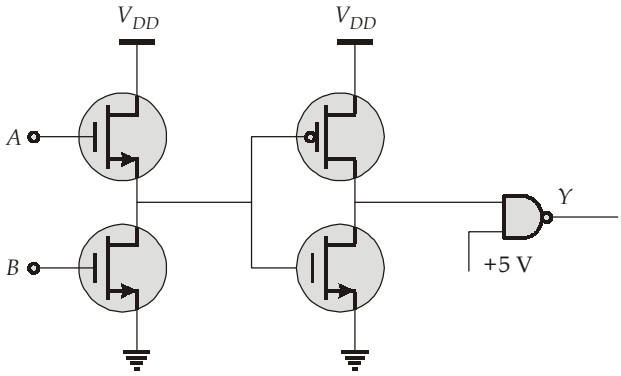
Q.13 Identify the type of asynchronous counter and the MOD number. Assume initial state $Q_2Q_1Q_0$ to be 000.



(a) Up-counter, MOD-3 (b) Down-counter, MOD-5

(c) Up-counter, MOD-5 (d) Down-counter, MOD-3

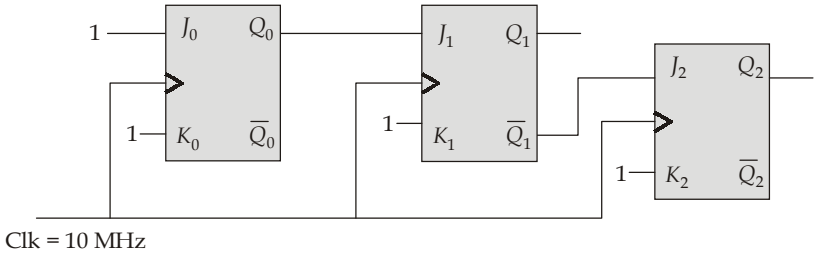
Q.14 The output Y can be represented by



(a) $B(A+B)(\bar{A}+\bar{B})$ (b) $(A+B)(\bar{A}+\bar{B})A$

(c) $(A+\bar{B})(\bar{A}+B)$ (d) $(\bar{A}+\bar{B})(\bar{A}+B)$

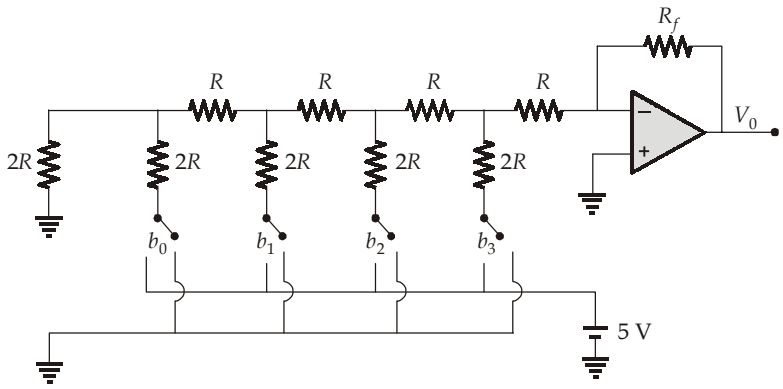
Q.15 In the circuit given below, initial state $Q_0Q_1Q_2$ = 000. The time taken by state $Q_2Q_1Q_0$ to become 110 is



(a) 0.1 μsec (b) 0.2 μsec

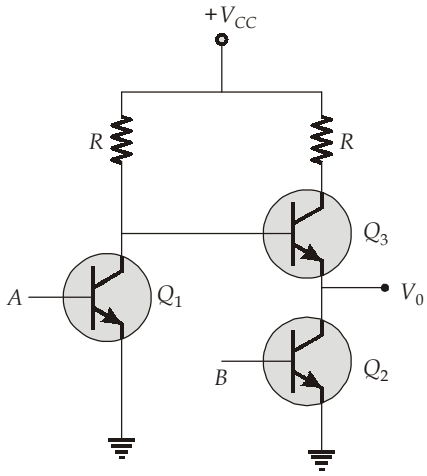
(c) 0.3 μsec (d) 0.4 μsec

Q.16 If the input to the ladder DAC is 1000. What is the value of output voltage V_0 if R = 5 kΩ and R_f = 10 kΩ?



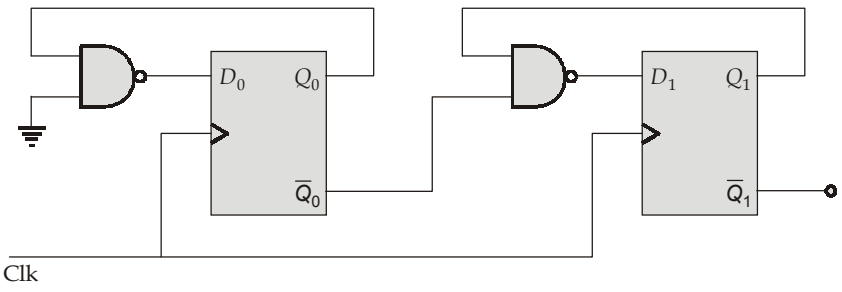
(a) –2.5 V
(b) 2.5 V
(c) –5 V
(d) 5 V

Q.17 In the given circuit, V_0 is the output, A and B are the inputs. The output can take the values 0, 1 and high impedance state (Z).
The output of the given circuit is



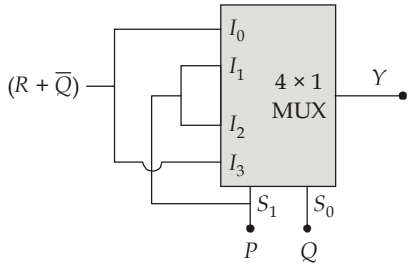
(a) V_0 = 0 if AB = 00
(b) V_0 = 1 if AB = 11
(c) V_0 = 1 if AB = 10
(d) $V_0 = Z$ if AB = 10

Q.18 What is the state Q_1Q_0 of the counter after 3 clock cycles, given initial state of the counter Q_0Q_1 = 10?



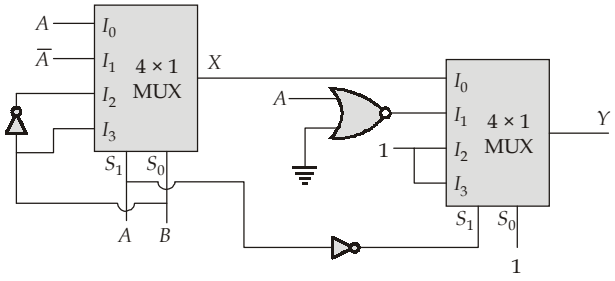
(a) 11
(b) 10
(c) 01
(d) 00

Q.19 The minimum number of 2-input NAND gates required to realise the minimized output expression Y of the given 4 × 1 MUX is



(a) 1 (b) 2
(c) 3 (d) 4

Q.20 The propagation delay of 4 × 1 MUX is 8 ns and delay of NOR and NOT gates is 2ns. For $A = 1$, $B = 0$ the output Y will be stable in

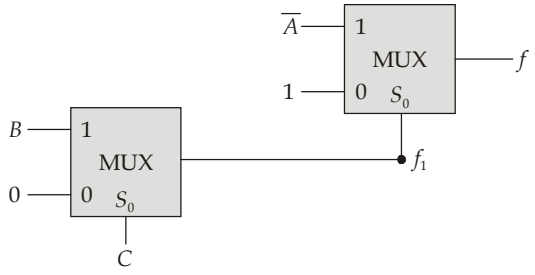


(a) 10 nsec (b) 5 nsec
(c) 15 nsec (d) 20 nsec

Q.21 Assume $Y = f(A, B, C, D)$ the Boolean expression $Y = \Sigma m(1, 3, 7, 11, 15) + d(0, 2, 5)$ in its simplified form is given as,

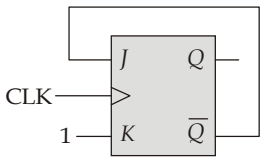
(a) $CD + AB$ (b) $CD + \overline{A}\,\overline{B}$
(c) $AC + \overline{B}\,\overline{D}$ (d) $AC + BD$

Q.22 The network shown below implements:



(a) NOR gate (b) NAND gate
(c) XOR gate (d) XNOR gate

Q.23 The JK flip-flop shown below is initially cleared and then 5 clock pulses are applied, the sequence at the Q output will be



(a) 010000 (b) 011001
(c) 010010 (d) 010101

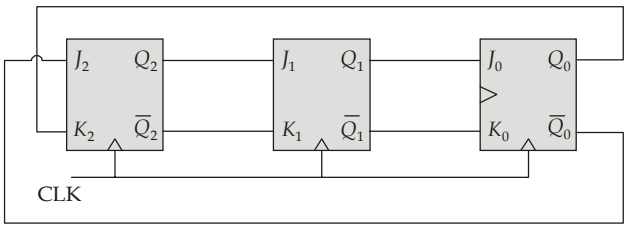
Q.24 A full adder is realized using only 2 input NOR gates. The minimum number of NOR gates required to realize Sum and Carry out is

(a) 8 (b) 9
(c) 10 (d) 12

Q.25 A 1-bit full-adder takes 20 ns to generate carry-out bit and 40 ns for the sum bit. The maximum rate of addition per second, when four 1-bit full adders are cascaded is

(a) 10×10^6 (b) 10×10^4
(c) 5×10^6 (d) 5×10^4

Q.26 The three stage Johnson counter as shown in figure below is clocked at a constant frequency of 15 MHz from the starting state of $Q_2\,Q_1\,Q_0 = 101$. The frequency of output $Q_2\,Q_1\,Q_0$ will be



(a) 5 MHz (b) 4.5 MHz
(c) 6 MHz (d) 7.5 MHz

Q.27 If $(7.FD6)_{16} = (7.7726)_x$ and $(7864)_{10} = (1EB8)_y$. Then the values of x and y are respectively

(a) 4 and 8 (b) 10 and 16
(c) 8 and 16 (d) 8 and 8

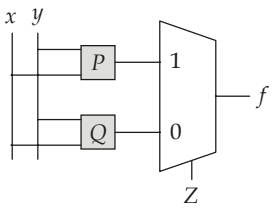
Q.28 The minimized expression for the Boolean function

$f(A, B, C, D) = \Sigma m\ (0, 2, 3, 4, 6, 8, 10, 11)$

(a) $\bar{A}\bar{D} + \bar{B}D + \bar{B}C$ (b) $\bar{A}\bar{D} + B\bar{D} + B\bar{C}$

(c) $\bar{A}\bar{D} + \bar{B}\bar{D} + BC$ (d) $\bar{A}\bar{D} + \bar{B}\bar{D} + \bar{B}C$

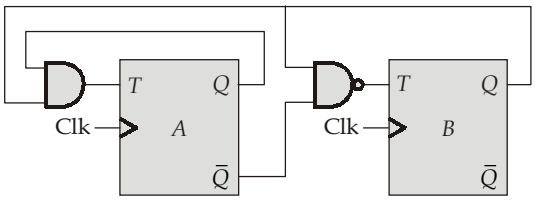
Q.29 The majority function is a Boolean function $f(x, y, z)$, that takes the value 1 whenever a majority of variables x, y, z are 1. In the circuit diagram for the majority function shown below. The logic gates for the boxes labeled P and Q are, respectively



(a) AND, OR (b) OR, AND

(c) EXOR, OR (d) EXOR, AND

Q.30 The circuit shown in figure below is,



Initially both flip-flops are at 00. After two clock pulses, the content at $Q_A Q_B$ is

(a) 00 (b) 01

(c) 10 (d) 11

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