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DIGITAL ELECTRONICS

EC-EE

Date of Test : 19/01/2024

ANSWER KEY ➤

1.	(b)	7.	(c)	13.	(c)	19.	(a)	25.	(d)
2.	(b)	8.	(b)	14.	(c)	20.	(c)	26.	(a)
3.	(a)	9.	(b)	15.	(b)	21.	(d)	27.	(a)
4.	(c)	10.	(d)	16.	(a)	22.	(d)	28.	(a)
5.	(b)	11.	(b)	17.	(b)	23.	(b)	29.	(b)
6.	(d)	12.	(d)	18.	(b)	24.	(c)	30.	(c)

DETAILED EXPLANATIONS

1. (b)

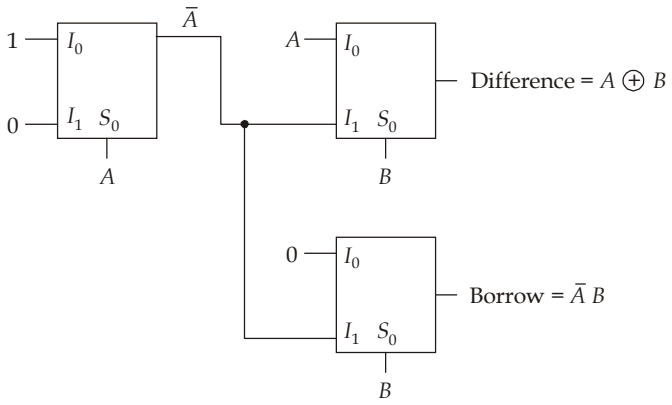
In J-K flip-flop

J	K	Output
1	0	Set
0	1	Reset
0	0	Hold
1	1	Racearound

2. (b)

$$\begin{aligned} X \oplus Y &= \overline{X \odot Y} = \overline{\bar{X}\bar{Y} + XY} \\ &= \overline{(\bar{X}\bar{Y})}\,\overline{(XY)} \\ &= (X+Y)(\bar{X}+\bar{Y}) \\ &= \bar{X}+\bar{Y} \qquad (\because\ X+Y=1 \text{ which is given}) \end{aligned}$$

3. (a)



4. (c)

The expression of Y can be written as

$$Y = (A)\bar{A}\bar{B} + (B)\bar{A}B + (B)A\bar{B} + (A)AB = \bar{A}B + AB = B$$

5. (b)

Dual slope A/D convertor has the highest accuracy among the given converters.

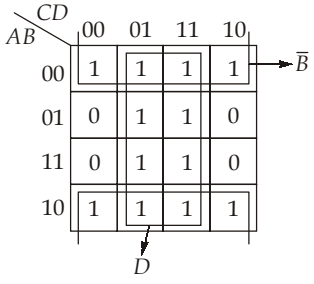
6. (d)

7. (c)

8. (b)

9. (b)

By properly arranging the given k-map.



$\therefore \quad f = \overline{B} + D$

$\therefore$ Complement, $f^C = B\overline{D}$

10. (d)

11. (b)

The given circuit represents a 3-bit counter. So the count can be represented as

Clk	Q_2	Q_1	Q_0	
Initially	0	0	0	
1	0	0	1	
2	0	1	0	
3	0	1	1	
4	1	0	0	
5	1	0	1	$\Rightarrow$5th clock pulse
6	1	1	0	
7	1	1	1	

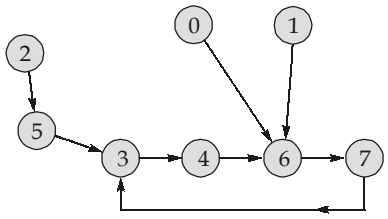
$\therefore \quad Y = Q_2 \oplus Q_1 \oplus Q_0$

$= 1 \oplus 0 \oplus 1 = 0$

12. (d)

Test for Lockout

Present State			Present Input						Nest State		
Q_2	Q_1	Q_0	J_2	K_2	J_1	K_1	J_0	K_0	Q_2	Q_1	Q_0
0	0	0	1	0	1	1	0	1	1	1	0
0	0	1	1	1	1	1	0	1	1	1	0
0	1	0	1	0	1	1	1	1	1	0	1
1	0	1	1	1	1	0	0	0	0	1	1



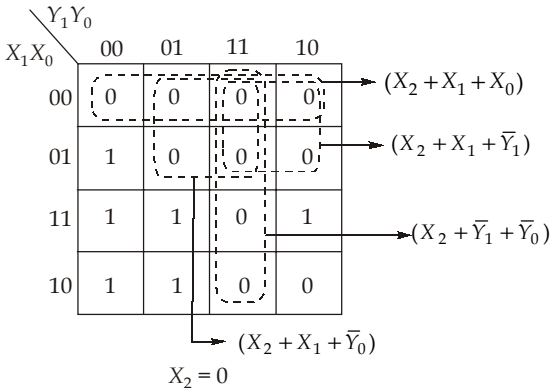
Hence, the counter does not enter into lockout state.

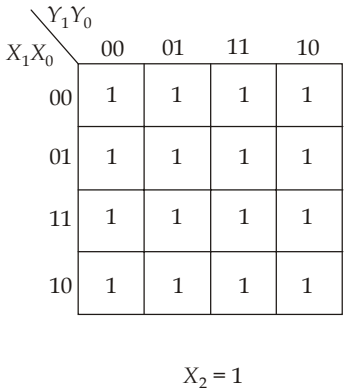
13. (c)

Now, $X > Y$ if

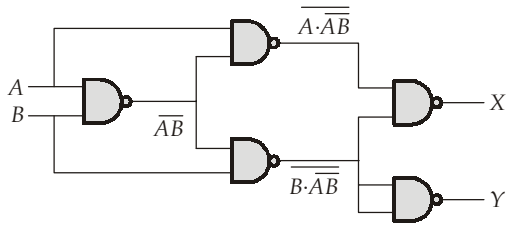
(a) $X_2 = 1$

(b) $X_2 = 0$ and $X_1X_0 > Y_1Y_0$





14. (c)

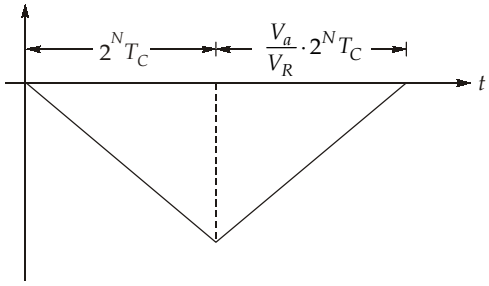


$$X = \overline{B}(A+B)+\overline{A}(A+B)$$
$$= A\overline{B}+\overline{A}B = A\oplus B$$
$$Y = B(\overline{AB})$$
$$= B(\overline{A}+\overline{B}) = \overline{A}B$$

The above circuit represents a half subtracter constructed using only NAND gates. Thus the truth table can be written as

A	B	Difference (X)	Borrow (Y)
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

15. (b)



Total conversion time, $(t) = 2^N T_C + \frac{V_a}{V_R}\cdot 2^N T_C$

Where,
N = Number of bits of converter
T_C = Time period of the clock
V_a = Analog voltage
V_R = reference voltage

The largest V_a can be equal to V_R therefore,

$$V_a = V_R$$
$$t = 2^{N+1}\,T_C$$
$$t = 2^{12+1}\cdot T_C$$
$$t = 2^{13}\times\frac{1}{100\times 10^3}\text{sec}$$
$$t = \frac{8192}{10^5}$$
$$f < \frac{10^5}{8192}$$

$$f < 12.20$$

$$\therefore \quad f_{max} = 12 \text{ Hz}$$

16. (a)

$$P = \bar{B}\bar{C}A + \bar{B}C\bar{A} + B\bar{C}\bar{A} + BCA$$

$$= \bar{A}[B\bar{C} + \bar{B}C] + A[BC + \bar{B}\bar{C}]$$

$$= \bar{A}[B \oplus C] + A[\overline{B \oplus C}]$$

$$P = A \oplus B \oplus C$$

$$P(A, B, C) = \Sigma m(1, 2, 4, 7)$$

$$Q = \bar{B}\bar{C} \cdot 0 + \bar{B}C\bar{A} + B\bar{C}\bar{A} + BC$$

$$= \bar{B}C\bar{A} + B\bar{C}\bar{A} + BC(A + \bar{A})$$

$$= \bar{B}C\bar{A} + B\bar{C}\bar{A} + ABC + \bar{A}BC$$

$$Q(A, B, C) = \Sigma m(1, 2, 3, 7)$$

17. (b)

From the given code converter we can write

x + (1's complement of 0011) + 1 = BCD

$$x + 1100 + 1 = \text{BCD}$$

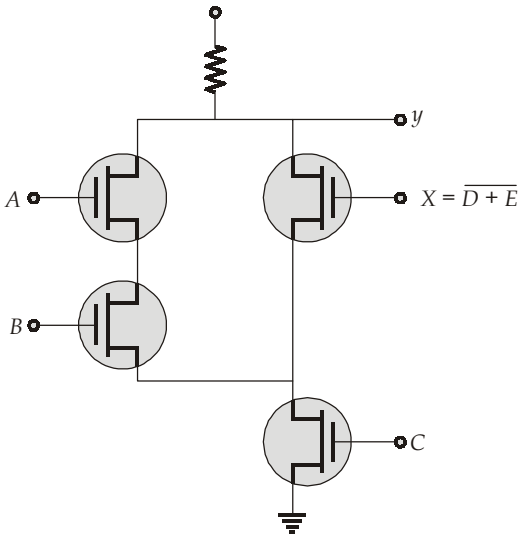
$$x + 1101 = \text{BCD}$$

$$x = \text{BCD} - 1101 = \text{BCD} + (2\text{'s complement of } 1101)$$

$$\therefore \quad x = \text{BCD} + 0011 = \text{Excess-3 code}$$

18. (b)

By redrawing the given circuit,

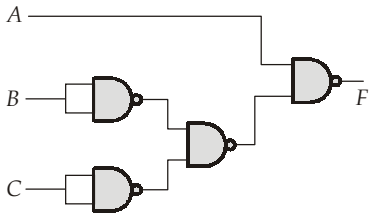


$$\therefore \quad y = \overline{(AB + X) \cdot C} = \overline{\left(AB + (\overline{D + E})\right) \cdot C}$$

$$y = \bar{C} + (\bar{A} + \bar{B})(D + E)$$

19. (a)

$$F = \overline{A(B+C)}$$



20. (c)

From the given diagram,

$$J_1 = \bar{Q}_1 Q_2$$
$$K_1 = \bar{Q}_2$$
$$J_2 = K_2 = \bar{Q}_1$$

Also given, $Q_1 = 0$; $Q_2 = 0$ initially

Clk	Q_1	Q_2	J_1	K_1	J_2	K_2
0	0	0	0	1	1	1
1	0	1	1	0	1	1
2	1	0	0	1	0	0
3	0	0	0	1	1	1

$\therefore$ It is MOD-3 counter.

21. (d)

PS		NS		FF inputs	
Q_A	Q_B	Q_A	Q_B	J_B	k_B
0	0	1	1	1	x
1	1	1	0	x	1
1	0	0	1	1	x
0	1	0	0	x	1

On solving for J_B and k_B

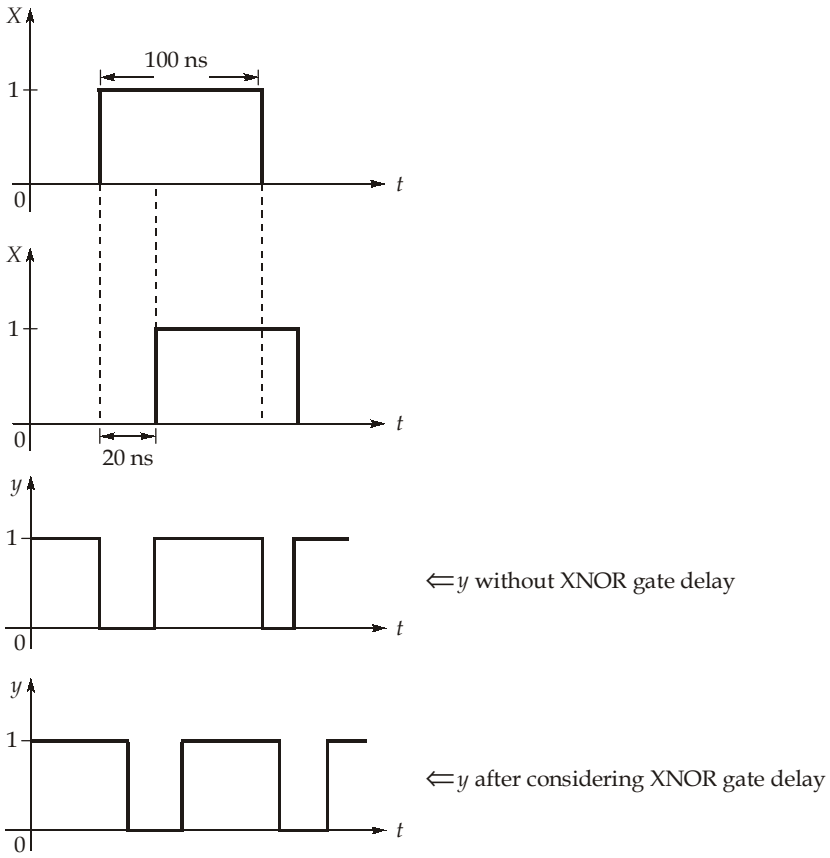
Q_A \ Q_B	0	1
0	1	x
1	1	x

$J_B = 1$

Q_A \ Q_B	0	1
0	x	1
1	x	1

$k_B = 1$

22. (d)



23. (b)

$$\begin{aligned} f_2 &= \bar{x}_0x_1 + x_1x_2 + x_0\bar{x}_1\bar{x}_2 \\ &= \bar{x}_0x_1x_2 + \bar{x}_0x_1\bar{x}_2 + x_0x_1x_2 + \bar{x}_0x_1x_2 + x_0\bar{x}_1\bar{x}_2 \\ &= \Sigma m(1, 2, 6, 7) \end{aligned}$$

24. (c)

Given, initially, PQR is 010.

$$D_1 = R, \quad D_2 = \overline{PR}, \quad D_3 = Q \odot \bar{R}$$

Clk	D_1	D_2	D_3	P	Q	R
0	0	1	1	0	1	0
1	1	1	0	0	1	1
2				1	1	0

25. (d)

26. (a)

Input equations of flip-flops

$$T_A = BX, T_B = X, Y = AB$$

State equations, $A(t+1) = T'A + TA'$

$$= (BX)'A + (BX)A'$$

$$= AB' + AX' + A'BX$$

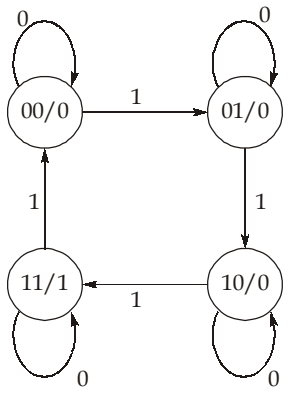
$$B(t+1) = T'B + TB'$$

$$= X'B + XB' = X \oplus B$$

State table:

Present State		Input	Next State		Output
A	B	X	A	B	Y
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	0	1	0
0	1	1	1	0	0
1	0	0	1	0	0
1	0	1	1	1	0
1	1	0	1	1	1
1	1	1	0	0	1

State diagram:



27. (a)

$$000 \xrightarrow{1^{st}\ CLK} 100 \xrightarrow{2^{nd}\ CLK} 010 \xrightarrow{3^{rd}\ CLK} 101$$

The op-amp circuit is a R-2R Ladder DAC with digital input 101. Therefore,

$$V_0 = -\left(\frac{R_f}{R}\right)\times\left(\frac{V_{ref}}{2^3}\right)\times(\text{Decimal equivalent of } 101)$$

$$V_0 = \frac{-R}{R}\times\frac{5}{8}\times 5$$

$$V_0 = -3.125\ \text{V}$$

28. (a)

$$\begin{array}{r} 10W1Z \\ \times\ 1111 \\ \hline (10)(10)\ (1)\ (0) \\ (10)10W1Z \\ (10)10W1Z \\ 10W1Z \\ 10W1Z \\ \hline 10101100Z \end{array} \quad [\Theta 15_{10} = (1111)_2]$$

$= Y01011001$

$Y = 1$, $Z = 1$

$1 + W + 1 + Z = 100 (W = 1)$

Carry

$\therefore \quad (WYZ)_2 = (111)_2 = 7$

29. (b)

There are three data paths (flop A to flop B, flop A to flop C, flop B to flop C). Setup time is used for deriving the maximum clock frequency.

Path $A \rightarrow B$: $t_{CLK} > t_{CLK \rightarrow Q} + t_s = 9 + 2 \Rightarrow t_{CLK} > 11$ ns

Path $A \rightarrow C$: $t_{CLK} > t_{CLK \rightarrow Q} + t_s + t_{pd} = 9 + 2 + 4 \Rightarrow t_{CLK} > 15$ ns

$t_{clk} > 15$ nsec

$$f_{max} = \frac{1}{t_{clk}\,(min)} = \frac{1}{15 \times 10^{-9}} = 66.67 \text{ MHz}$$

30. (c)

We know that

$$t_{setup} \leq t_{clk} - t_{pd,\,D} - t_{pd,\,CL}$$

for maximum setup time,

$$\begin{aligned} t_{setup} &= t_{clk} - t_{pd,\,D} - t_{pd,\,CL} \\ &= 25 - 6 - \max(11, 9) \\ &= 25 - 6 - 11 \\ &= 8 \text{ ns} \end{aligned}$$

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